ECE 3040 Microelectronic Circuits

Exam 2

March 17, 2006

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Print your name clearly and largely: Solutions

Instructions:
Read all the problems carefully and thoroughly before you begin working. You are allowed to use 1 new sheet of notes (1 page front and back), your note sheet from the previous exam as well as a calculator. There are 100 total points in this exam. Observe the point value of each problem and allocate your time accordingly. SHOW ALL WORK AND CIRCLE YOUR FINAL ANSWER WITH THE PROPER UNITS INDICATED. Write legibly. If I can not read it, it will be considered to be a wrong answer. Do all work on the paper provided. Turn in all scratch paper, even if it did not lead to an answer. Report any and all ethics violations to the instructor. Good luck!

Sign your name on **ONE** of the two following cases:

I DID NOT observe any ethical violations during this exam:

I observed an ethical violation during this exam:

Solutions

First 20% **True /False and Multiple Choice - Select the most correct answer(s)**

1.) (2-points) True / [✓ False]: The depletion capacitance of a transistor junction increases in magnitude with increasing reverse bias.

2.) (2-points) [✓ True] / False: The law of the junction predicts increasing voltage for excess minority carrier concentrations greater than equilibrium (at the depletion region edges).

3.) (2-points) True / [✓ False]: For reasons of speed, solar cells should have very small minority carrier diffusion lengths.

4.) (2-points) [✓ True] / False: A forward active biased transistor with zero base width modulation effect can be considered a near perfect current source.

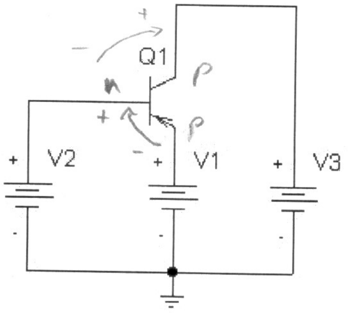
5.) (2-points) True / [✓ False]: Polycrystalline silicon emitters are typically used for modern BJTs because manufacturing problems prevent the use of crystalline silicon emitters.

6.) (2-points) True / [✓ False]: Breakdown should always be avoided because it destroys (or at least damages) the diode.

7.) (2-points) If a Clemson engineer wanted to bias this transistor into Inverse Active mode, which of the following is true?
- a. V3>V1 and V1>V3
- [✓ b.] V2>V1 and V2<V3
- c. V2>V3 and V1>V3
- d. V1<V2 and V3$\overset{\leq}{>}$V2
- e. None of the above.

$V_3 > V_2$

$V_2 > V_1$



8.) (2-points) Which of the following is NOT a use of a diode, ...
- a. Solar Cell
- b. Frequency doublers (through generation of harmonics)
- c. Full wave rectifier
- [✓ d.] High frequency amplifier
- e. Light emitting diode
- f. All of the above are uses of a diode

9.) (2-points) Regarding Large signal vs Small signal models of diodes and transistors, which of the following are NOT true:
- [✓ a.] Large signal models are linear models
- b. Mathematically, small signals are when voltages are less than the thermal voltage
- c. Ohms law applies for small signals
- d. The AC conductance is determined by finding the slope of current vs voltage curves at a DC operating point.
- [✓ e.] Small signal resistances are small when p-n junctions are reverse biased.
- f. This question is completely unfair!

10.) (2-points) The current flowing in the emitter-base junction of a forward active biased transistor ...

a. ...is mostly due to minority carriers drifting across the depletion region in response to the electric field

b. ...is mostly due to majority carriers drifting across the depletion region in response to the electric field

[✓ c.] ...is mostly due to majority carriers diffusing across the depletion region due to a lowered energy barrier

d. ...is mostly due to minority carriers diffusing across the depletion region due to a raised energy barrier

e. None of the above

12.) (20 points total in 2 parts)

A room temperature silicon p-n solar cell with an intrinsic concentration of 1×10^{10} cm^{-3} is measured in sunlight to have a voltage at it's terminals of 0.5 V.

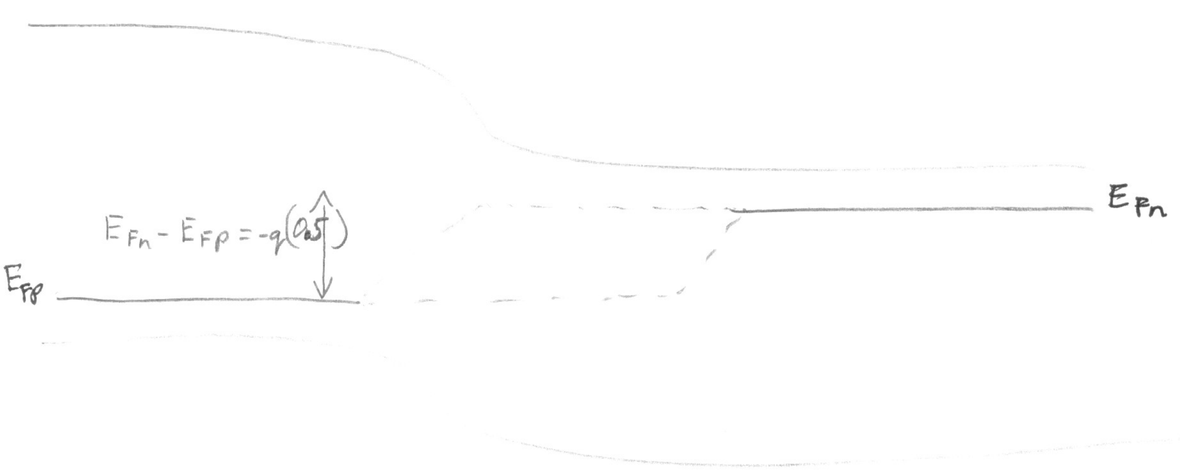
(a – 10 points) If the minority carrier concentration at the depletion region edge on the n-type side is 10^{15} cm^{-3}, what is the minority carrier concentration at the depletion region edge on the p-type side?

$$V_A = \frac{kT}{q} \ln\left(\frac{[n_p(x=-x_p)][p_n(x=x_n)]}{n_i^2}\right)$$

$$0.5\,V = 0.0259\,V \ln\left(\frac{n_p\,(10^{15})}{(10^{10})^2}\right)$$

$$\boxed{n_p = 2.42 \times 10^{13}\ \text{cm}^{-3}}$$

(b – 10 points) Sketch and label an energy band diagram of the solar cell labeling the magnitude of the quasi-fermi level splitting between the n-type and p-type sides of the solar cell.



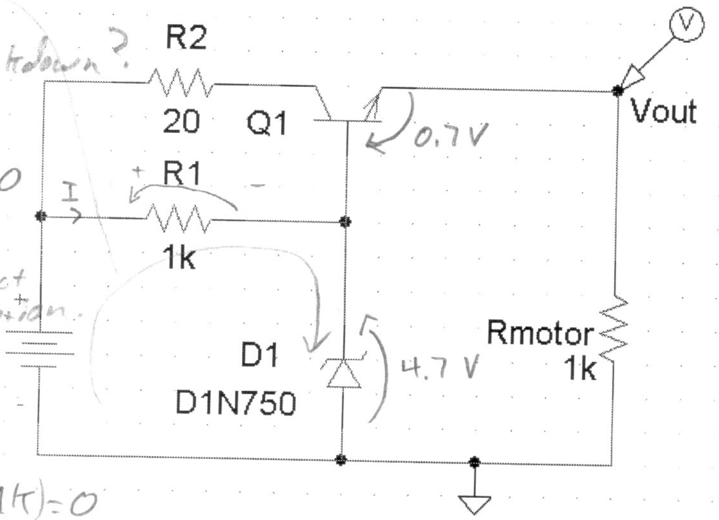
13) (20 – points)

For the following circuit, the battery, Vsource, is fully charged to an initial voltage of 24 V. Calculate the voltage, Vout, for this case (a fully charged battery) and for a battery that is "discharged" having only a voltage of 12 V. The 1N750 diode and Q1 has a forward turn on voltage of 0.7 V and a reverse breakdown voltage of 4.7 V. You can assume the transistor Q1 is always maintained in forward active mode. You know nothing about β, α, I_B, or I_C. (Yes you have been given enough information to solve the problem).

except I_B is very small compared to current flowing in the diode.

Is zener in Breakdown?

Assume So:



$24V - 4.7V - I(1k) = 0$

$I = 19.3mA$

positive ⇒ correct assumption.

Case 2:

$12V - 4.7V - I(1k) = 0$

$I = 7.3\ mA$

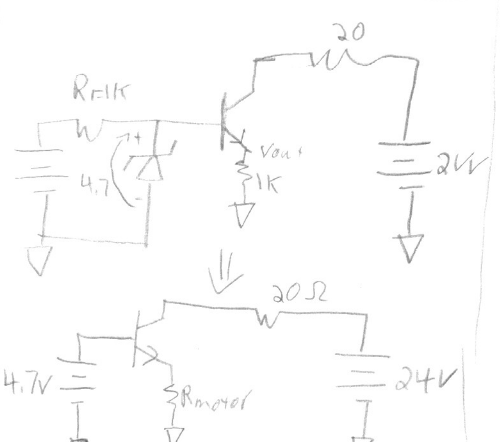
correct assumption!

$\therefore$ Vout = $4.7\ V - 0.7\ V = 4\ V$

for both cases.

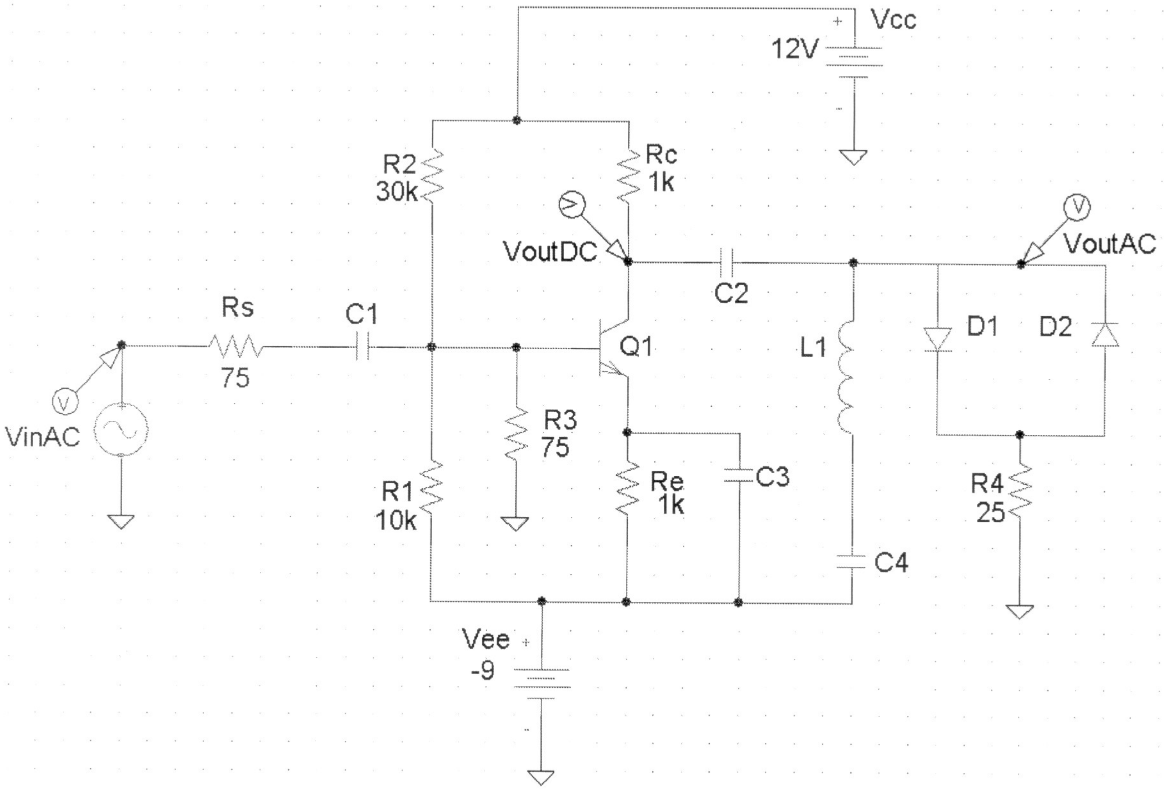
This is a voltage regulator circuit that maintains a constant output voltage as long as the input voltage is large enough to keep the transistor in forward active mode.

Alternate Solution
Thevenize Base



14). **Pulling all the concepts together for a useful purpose**:
(40-points total: DC solution = 12 points, conversion to small signal model = 12 points, AC solution = 12 points and 4 points for accuracy of the graph)

For the circuit below:
Diode: Io=Is=259 μA
Q1: $V_{\text{turn on}}$=0.7 V, Is=1.46e-14 A, β_{DC}=100, V_A=100V
VinAC = 1mV amplitude (i.e. 2mV peak to peak) at 1 KiloHertz



Given the above input voltage, VinAC, sketch and accurately label a plot the TWO output waveforms VoutAC and VoutDC on the graph paper provided on the next page. Assume the turn on voltages for all forward biased junctions are 0.7 V. You may assume all capacitors are very large values and are thus, AC shorts and any inductors are very large values, and thus AC opens. Additionally consider the circuit to be operated at low frequencies where you can neglect all small signal capacitances of transistors and diodes. Also, neglect all resistances that result from quasi-neutral regions. **For full Credit, be sure to check your assumptions on the mode of operation of the transistor and to clearly label the axes of your plot**.

Hint: Use the CVD/Beta analysis for the DC transistor solution. You will need to use the full diode model (i.e. not the CVD model) for the diodes. Then apply your results to convert to the small signal model for both the BJT and diodes (i.e. do not ignore the small signal model of the diode).

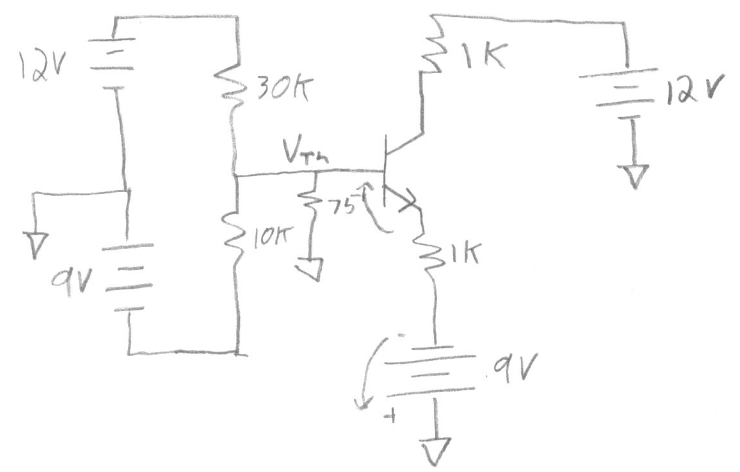
DC ~~15~~ 14
Conv. 9
AC 14
Graph 3 inverted, offset, labels

Extra work can be done here, but clearly indicate with problem you are solving.

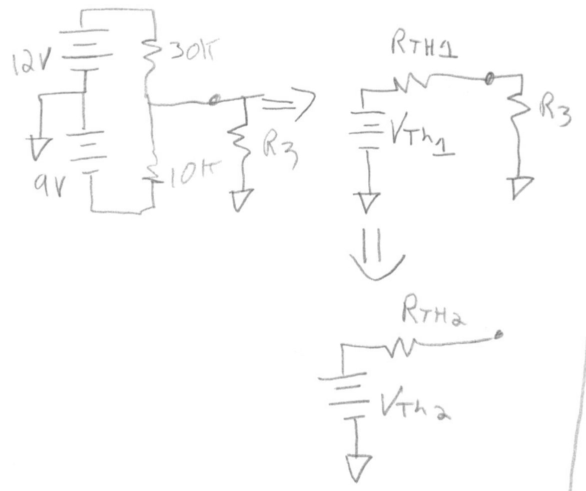
DC solution:

Diodes: $I_D = 0$

Transistor:



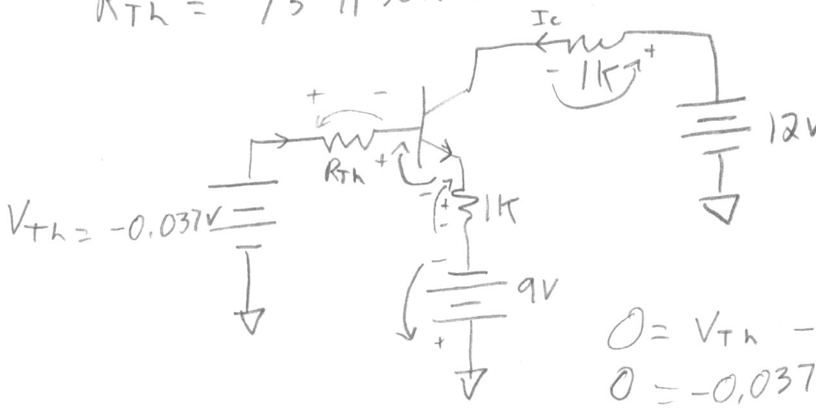
Alternative Approach to Thevenin BaseCircuit



Using Superposition in the base circuit:

$$V_{Th} = -9V \frac{(75 \| (30K))}{10K + (75 \| 30K)} + 12V \frac{(10K) \| 75}{(10K) \| 75 + 30K} = -0.037V$$

$$R_{Th} = 75 \| 30K \| 10K \approx 75\Omega$$



$$0 = V_{Th} - I_B R_{Th} - 0.7V - \underbrace{(100+1) I_B (1K)}_{I_E} + 9$$

$$0 = -0.037 - I_B (75 + 101(1K)) + 8.3V$$

$I_B = 81.7 \mu A$

$I_C = 100 I_B = 8.17 mA$

$I_E = 101 I_B = 8.26 mA$

$V_C = 12V - 1K I_C = 3.825 V$

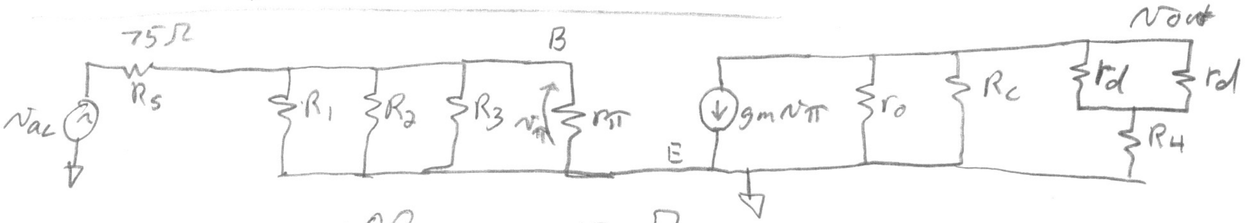
$V_E = -9V + 1K I_E = -0.74V$

$V = +0.7 + V_E = -0.04V$

FA verified.

Extra work can be done here, but clearly indicate with problem you are solving.

Small signal conversion:



$\beta = g_m r_\pi$

$$r_\pi = \frac{100}{g_m} = 317\ \Omega$$

$$g_m = \frac{I_C}{V_T} = \frac{8.17mA}{0.0259V} = 0.3154\ S$$

$$r_o = \frac{V_A + V_{CE}}{I_C} = \frac{100 + (3.825 + 0.74)}{8.17\ mA} = 12.7\ k\Omega$$

$$\frac{1}{r_d} = g_d = \frac{I_D + I_S}{V_T} = \frac{I_S}{V_T} = \frac{259mA}{0.0259} = 0.01 \Rightarrow r_d = 100\Omega$$

AC Solution:

$$v_\pi = v_{iac} \frac{R_1 \| R_2 \| R_3 \| r_\pi}{R_S + R_1 \| R_2 \| R_3 \| r_\pi}$$

$\Updownarrow$

$$\frac{v_\pi}{v_{iac}} = \frac{R_1 \| R_2 \| R_3 \| r_\pi}{R_S + R_1 \| R_2 \| R_3 \| r_\pi} = \frac{60.16}{75 + 60.16} = 0.445\ v/v$$

$$v_{out} = (-g_m v_\pi)(r_o \| R_c \| (R_4 + r_d \| r_d))$$

$\Updownarrow$

$$\frac{v_{out}}{v_\pi} = -g_m\ r_o \| R_c \| [R_4 + (r_d \| r_d)] = -0.3154\,(69.39)$$

$$= -21.88\ v/v$$

$$\frac{v_{out}}{v_{inac}} = \left(\frac{v_\pi}{v_{inac}}\right)\left(\frac{v_{out}}{v_\pi}\right) = (0.445)(-21.88) = -9.74\ v/v$$

$v_{out\,ac} = -9.74\ mV$ @ 1 kHz

$v_{out\,DC} = (-9.74\ mV$ @ 1 kHz$) + 3.825V\ DC$

$\uparrow$

$V_c\ DC$

Answer Page