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ECE 3040 Microelectronic Circuits

Exam 3

April 19, 2006

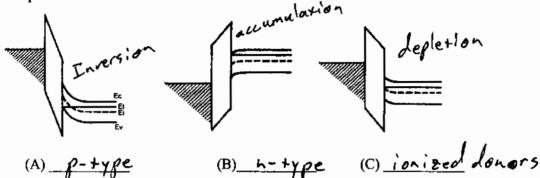
Dr. W. Alan Doolittle

Print your name clearly and largely: 50 (ution 5)
Instructions: DO NOT TAKE APART ANY PAGES OF THIS EXAM AND SHOW ALL WORK ON THE PROVIDED PAGES. Read all the problems carefully and thoroughly before you begin working. You are allowed to use 1 new sheet of notes (1 page front and back), your note sheet from the previous exams as well as a calculator. There are 100 total points in this exam. Observe the point value of each problem and allocate your time accordingly. SHOW ALL WORK AND CIRCLE YOUR FINAL ANSWER WITH THE PROPER UNITS INDICATED. Write legibly. If I cannot read it, it will be considered a wrong answer. Do all work on the paper provided. Turn in all scratch paper, even if it did not lead to an answer. Report any and all ethics violations to the instructor. Good luck!
Sign your name on <u>ONE</u> of the two following cases:
I DID NOT observe any ethical violations during this exam:
I observed an ethical violation during this exam:

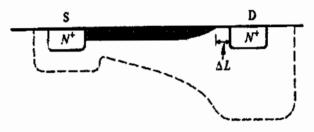
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First 26% Multiple Choice and True/False (Select the most correct answer)

 (3-points total) In each of the three cases shown below indicate whether the charge at the oxide/semiconductor interface is <u>predominately</u> p-type, n-type, ionized donors or ionized acceptors.



- 2.) (2-points) True False: The Gate-Source overlap capacitance (not the gate input capacitance) results in an increase in gain at high frequencies.
- ★3.) (Apoints) In the MOSFET transistor to the right, what is the voltage across the pinched off region?
 - a.) V6-VT
 - b.) V_{DS}
 - c.) V_{D-sat}
 - e.) Not enough information given to solve



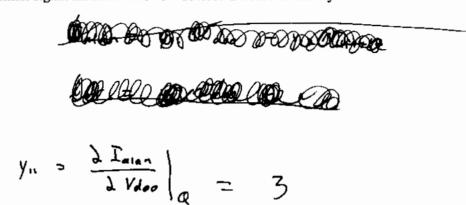
- 4.) (**points) True / False: A well designed transresistance amplifier should have a very high input resistance.
- 5.) (3-points) Which of the following is true of feedback circuits.
 - a) Feedback in a voltage amplifier can increase the input resistance
 - (b) Feedback in a voltage amplifier can decrease the output resistance
 - c) Feedback in a voltage amplifier can decrease the input resistance
 - d) Feedback in a voltage amplifier can increase the output resistance
 - e) Feedback in a voltage amplifier can increase the amplifier bandwidth if the open loop gain is larger than the closed loop gain
 - f) Feedback in a voltage amplifier can decrease the amplifier bandwidth if the open loop gain is larger than the closed loop gain
 - g) There are too many answers here for a measly 3 point problem

Short Answer

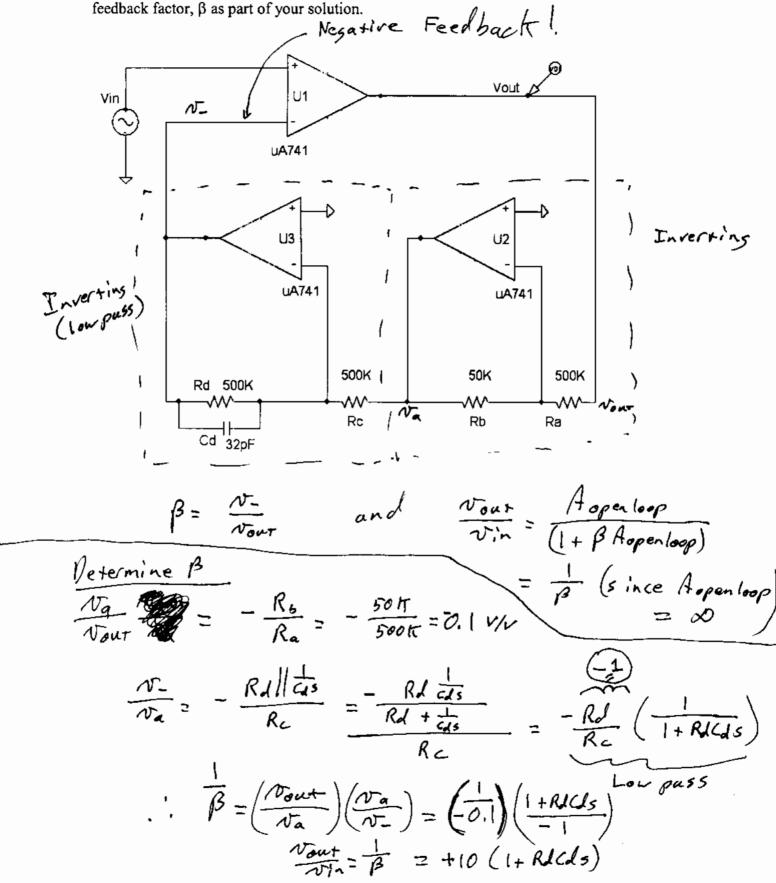
6.) (4-points) Your brilliant professor has developed an new device that has a DC IV characteristic of:

$$I_{alan} = 3 V_{doo} - 4 V_{little}$$
 and $I_{dr} = 5 V_{doo} - 6 V_{little}$

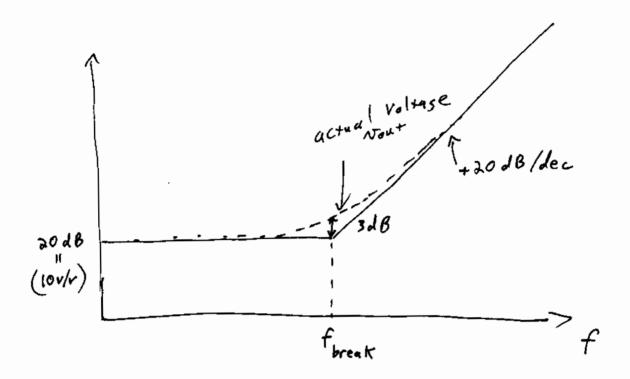
The bias voltages of the new device are V_{doo} =7 V and V_{little} = 8V. Determine all four y-parameters for the small signal model of this new device. Be sure to show your work.



7.) (20-points) Sketch and label all break frequencies, the voltage gain in flat regions in a Bode plot (gain in dB vs Log(frequency)). You may assume that the Op-Amps are ideal. To receive full credit the asymptotes and an estimate of the actual gain curve should BOTH be sketched on the same plot. Hint: you may find it helpful to determine the feedback factor. B as part of your solution

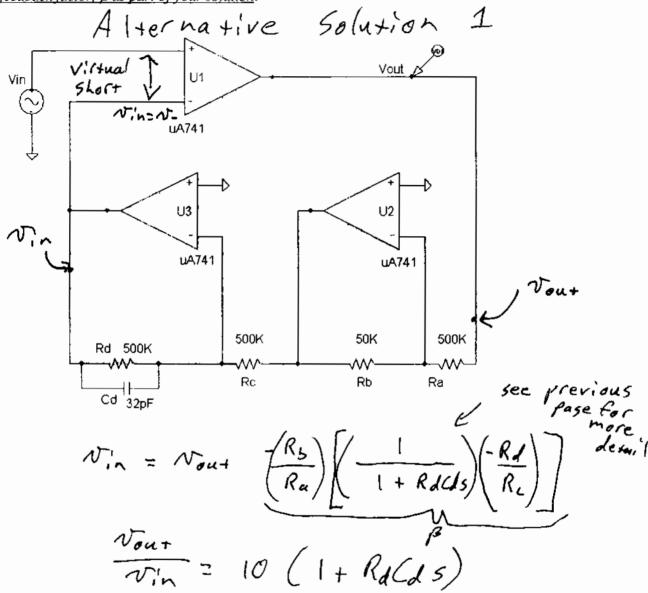


Extra work can be done here, but clearly indicate with problem you are solving.



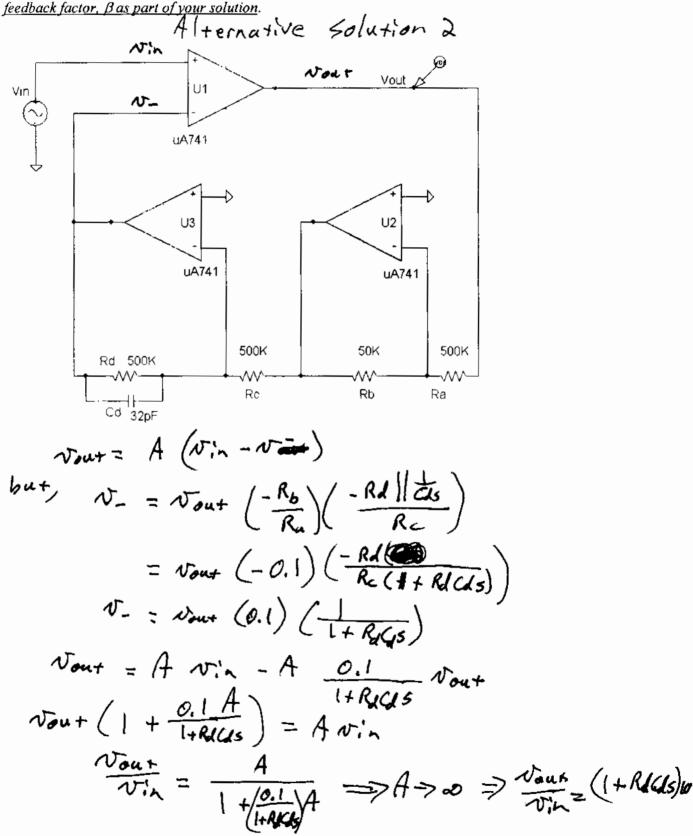
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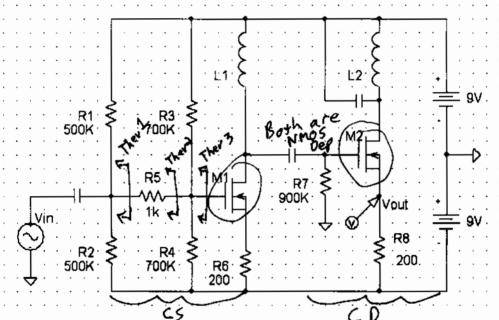
Note: The virtual short exists
be cause B is positive the theedback
overall is negative.

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Pulling all the concepts together for a useful purpose:

(50-points) Given the following circuit, (a) Identify the configuration of the two stages (common _____). (b) What is the AC voltage gain, V_{out}/V_{in}? You may assume all capacitors have infinite capacitance. You may assume all inductors have infinite inductance. Additionally consider the circuit to be operated at low frequencies where you can neglect all small signal capacitances. Grading will be based as such: part a=5 points, part b=18 points for DC solution (gate, source and drain voltages along with drain current), 9 points for the conversion to the small signal model and 18 points for small signal analysis.



Use the following parameters (note that V_T and λ vary with transistor type):

	-					_
1	For NMOS Dep	letion Transisto	-	15 20 08 11		
	$K_n'=20 \text{ uA/V}^2$	V_T = -4.0 V	$\lambda = 0.0 \text{ V}^{-1}$	Length (L)=10 um	Width (W)=10 um	1 = 30 m
	L					
For NMOS Enhancement Transistors:						
	$K_n' = 30 \text{ uA/V}^2$	$V_T = +0.75V$	$\lambda = 0.1 \text{ V}^{-1}$	Length (L)=10 um	Width (W)=10 um	
				~		

For PMOS Depletion Transistors: $K_n'=40 \text{ uA/V}^2$ $V_T=+3.0 \text{V}$ $\lambda=0.0 \text{ V}^{-1}$ Length (L)=10 um Width (W)=10 um

For PMOS Enhancement Transistors:

 $K_n'=50 \text{ uA/V}^2$ $V_T=-1.75 \text{V}$ $\lambda=0.1 \text{ V}^{-1}$ Length (L)=10 um Width (W)=10 um

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Extra work can be done here, but clearly indicate with problem you are solving.

Stage 1
                                                      Should notice that RI + R3 are symmetric with R2 + R4 => V6 M1 = 0 but assuming you
                                                          did not.
                                     Thevinen 1 (see draving):
                                                                                                                 V+h= OV R+h= 250K
                                         Therinen 2:
                                                                                                          OV = V+h= OV R+h= 251 K
                                                    OV = \frac{251 \text{K}}{\sqrt{\frac{5}{251 \text{K}} || 700 \text{K}}} = 5V
V+L = \frac{5}{251 \text{K}} \frac{251 \text{K}}{\sqrt{1700 \text{K}}} + \frac{251 \text{K}}{\sqrt{1700 \text{K}}} = 0
                                               Thevinen 3:
                                | 25|K||700K + 700N | R+h = 700K | 700K | 251K | R+h = 700K | 700
                                                                                                                                                                           VGS = 800 9 - IOS RG
                                                                                                                          => Ios = Ikn (9- Ios Ro 3- VTA)2
                                                                                                                                                                        = 1tn (13- Pos Rc)
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= 18 Fos Re + Fos (Re))

Extra work can be done here, but clearly indicate with problem you are solving.

$$I_{05} = \frac{1}{2} K_{n} \left(169 - 26 I_{05} R_{6} + I_{05}^{2} (R_{6})^{2} \right)$$

$$O = \frac{1}{2} K_{n} 169 \left(\frac{1}{2} K_{n} (26) R_{c} \right) I_{05} + \frac{1}{2} K_{n} R_{6}^{2} I_{05}^{2}$$

$$= 0.00169 - I_{05} \left(1.09200 \right) + 0.4 I_{05}^{2}$$

$$= \frac{1.052 \pm \sqrt{(1.052)^{2} - 4(0.4)(0.00169)}}{2(0.4)}$$

$$= \frac{1.052 \pm \sqrt{(1.0507)}}{0.8}$$

IDS = 2.6 Amps or 1.607mA

Check assumption: -9 + Ios R6 + Vos = 9v and V65 = 9- Ios R6 Note: Stage 2 OC solution is Identical !!

Nin \$ 350K 350K (Vgs. 9m/2) \$ R7 (Vs.2 \$)5m2 \$ R8 \$200

$$g_{n_1} = g_{n_2} = \frac{I_{05}}{\frac{V_{05}-VI}{2}} = \frac{1.627mA}{\frac{1}{2}(12.67)} = 0.000$$

Extra work can be done here, but clearly indicate with problem you are solving.

$$N_{th} = \frac{350 \text{K}}{755 \text{K}} N_{in} \qquad C_{th} = |K| |350 \text{K}$$

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$$\frac{Na = -gm Ngs_1 R7}{Ngs_1} = -gm R7$$

3)
$$\sqrt{v_{a}} = \sqrt{v_{552}} + R89m \sqrt{v_{952}}$$

$$\frac{\sqrt{v_{a}}}{\sqrt{v_{552}}} = (1 + 9mR8)$$