ECE 3040 Microelectronic Circuits

Exam 3

April 19, 2019

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Print your name clearly and largely: Solutions

Instructions:
DO NOT TAKE APART ANY PAGES OF THIS EXAM AND SHOW ALL WORK ON THE PROVIDED PAGES. Read all the problems carefully and thoroughly before you begin working. You are allowed to use 1 new sheet of notes (1 page front and back), your two note sheets from the previous exams as well as a calculator. There are 100 total points in this exam. Observe the point value of each problem and allocate your time accordingly. SHOW ALL WORK AND CIRCLE YOUR FINAL ANSWER WITH THE PROPER UNITS INDICATED. Write legibly. If I cannot read it, it will be considered a wrong answer. Do all work on the paper provided. Turn in all scratch paper, even if it did not lead to an answer. Report any and all ethics violations to the instructor. Good luck!

Sign your name on **ONE** of the two following cases:

I DID NOT observe any ethical violations during this exam:

I observed an ethical violation during this exam:

First 16% **Multiple Choice and True/False (Select the most correct answer)**

1.) (1-points total) True / False: MOSFETs can result in the same current-voltage characteristic from one manufacturing generation to another simply by maintaining the same channel width to length ratio.

2.) (2-points) True / False: Low input impedance is desirable for a current amplifier.

3.) (2-points) True / False: Common drain amplifiers have a gain slightly greater than 1.

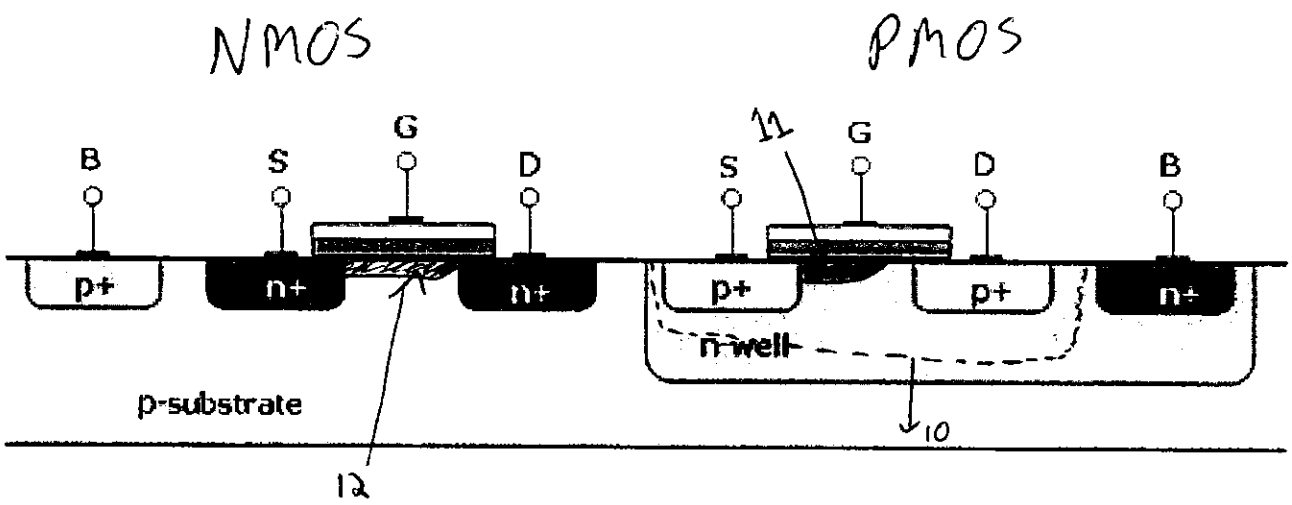
4.) (2-points) True / False: The channel length modulation parameter determines the slope of the I_{DS}-V_{DS} curve in saturation.

5.) (2-points) True / False: The larger the channel length modulation parameter the smaller the transistors small signal output resistance is.

6.) (2-points) True / False: The common drain amplifier has a180 degree phase shift.

7.) (2-points) True / False: MOSFET amplifiers can have very large bias resistors in the gate circuit because no current is drawn into the gate terminal.

8.) (2-points) True / False: Because the gate of a mosfet is a DC open circuit, no AC voltage signal can pass through the gate.



The above figure is for problems 9-12 and shows 2, 4-terminal enhancement mode mosfets including the body connections. When both NMOS and PMOS transistors are used in the same circuit, we call this CMOS (Complementary MOS). The Cross-section of two CMOS transistors is shown below with the Gate (G), Drain (D), Source (S) and Body (B) labeled.

9.) (5-points) Above each transistor, clearly label each transistor as NMOS and PMOS. ✓

10.)(5-points) On the drawing above, indicate with a clearly marked dashed line what the edge of the depletion region would look like if the PMOS transistor was biased into saturation. What condition is needed for the V_{GS} and V_{DS} relative to the threshold voltage for this to happen?

$V_{GS} \leq V_{TP}$ $\quad 0 \leq |V_{GS} - V_{TP}| \leq |V_{DS}|$

11.)(5-points) On the drawing above, indicate with a neatly shaded region, indicate what the channel would look like if the PMOS transistor was biased into saturation. What condition is needed for the V_{GS} and V_{DS} relative to the threshold voltage for this to happen?

same

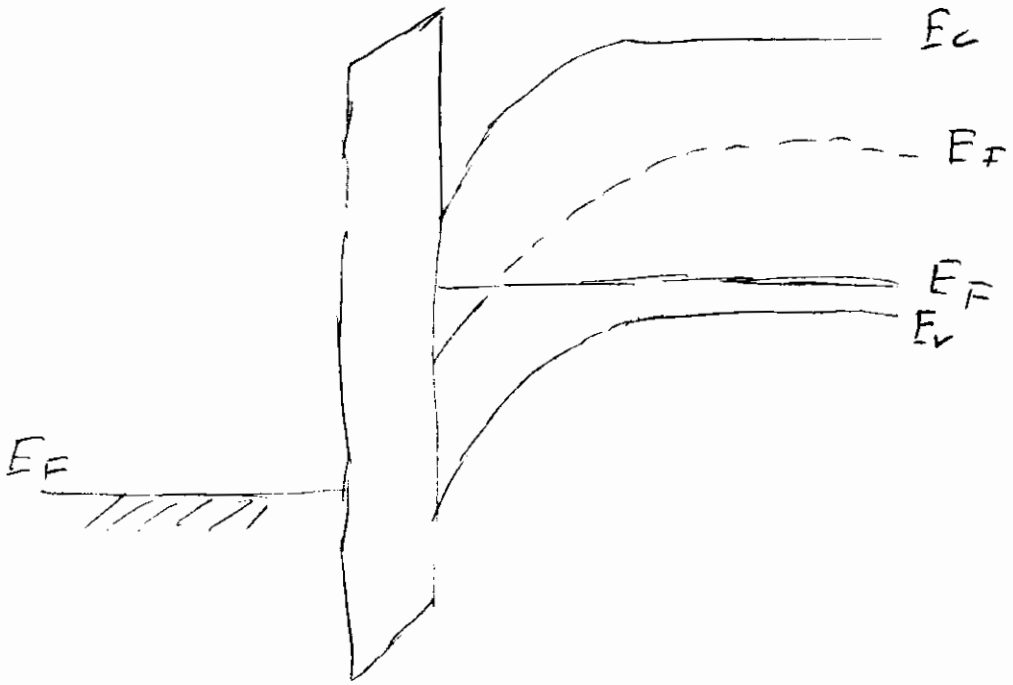
12.)(5-points) On the drawing above, indicate with a neatly shaded region, indicate what the channel would look like if the NMOS transistor was biased into the triode region. What condition is needed for the V_{GS} and V_{DS} relative to the threshold voltage for this to happen?

$V_{GS} \geq V_T$ $\quad (V_{GS} - V_{TN}) \geq V_{DS}$

P-type Substrate !!!

13.) (10 Points) Draw the energy band diagram of an NMOS CAPACITOR biased into inversion. For full credit be sure to show the fermi level positions, the intrinsic, conduction band and valence band energy and indicate what sign the gate voltage must have.

$V_G > 0 \Rightarrow$ ↓ Energy



14.) (2 Points) For the MOS capacitor that is incorporated into the MOSFET, what mode of MOS capacitor bias results in the MOSFET biased into linear mode ?

Inversion

15) (2 Points) If you wanted to switch a motor fully on (drive as much current as possible) what MOSFET bias mode would you use ?

Linear / Triode

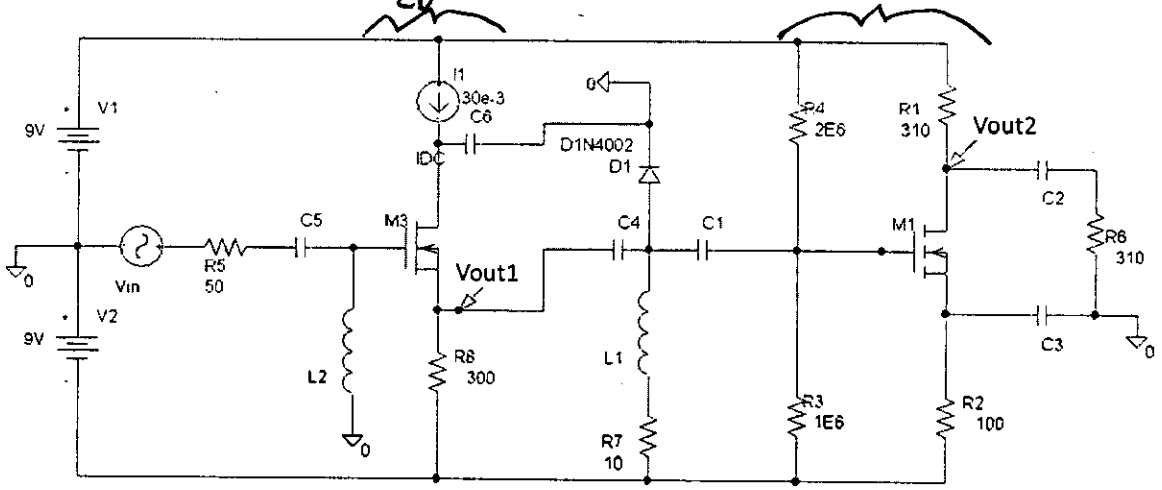
Several students were trying to memorize
NOTE: solutions instead of understanding the approach.

Pulling all the concepts together for a useful purpose: This problem reverses the CD/CS stages to avoid this possibility,

16) (50-points) Given the following amplifier circuit, (a) Identify the configuration of the each transistor stage (common ____). (b) What is the AC voltage gain, v_{out1}/v_{in} AND v_{out2}/v_{in}? You may assume all capacitors have infinite capacitance and all inductors have infinite inductance. Additionally consider the circuit to be operated at low frequencies where you can neglect all small signal parasitic components including capacitances.

Grading will be based as such: part a=5 points, part b=18 points for DC solution (gate, source and drain voltages along with drain currents), 12 points for the conversion to the small signal model and 15 points for small signal analysis. ***SHOW ALL WORK TO GET CREDIT!!!!! Do not just quote a result!!!!!***

CD CS



Use the following parameters (note that K, V_T and λ vary with transistor type):

$K_n = 2.5e\text{-}3\ A/V^2$ → For NMOS Depletion Transistors:
K_n'=250 uA/V^2 **V_T= -4.0V** **λ=0.1 V^{-1}** Length (L)=1 um Width (W)=10 um M3

$K_n = 50e\text{-}3\ A/V^2$ → For NMOS Enhancement Transistors:
K_n'=5 mA/V^2 **V_T= +2V** **λ=0.0 V^{-1}** Length (L)=0.18 um Width (W)=1.8 um M1

For PMOS Depletion Transistors:
K_p'=40 uA/V^2 **V_T= +3.0V** **λ=0.0 V^{-1}** Length (L)=20 um Width (W)=30 um

For PMOS Enhancement Transistors:
K_p'=50 uA/V^2 **V_T= -1.75V** **λ=0.1 V^{-1}** Length (L)=10 um Width (W)=10 um

Extra work can be done here, but clearly indicate with problem you are solving.

$I_D = -I_o$

Diode DC: Reverse biased!

$g_d = \frac{-I_o + I_o}{V_T} = 0$

Note: You do not need I_o!

$r_d = \infty$

DC M3: Assume Saturation

$I_{DS} = 0.03\,A$ $V_{G_3} = 0$ $V_{S_3} = 0.03(300) - 9V = 0\,V$

$V_{GS_3} = 0\,V$

$30mA = \frac{250\mu A/V^2}{2}\left(\frac{10}{1}\right)(0-(-4))^2(1 + 0.1V_{DS})$

$V_{DS} = 5V$

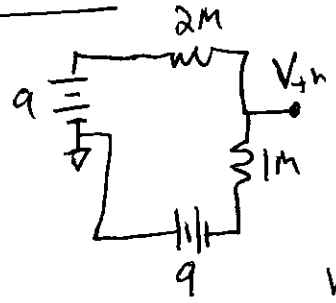
Check assumption: $V_{GS} - V_{Th} < V_{DS}$?

$V_{GS} = 0V > V_{Th} = -4V$ $0 - (-4)V < 5V$

$4V < 5V$ ✓

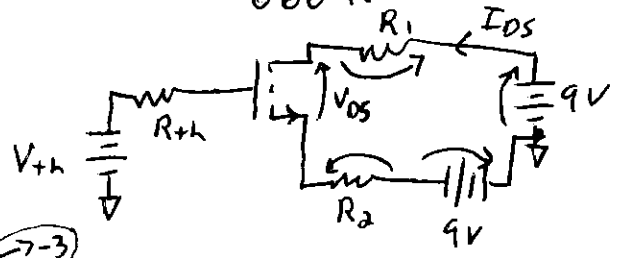
DC M1:

Gate Thevenin:



$V_{Th} = 9\left(\frac{1M}{2M+1M}\right) - 9\left(\frac{2M}{1M+2M}\right) = -3V$

$R_{Th} = 666.\overline{6}\,k\Omega$



1) V_{Th} (→ −3) $- V_{GS} - I_{DS}R_2 + 9V = 0$

$-V_{GS} - I_{DS}R_2 + 6V = 0$

2) $I_{DS} = \frac{k_n'}{2}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2(1 + \lambda V_{DS})$ ($\lambda V_{DS} \to 0$)

$= (0.025)(V_{GS}^2 - 4V_{GS} + 4)$

Putting 2) into 1): $-V_{GS} - 2.5(V_{GS}^2 - 4V_{GS} + 4) + 6 = 0$

$-2.5V_{GS}^2 + 9V_{GS} - 4 = 0$

$V_{GS} = 3.08V$ ✓ or $V_{GS} = 0.519$ ($V_{GS} < V_T$)

Check Assumption!

$I_{DS} = 29.2mA$

3) $9 - I_{DS}R_1 - V_{DS} - I_{DS}R_2 + 9V = 0 \Rightarrow V_{DS} = 6.04V$

$V_{GS} - V_T = 1.08V < V_{DS} = 6.04V$