ECE 3040
Dr. Doolittle

Homework 4

Unless otherwise specified, assume room temperature (T = 300 K).

1) Purpose: Understanding *p-n* junction band diagrams.
Consider a *p-n* junction with $N_A = 5x10^{14}$ cm^{-3} and $N_D = 10^{18}$ cm^{-3}. Draw the band diagram of this device under the following conditions. Solve for and label all energy levels where applicable (intrinsic Fermi levels, Fermi levels and quasi-Fermi levels) and the potential barrier in each diagram.
   a. At equilibrium (applied voltage V_A = 0 V).
   b. At V_A = 0.5 V.
   c. At V_A = -1.0 V.

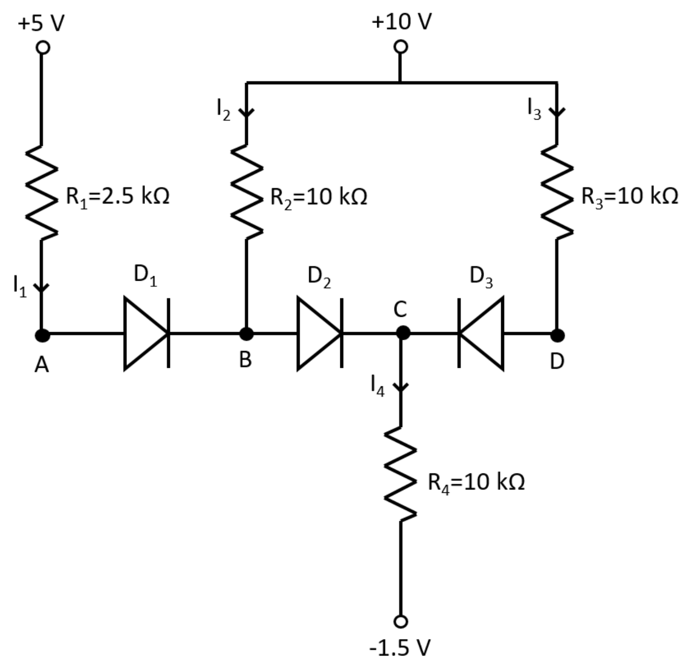
2) Purpose: Understanding *p-n* junction electrostatics.
Consider a silicon *p-n* junction with $N_A = 5x10^{17}$ cm^{-3} and $N_D = 10^{15}$ cm^{-3}. The relative permittivity of silicon is 11.8, and the permittivity of free space is 8.85x10^{-14} F/cm.
   a. Determine the magnitude of the depletion width on the *p*-side of the metallurgical junction (x_p), the depletion width on the *n*-side of the metallurgical junction (x_n), and the entire depletion width (W).
   b. Determine the maximum electric field in the depletion width, as well as the electric field at $x = -x_p/2$.
   c. Determine the built-in potential (V_{bi}), as well as the potential at $x = x_n/2$.

3) Purpose: Understanding junction capacitance.
Consider the *p-n* junction described in Question 2 above. Assume the cross-sectional area of the diode is 2x10^{-5} cm^2.
   a. Determine the equilibrium junction capacitance (C_{J0}).
   b. The diode is to be used in an LC circuit with a 10-nH inductor. If the desired oscillation frequency of the circuit is f = 5 GHz, at what voltage should the diode be biased?

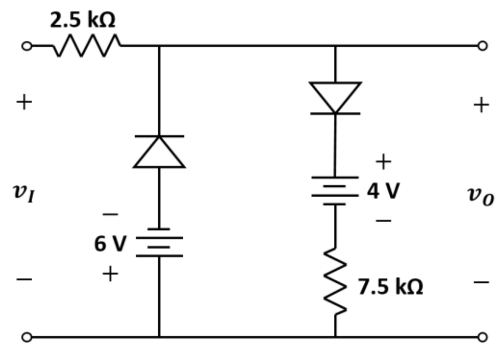
   Hint: The applied bias will be negative.

4) Purpose: Understanding *p-n* junction carrier concentrations.
Consider a silicon *p-n* junction with $N_A = 10^{16}$ cm^{-3} and $N_D = 10^{18}$ cm^{-3}. Let the mobility of electrons (μ_n) be 1300 cm^2/V-s and the mobility of holes (μ_p) be 400 cm^2/V-s. Let the minority carrier lifetime electrons and holes (τ_n and τ_p, respectively) both be 10^{-6} s. There is an applied voltage of 0.6 V.
   a. Solve for the excess electron concentrations on the *p*-side of the junction at 130 μm, 580 μm, and 1160 μm away from the depletion width edge (i.e. moving further into the *p*-side of the device).
   b. Solve for the excess hole concentration on the *n*-side of the junction at 70 μm and 1000 μm away from the depletion width edge.

5) Purpose: Understanding *p-n* junction *I-V* characteristics.
Consider the same diode described in Question 3. What is the reverse saturation current (I_0) of the diode? What is the current in the diode when the applied voltage (V_A) is 0.6 V?
6) Purpose: Understanding how diodes behave in circuits.
Find the Q-points for the three diodes in the circuit below. Use the constant voltage drop model for the diodes, with $V_{on} = 0.7$ V.
Hint: See Example 3.8 in Jaeger & Blalock.



7) Purpose: Using diodes to shape signal waveform.
Calculate output voltage, v_o, for the following circuit. Show the graphical representation of v_O for $-20\text{ V} \leq v_I \leq +20\text{ V}$, assuming ideal diodes. Show all work for full credit.



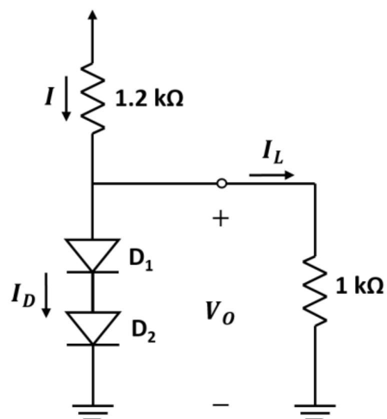
8) Purpose: Implementing diodes in practical circuits.

A particular design of a voltage regulator circuit is shown in the next page. Diodes D_1 and D_2 each has a voltage drop of 0.65 V at 1.4 mA.

(a) What regulator voltage output, V_O, when a 1 kΩ resistance is not connected (no load condition)?

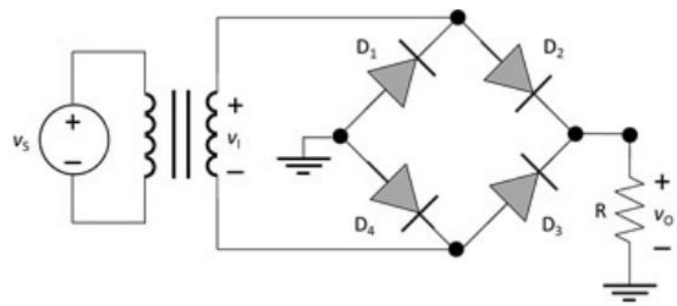
(b) What is V_O when a 1 kΩ resistance is added as load?

Hint: Use diode exponential model and iterative process to solve V_O.



9) Purpose: Investigating the full-wave bridge rectifier.
Consider the following full wave rectifier circuit. The supply voltage from wall-point is stepped down using a transformer and connected to the input of the full wave rectifier. Here, the input voltage (v_I) to the rectifier is a ***sine-wave*** with amplitude of 10 V. Assume that diodes can be represented by the constant-voltage-drop model with $V_D = 0.6$ V.

(a) Show the current path for the positive and negative half-cycle of v_I. Also, sketch and clearly label the transfer characteristic (v_O vs. v_I) and the time response (same plot showing v_O vs. t and v_I vs. t) of the circuit shown.



(b) The output resistance, R is now replaced with a Zener diode, Z. Assume that the Zener voltage is 6.5 V and that r_z is negligibly small. How does the transfer characteristic and time response change? Generate both plots for the modified circuit.