Lecture 15

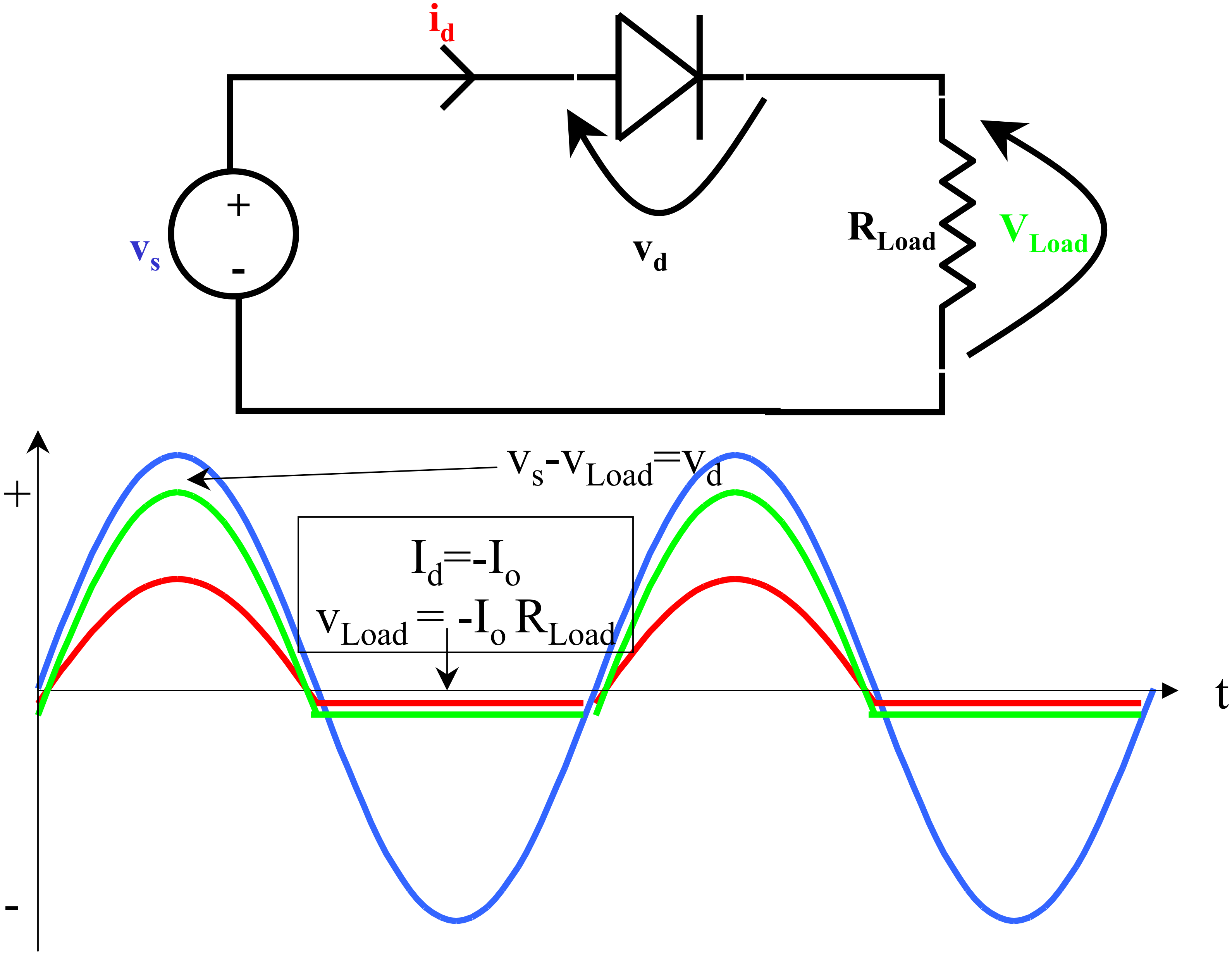
P-N Junction Diodes: Part 5

Large signal (complete model) and small signal (limited use) models of a Diode

Reading:

Jaeger 3.4-3.14, 13.4, Notes

Diode Applications: 1/2 Wave Rectifier

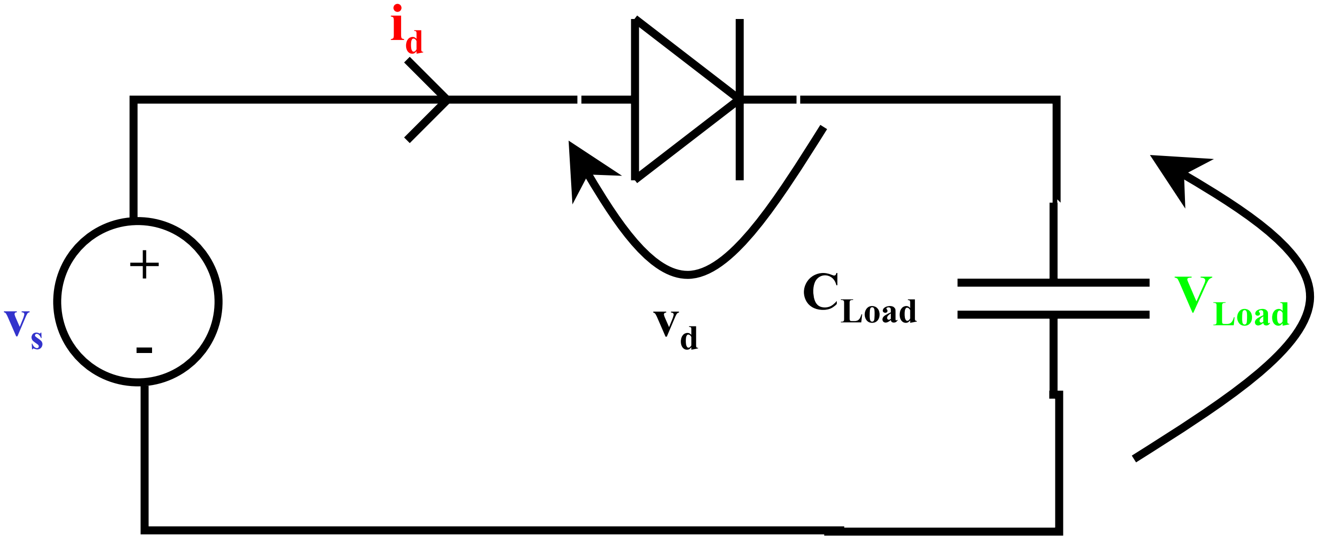


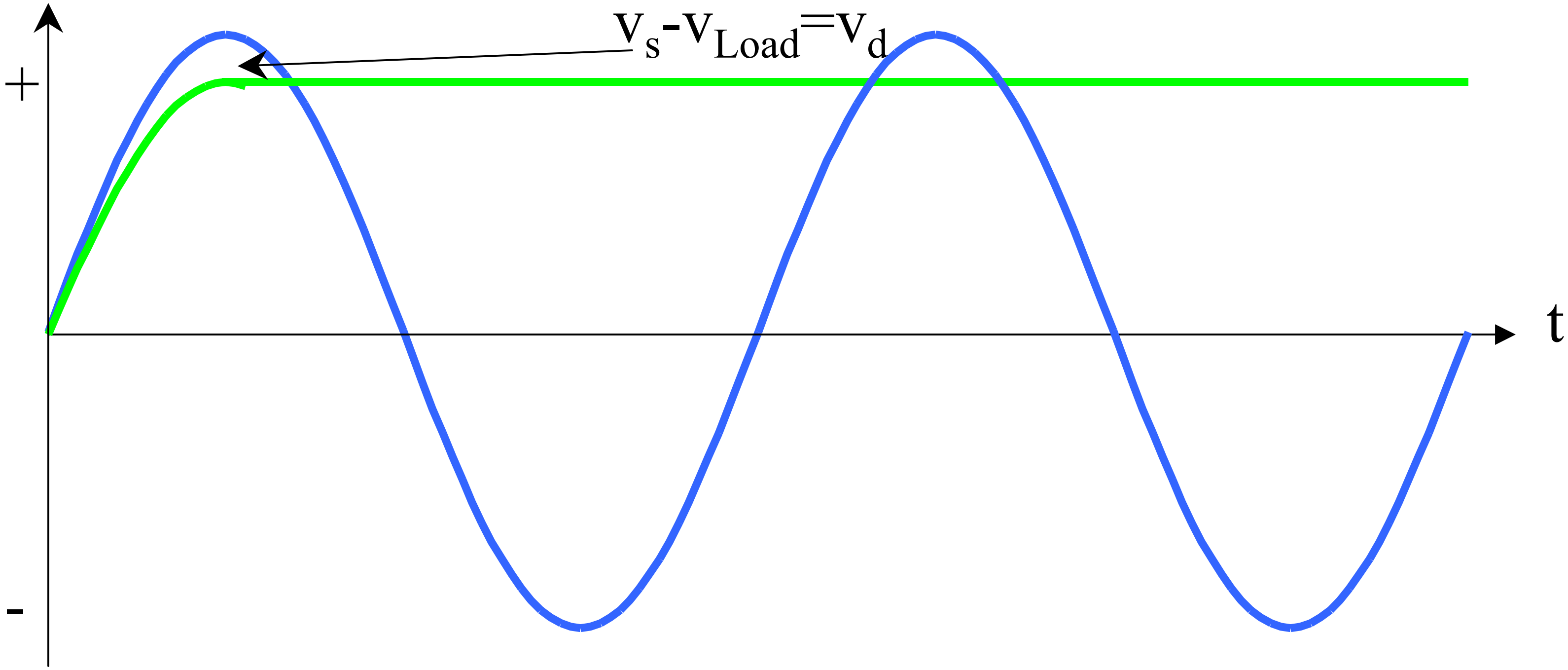
$v_s - v_{Load} = v_d$

$I_d = -I_o$

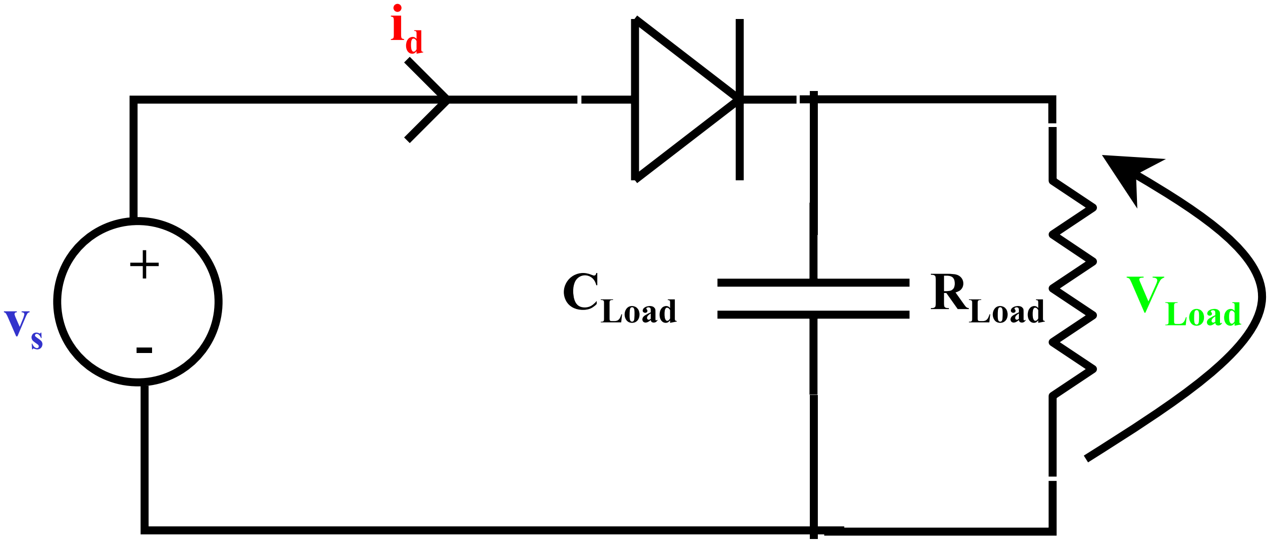
$v_{Load} = -I_o R_{Load}$

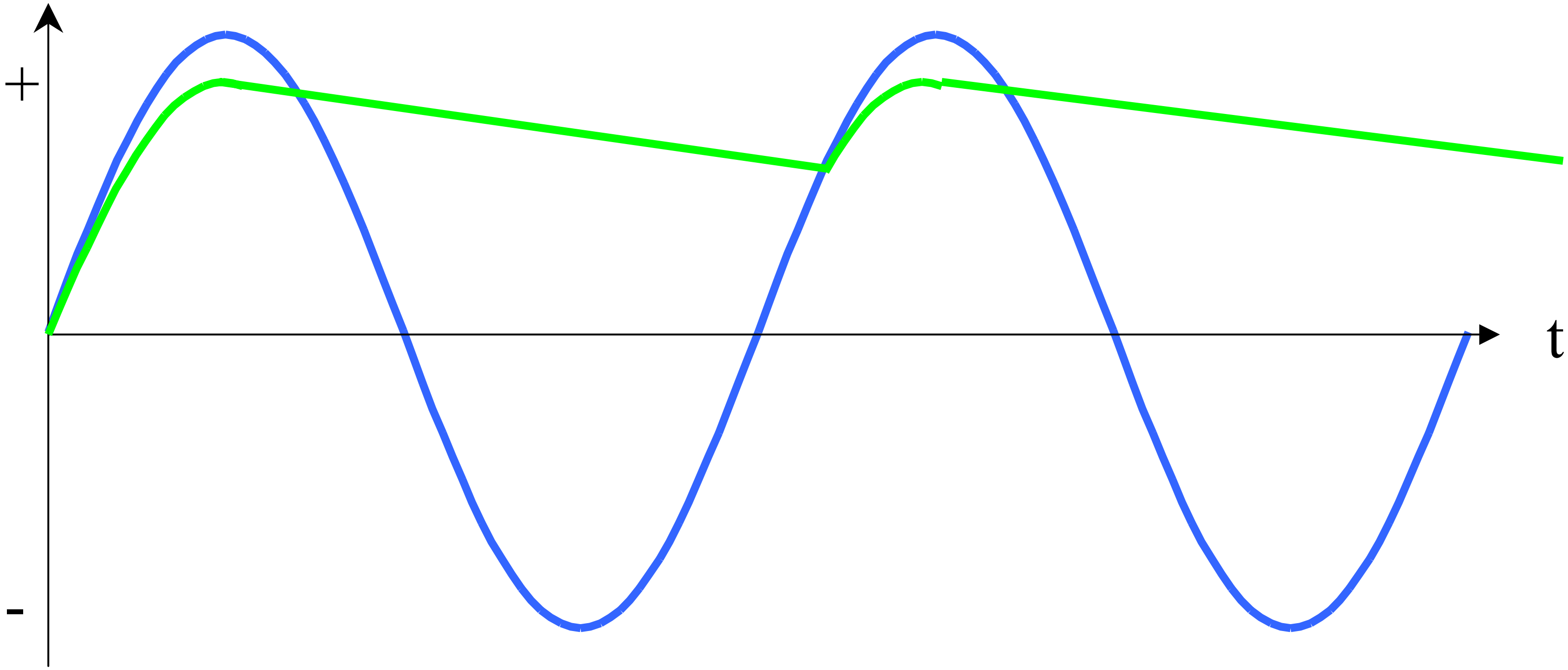
Diode Applications: Peak Detector



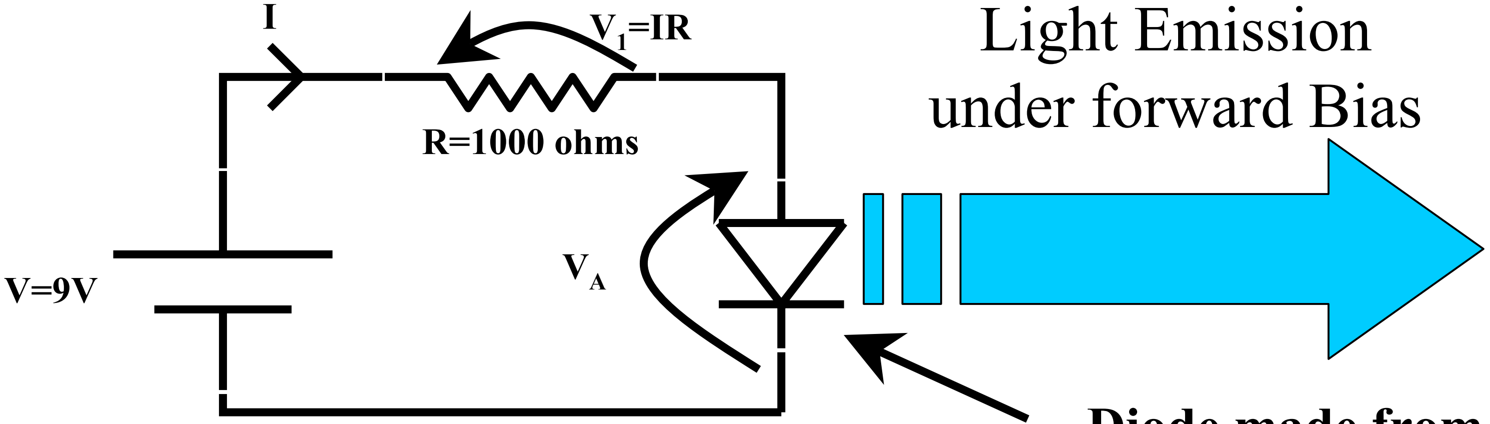


Diode Applications: 1/2 Wave Rectifier with an RC Load





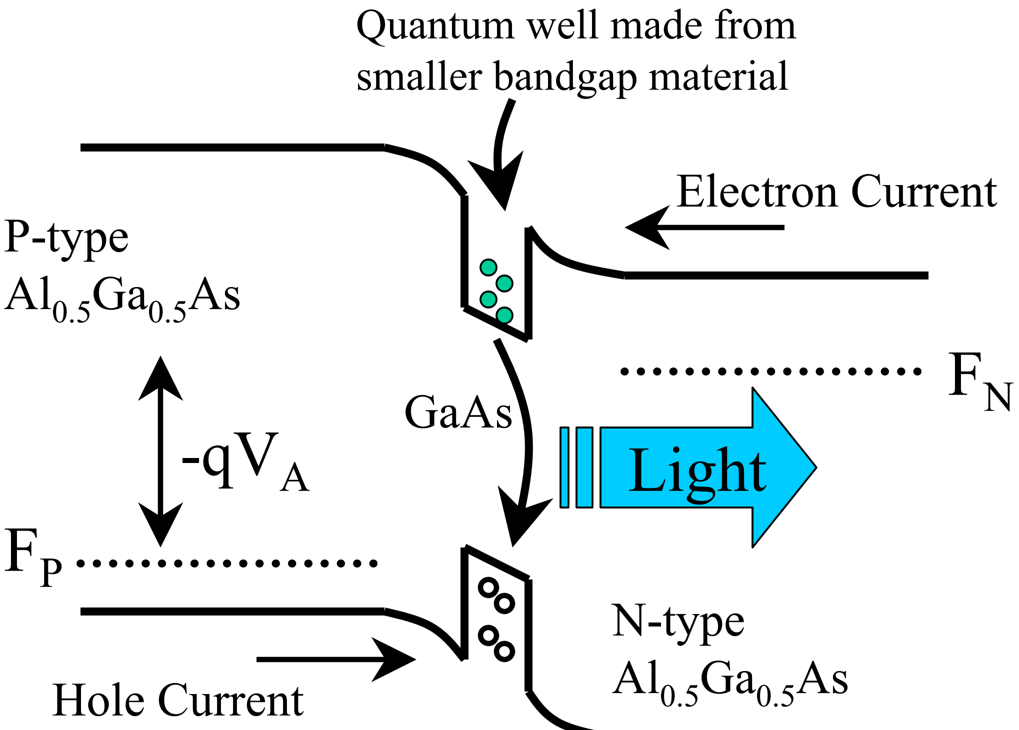
Diode Applications: LED or a Laser Diode



Light Emission under forward Bias

Diode made from a direct bandgap semiconductor.

Note: These devices may not be a simple p-n type diode, but behave electrically identical to a p-n junction diode.



Majority Carriers that are injected to the oppposite side of the diode under forward bias become minority carriers and recombine. In a direct bandgap material, this recombination can result in the creation of photons. In a real device, special areas are used to trap electrons and holes to increase the rate at which they recombine. These areas are called quantum wells.

Models used for analysis of Diode Circuits

Mathematical Model (previously developed)

Graphical Analysis

Ideal diode Model

- Treat the diode as an ideal switch

Constant Voltage Drop Model

- Treat as an ideal switch plus a battery

Large signal Model (model used by SPICE transient analysis)

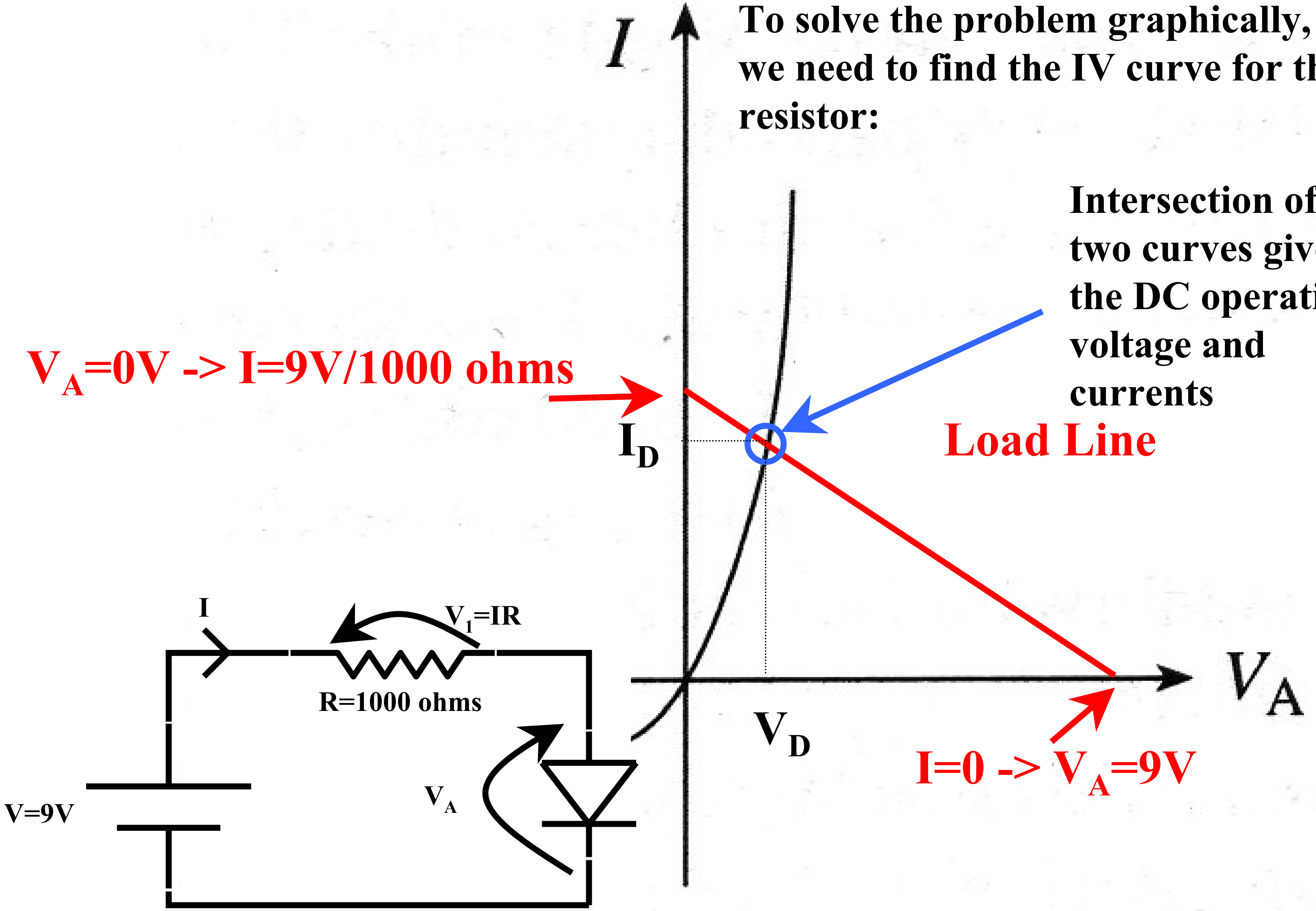
- multi-components
- generally applicable

Small Signal Model (model used by SPICE AC analysis)

- easier math
- valid only for limited conditions-ie small signals

Diode Circuits: Graphical Solution

To solve the problem graphically, we need to find the IV curve for the resistor:



V_A=0V -> I=9V/1000 ohms

Intersection of the two curves gives the DC operational voltage and currents

Load Line

I=0 -> V_A=9V

Diode Circuits: Other Models

Besides the direct mathematical solution and the graphical solution, we can use 2 other models to approximate circuit solutions:

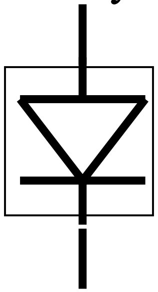
1.) Ideal Diode Model:

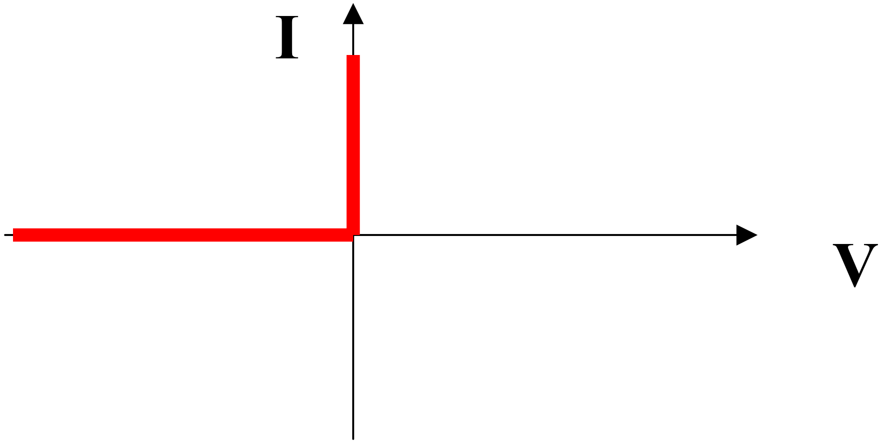
a) The voltage across the diode is zero for forward bias.

b) The slope of the current voltage curve is infinite for forward bias.

c) The current across the diode is zero for reverse bias.

Circuit Symbol





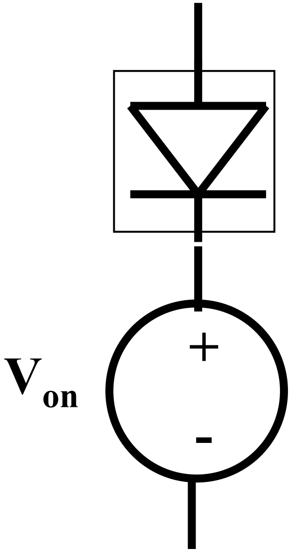
Diode Circuits: Other Models

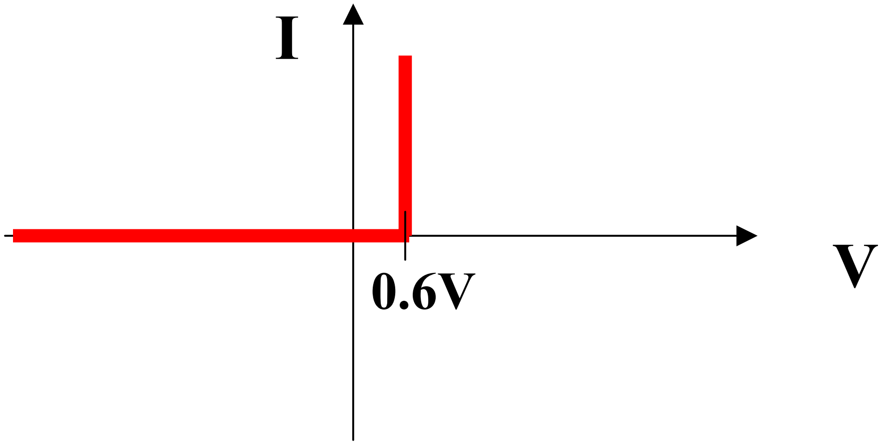
2.) Constant Voltage Drop (CVD) Model:

a) The voltage across the diode is a non-zero value for forward bias. Normally this is taken as 0.6 or 0.7 volts.

b) The slope of the current voltage curve is infinite for forward bias.

c) The current across the diode is zero for reverse bias.





Concept of the Small- Signal Model

- Superposition principle allows us to separate DC and AC analysis of circuits containing active devices (like diodes, transistors, amplifiers etc...).
- We assume the AC signals are small enough so that the circuit behaves linearly and can be analyzed by replacing "non-linear" components by "Linear Elements" such as resistors etc...
- DC analysis is first performed to determine the bias point which will determine some of the parameters used in the "AC-small signal analysis".
- Consider a two terminal device (like a pn diode) at a given DC *operating point* (or "Q- point").

Let: V_D = DC voltage applied to the diode
I_D = DC current produced by the diode

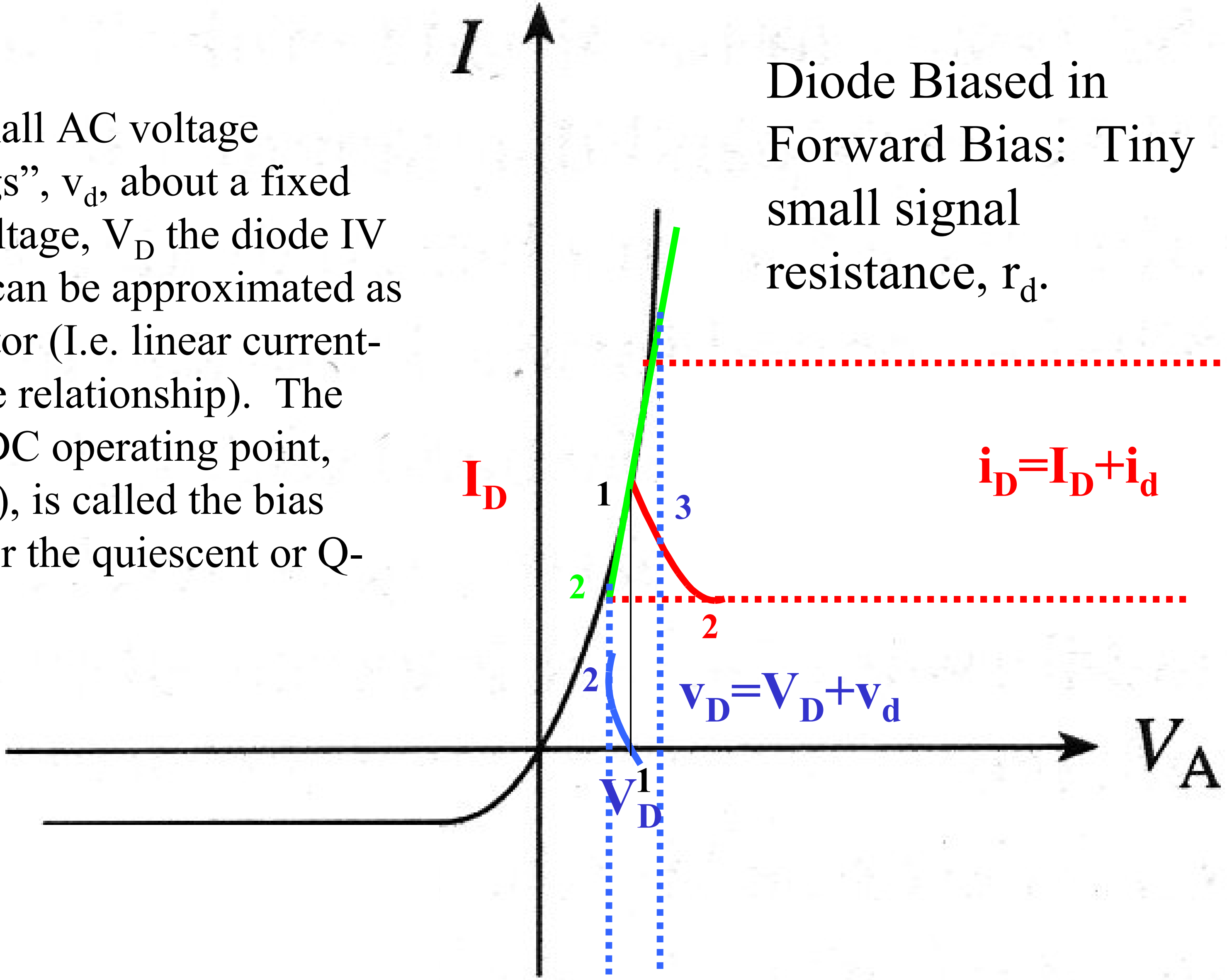
Total current or voltage = DC part + AC part:

$$v_D = V_D + v_d \qquad\qquad i_D = I_D + i_d$$

Note: (1) all caps = DC; (2) all lower case = AC; (3) lower case symbol with upper case subscript = total voltage or current

Small Signal Analysis of Diodes

For small AC voltage "swings", v_d, about a fixed DC voltage, V_D the diode IV curve can be approximated as a resistor (I.e. linear current-voltage relationship). The fixed DC operating point, (V_D-I_D), is called the bias point or the quiescent or Q-point.



Diode Biased in Forward Bias: Tiny small signal resistance, r_d.

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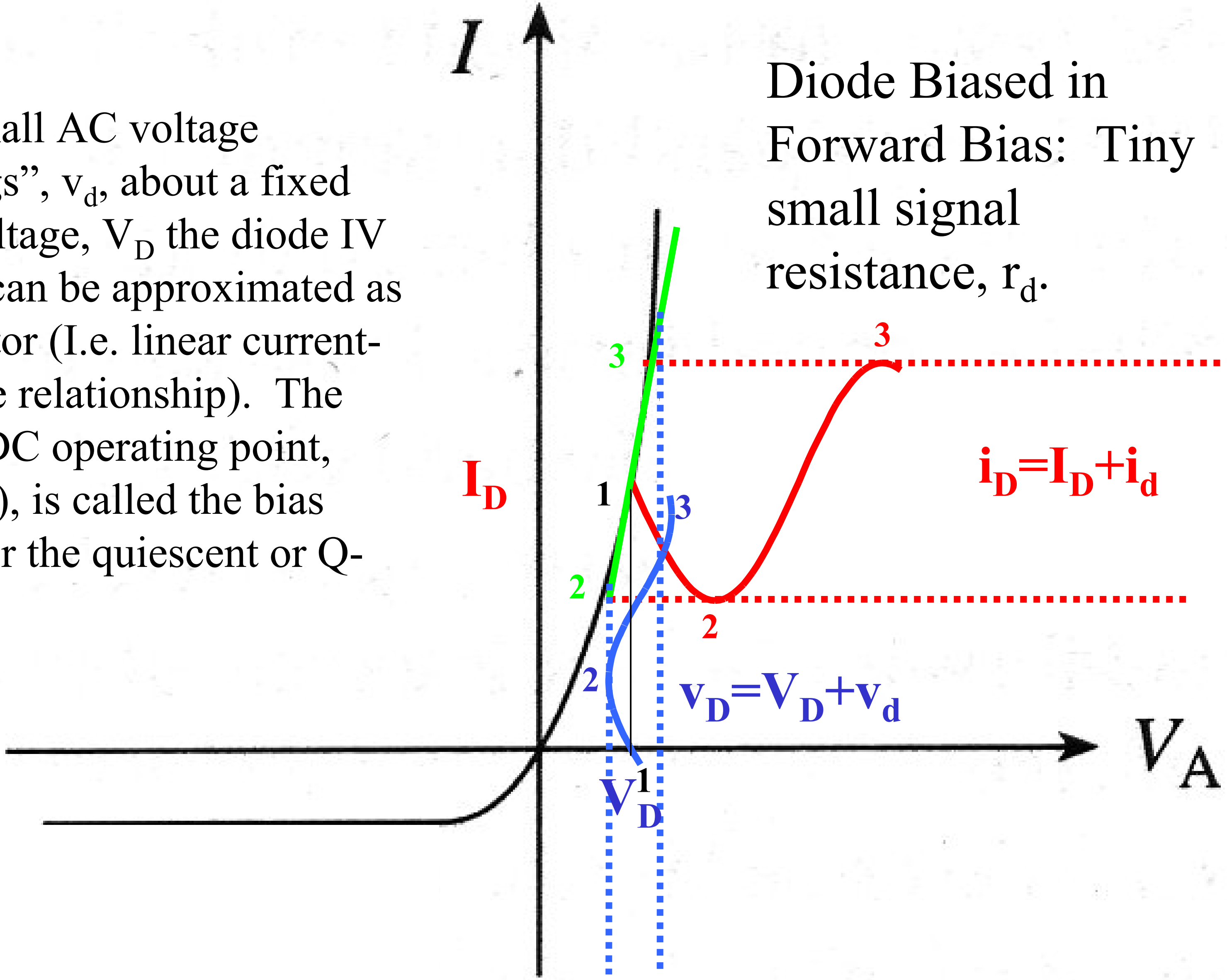

Diode Biased in Forward Bias: Tiny small signal resistance, r_d.

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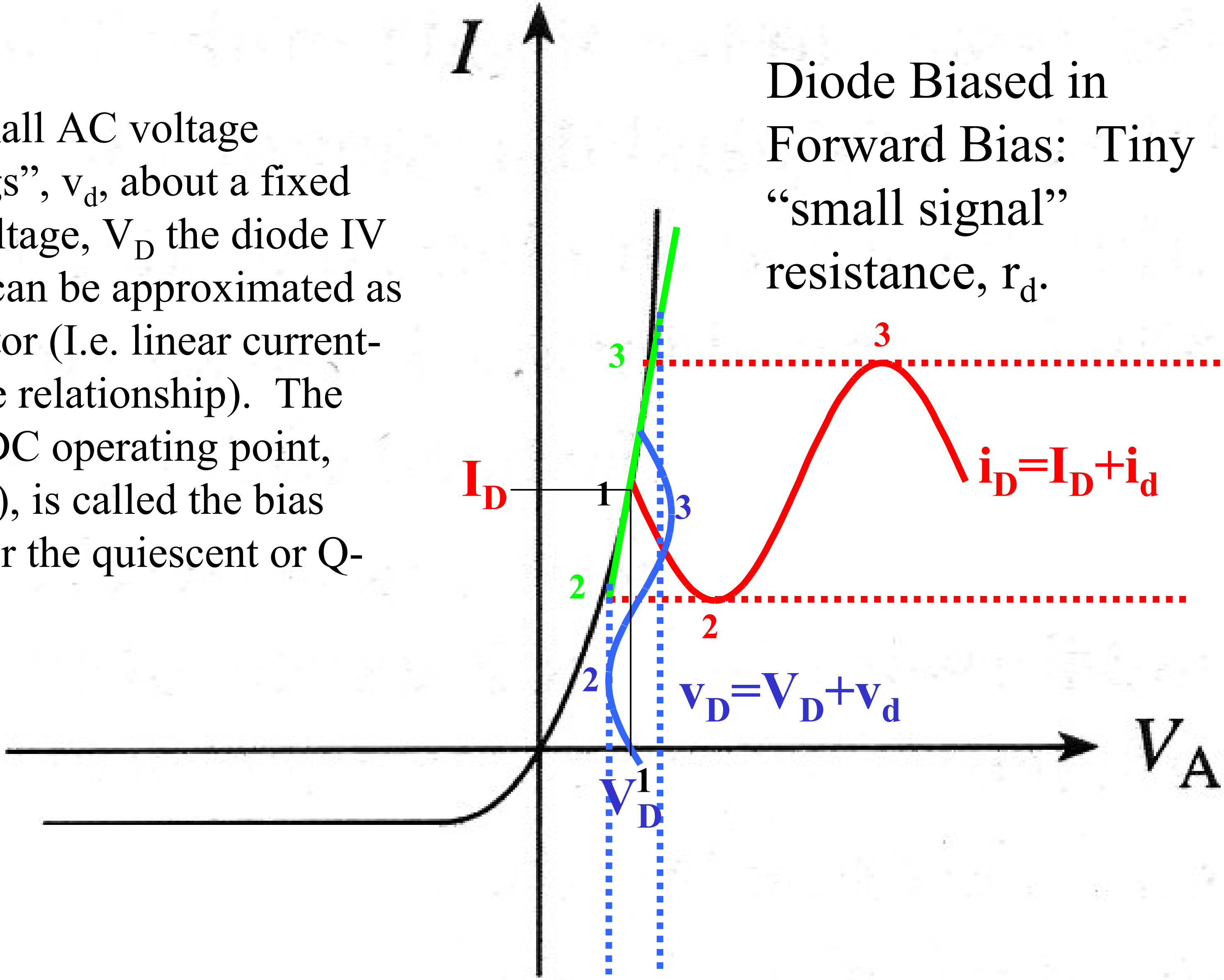
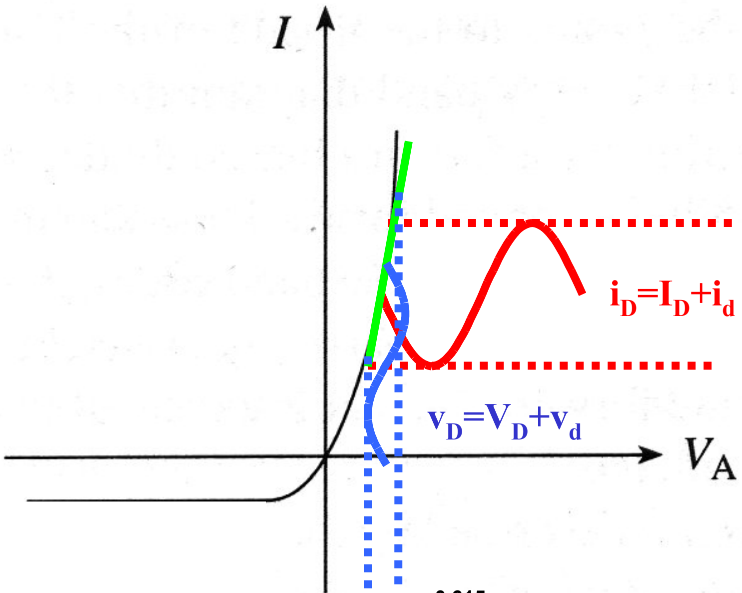
Diode Biased in Forward Bias: Tiny "small signal" resistance, r_d.



Small vs Large Signal Concept For Diodes



Consider the small signal case where

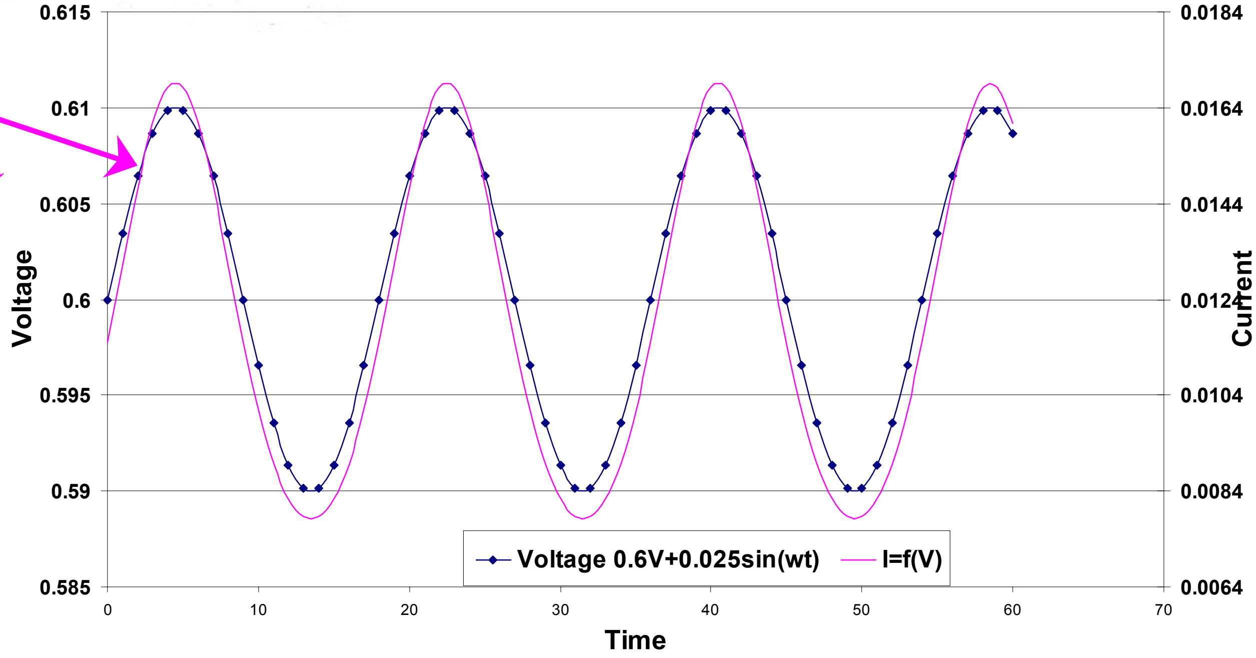
$$v_D(t) = 0.6 + 0.025\sin(wt) \text{ then,}$$

$$i_D(t) = 1e\text{-}12\left(e^{v_D(t)/0.0259} - 1\right)$$

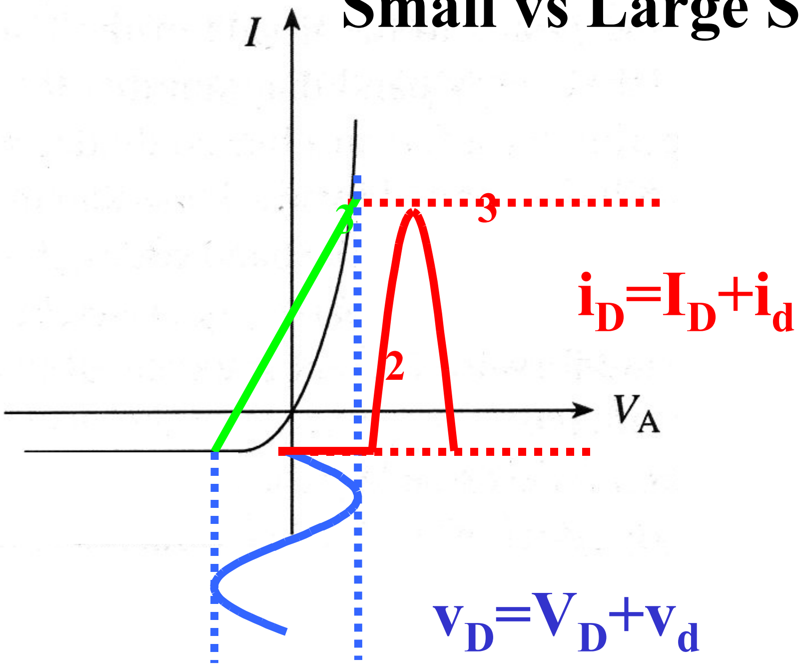
$$\Rightarrow i_d(t) \approx \frac{1}{r_d} v_d(t) \quad \text{but} \quad i_D(t) \neq \frac{1}{r_d} v_D(t)$$

Both Voltage and Current are (approximately) a sine wave.

Some distortion is observed because in this example we have exceeded the mathematical limits valid for small signal analysis (0.025 is not << kT/q). In most cases, this is tolerable.



Small vs Large Signal Concept For Diodes



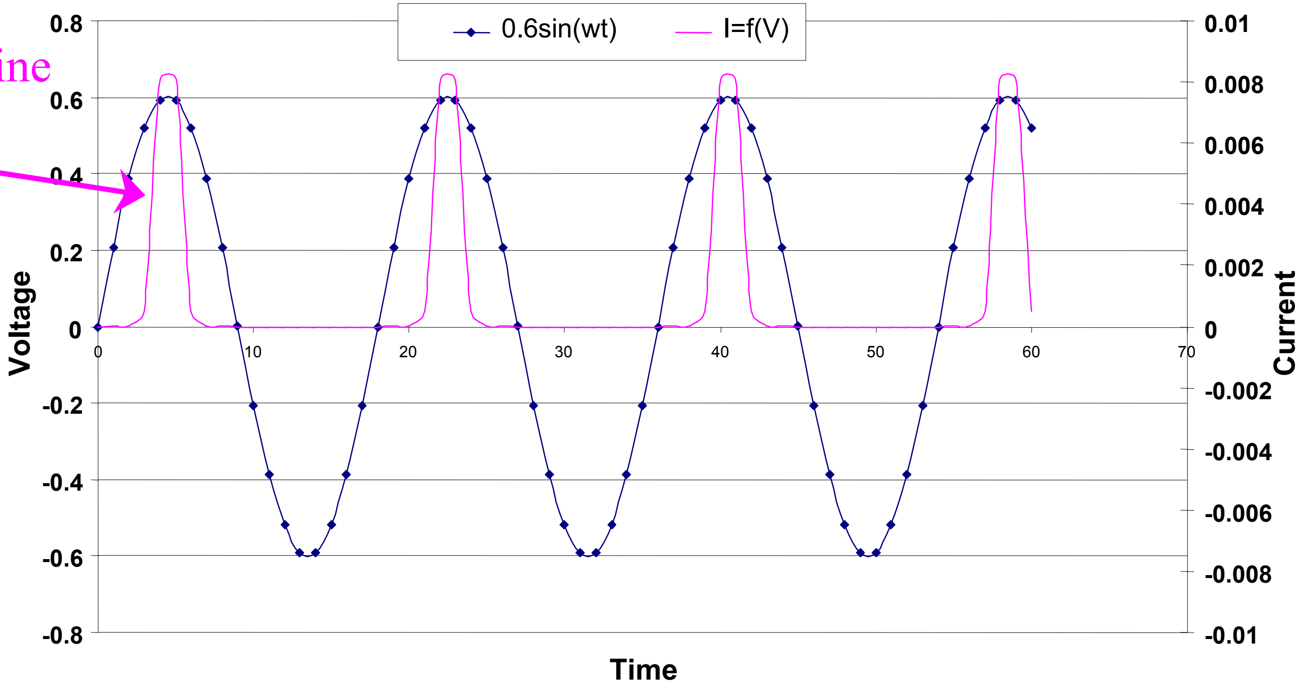
Consider the Large Signal case where

$$v_D(t) = 0.6\sin(wt) \text{ then,}$$

$$i_D(t) = 1e-12(e^{v_D(t)/0.0259} - 1)$$

$$\Rightarrow i_D(t) \neq \frac{1}{r_d} v_D(t)$$

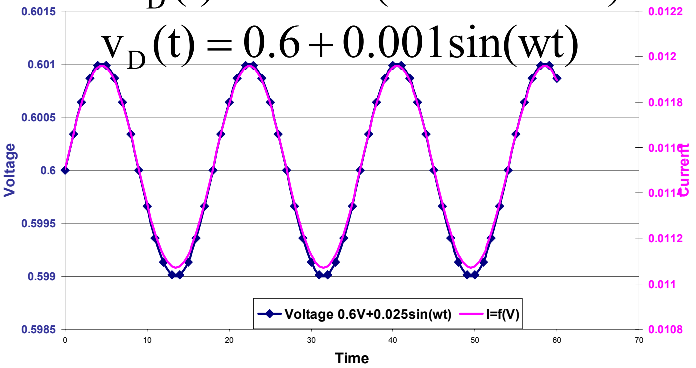
Voltage is a sine wave but the current is "distorted"



The transition from valid small signal limits to Large Signal conditions is a matter of what is acceptable for your requirements

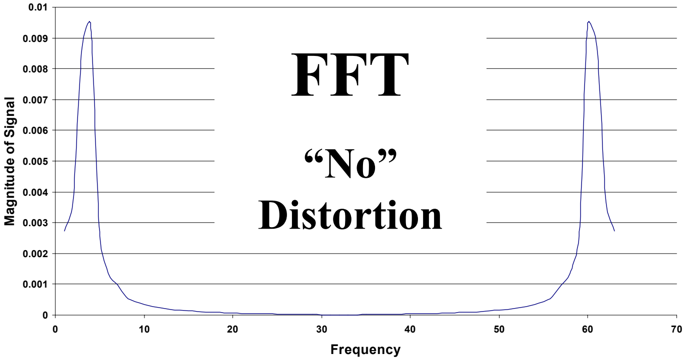
$$i_D(t) = 1e\text{-}12(e^{v_D(t)/0.0259} - 1)$$

$$v_D(t) = 0.6 + 0.001\sin(wt)$$

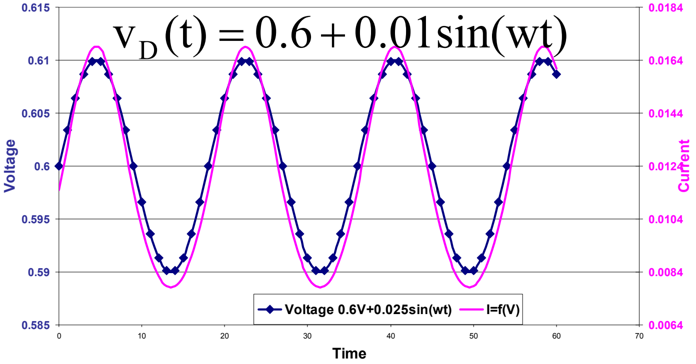


FFT

“No” Distortion



$$v_D(t) = 0.6 + 0.01\sin(wt)$$



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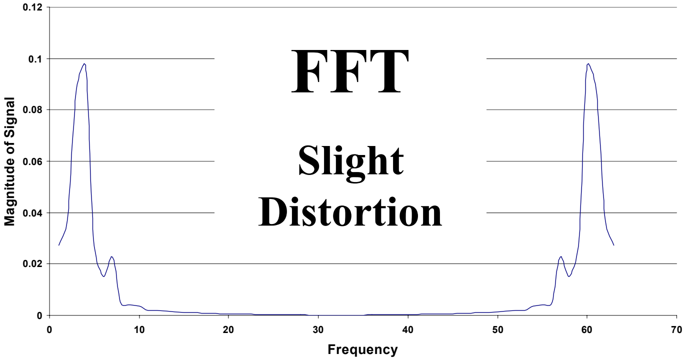
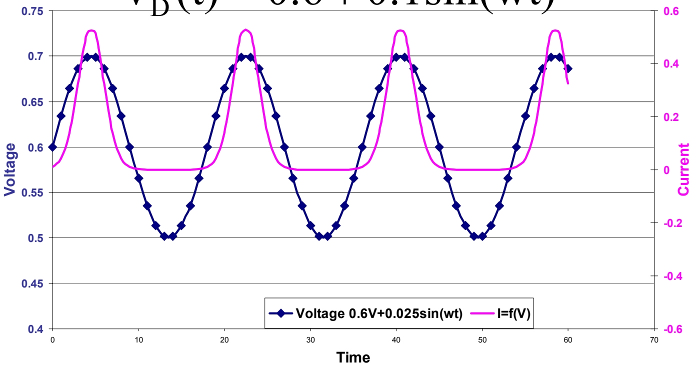
Slight Distortion

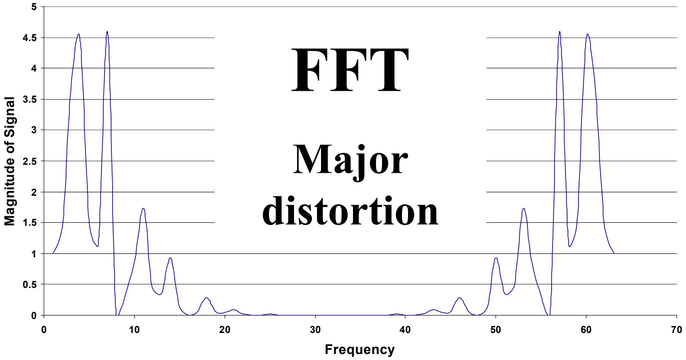


$$v_D(t) = 0.6 + 0.1\sin(wt)$$



FFT

Major distortion



Small Signal Analysis of Diodes

$$g_d \equiv small\ signal\ conduc\tan ce\ of\ the\ diode$$

$$r_d \equiv small\ signal\ resis\tan ce\ of\ the\ diode,\quad r_d = \frac{1}{g_d}$$

$$g_d = \left.\frac{\partial i_D}{\partial v_D}\right|_{Bias\ Po\text{int}\ or\ "Quiscient"\ or\ "Q-po\text{int}"}$$

$$= \left.\frac{\partial\left\{I_S\left(e^{v_D/V_T}-1\right)\right\}}{\partial v_D}\right|_{Q-po\text{int}}$$

$$= \left.\frac{I_S}{V_T}e^{v_D/V_T}\right|_{Q-po\text{int}} = \frac{I_S}{V_T}e^{V_D/V_T}e^{v_d/V_T}$$

$$Assu\min g\ small\ signals,\quad v_d \langle\langle V_T,\quad e^{v_d/V_T} \rightarrow 1\quad and$$

$$= \frac{I_S e^{V_D/V_T}}{V_T} = \frac{I_S e^{V_D/V_T} - I_S + I_S}{V_T}$$

$$\boxed{g_d = \frac{I_D + I_S}{V_T}}$$

Small Signal Analysis of Diodes

$$\mathrm{I_D} = I_o\left(e^{V_A/V_T} - 1\right) \quad where\ V_T = \frac{kT}{q}$$

$$i_D = I_D + g_d v_d$$

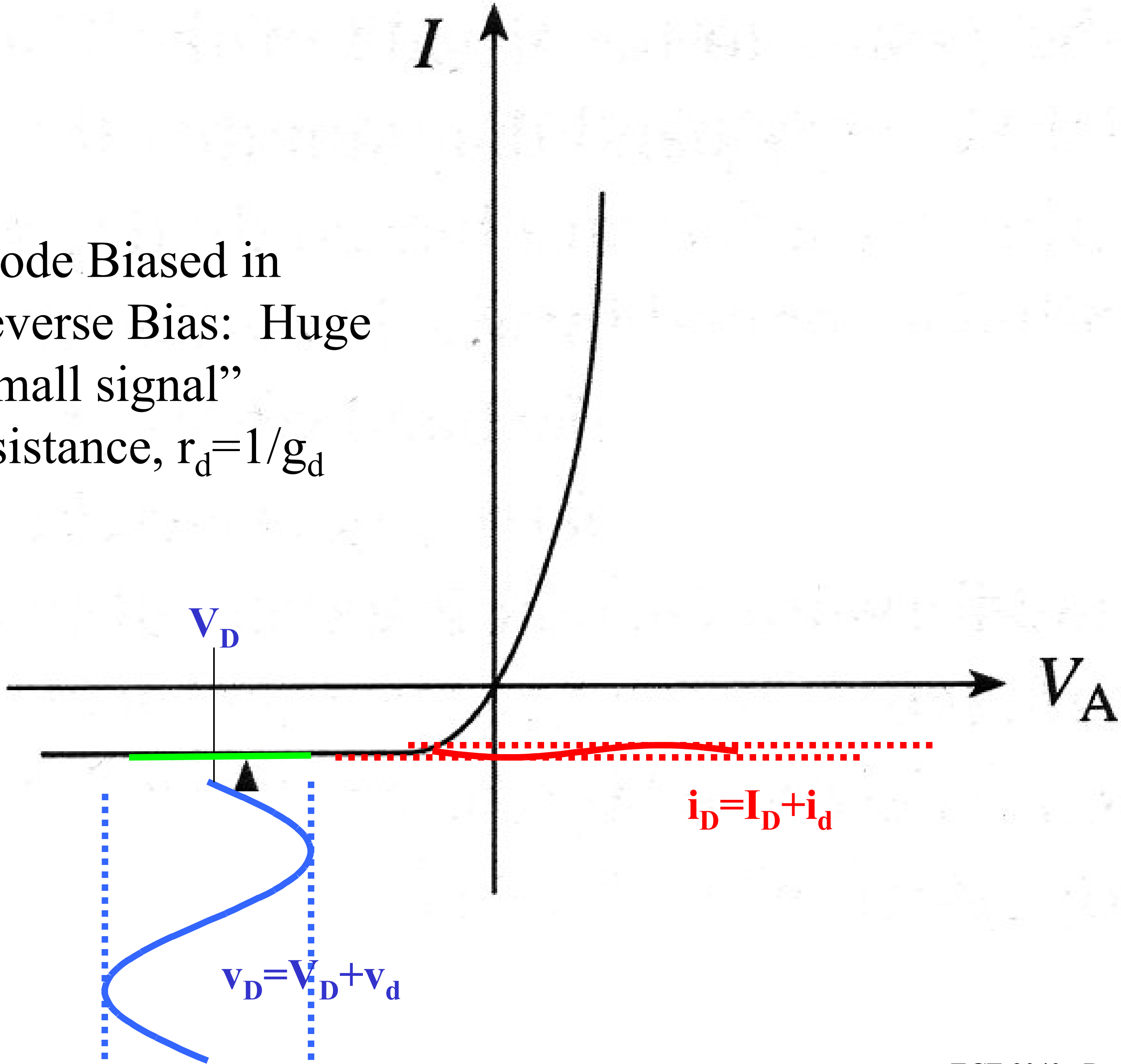
$$g_d = \frac{I_D + I_S}{V_T} \quad in\ General$$

$$g_d \approx \frac{I_D}{V_T} \quad in\ Forward\ Bias \longrightarrow \mathrm{V_A} >> 0 \rightarrow \mathrm{I_D} \approx I_o e^{V_A/V_T} \quad where\ V_T = \frac{kT}{q}$$

$$g_d \approx \frac{-I_S + I_S}{V_T} \approx 0 \quad in\ \mathrm{Re}verse\ Bias \longrightarrow \mathrm{V_A} << 0 \rightarrow \quad e^{V_A/V_T} \rightarrow 0$$

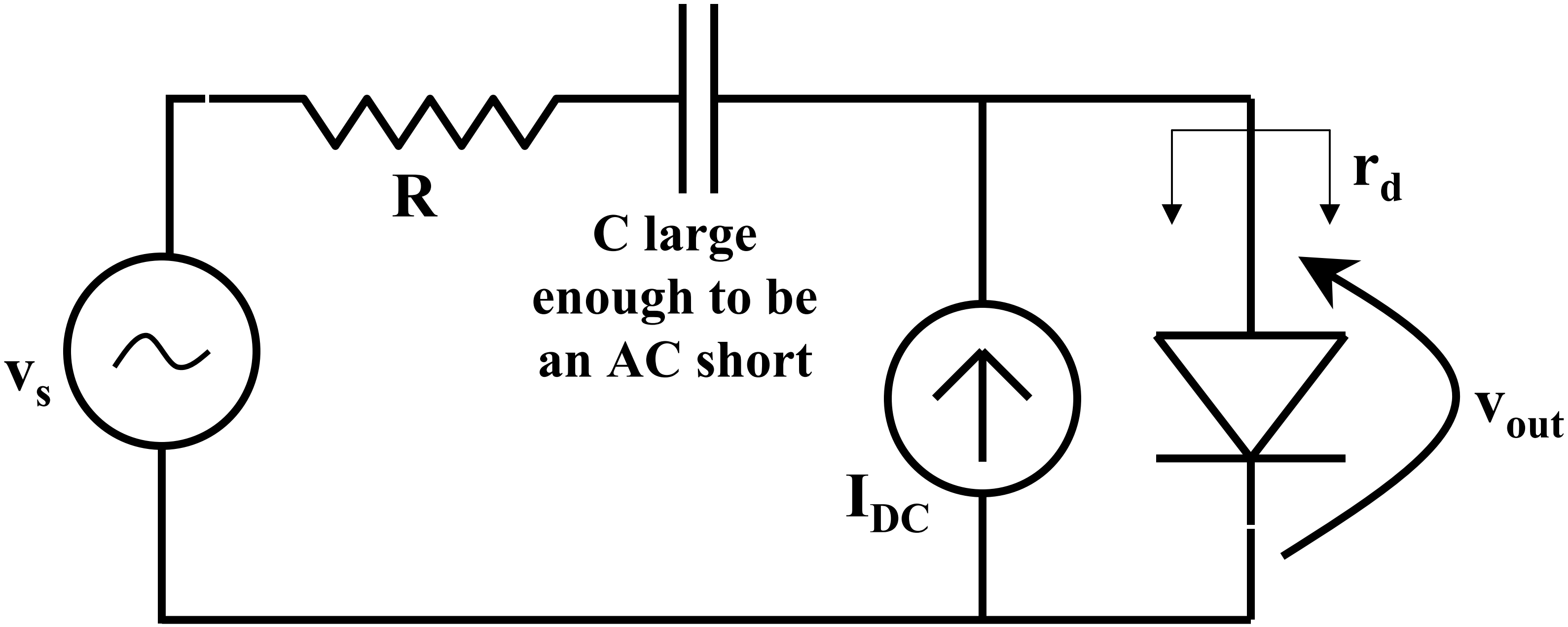
Small Signal Analysis of Diodes

Diode Biased in Reverse Bias: Huge "small signal" resistance, $r_d=1/g_d$



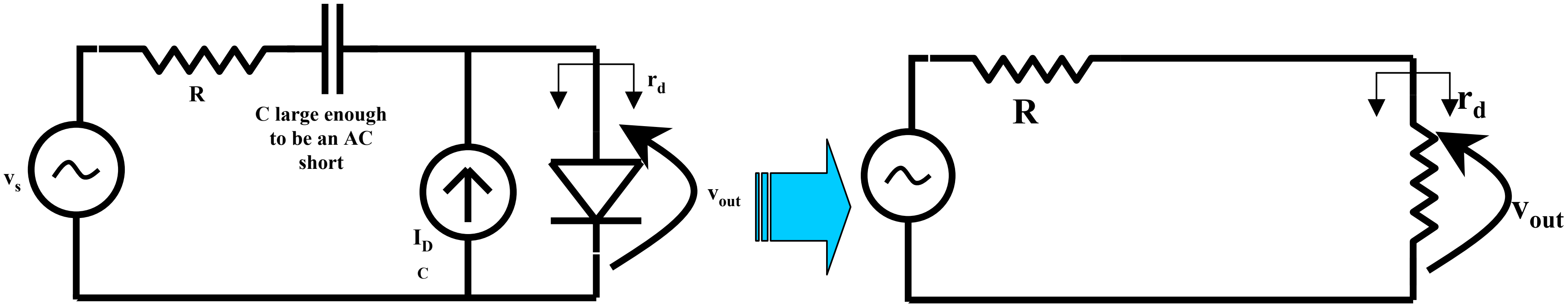
Small Signal Analysis of Diodes:

Application: Diode as an AC variable attenuator



Small Signal Analysis of Diodes:

Conversion to AC equivalent circuit



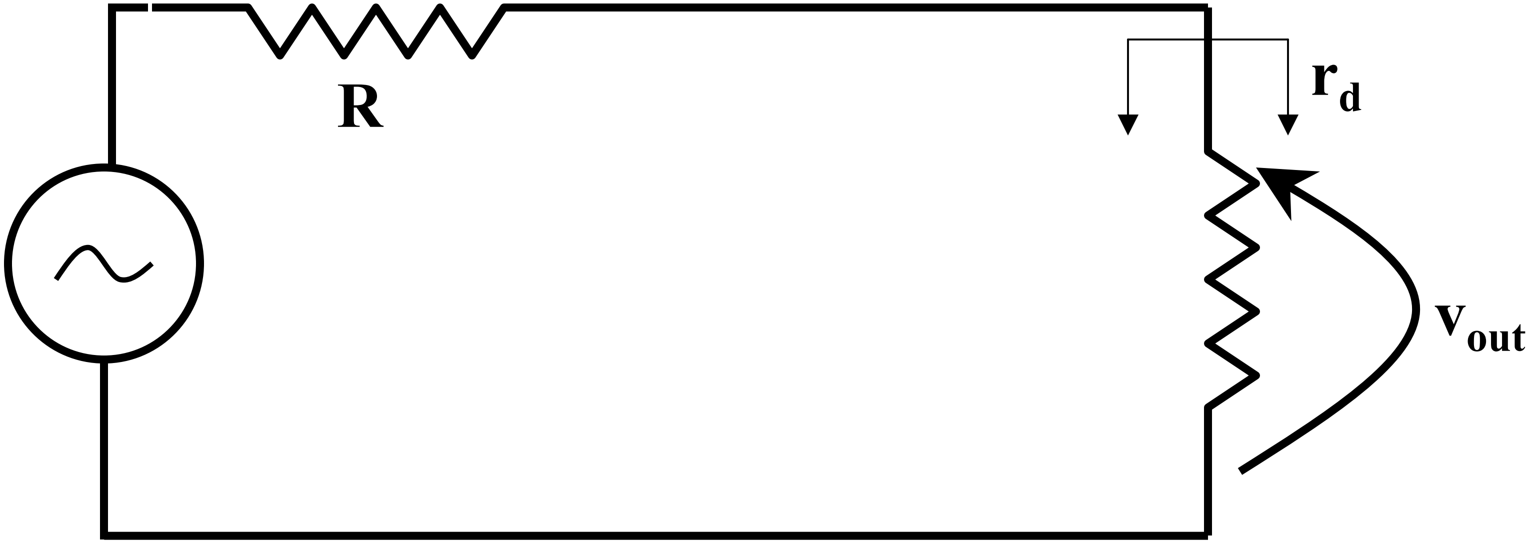
Steps to Analyze a Diode Circuit

1.) Determine DC operating point and calculate small signal parameters, r_d and others to come in later lectures)

2.) Convert to the AC only model.
- •DC Voltage sources are shorts
- •DC Current sources are open circuits
- •Large capacitors are short circuits
- •Large inductors are open circuits

Small Signal Analysis of Diodes:

Application: Diode as an AC variable attenuator



$$v_{out} = v_{in} \frac{r_d}{r_d + R}$$

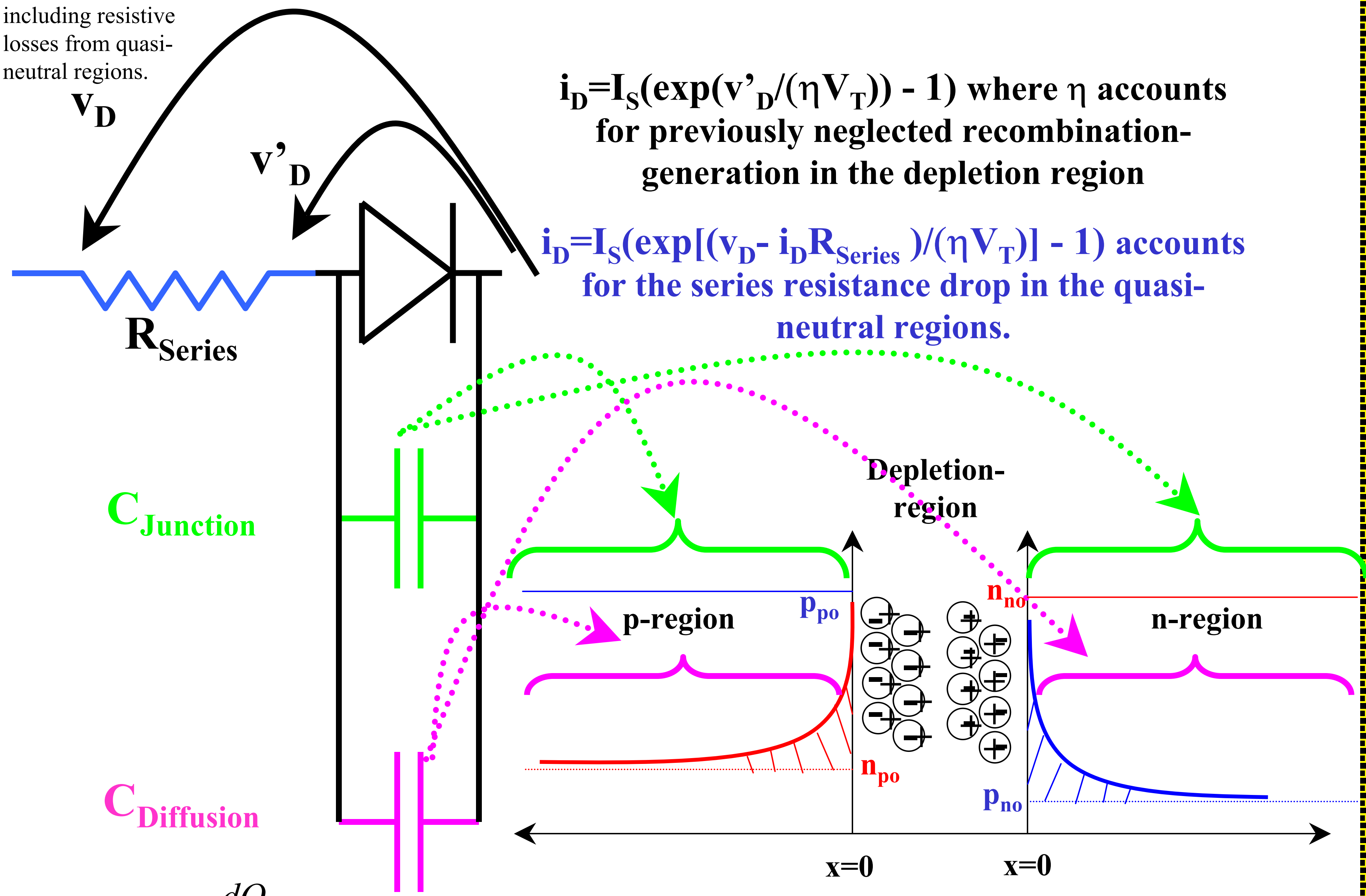
$$v_{out} = v_{in} \frac{1}{1 + \dfrac{R}{r_d}} = v_{in} \frac{1}{1 + \dfrac{(I_{DC} + I_S)R}{V_T}}$$ *or at room temperature*

$$v_{out} \approx v_{in} \frac{1}{1 + 40(I_{DC} + I_S)R}$$

Completing the Large signal model of a diode

$i_D = I_S(\exp(v'_D/(\eta V_T)) - 1)$ where η accounts for previously neglected recombination-generation in the depletion region

$i_D = I_S(\exp[(v_D - i_D R_{Series})/(\eta V_T)] - 1)$ accounts for the series resistance drop in the quasi-neutral regions.



$$C = \frac{dQ}{dv'_D} = \text{Change in charge resulting from a change in voltage}$$

Completing the Large signal model of a diode

For an abrupt diode (uniform doping on both sides of the junction):

$$C_{junction} = \frac{K_s \varepsilon_o A}{W}$$

$$but...$$

$$W = x_p + x_n = \sqrt{\frac{2K_S\varepsilon_o}{q}\frac{(N_A + N_D)}{N_A N_D}(V_{bi} - V_A)}$$

$$C_{junction} = A\sqrt{\frac{qK_S\varepsilon_o}{2}\frac{N_A N_D}{(N_A + N_D)}\frac{1}{(V_{bi} - V_A)}}$$

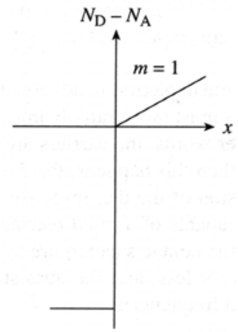
$$Thus,$$

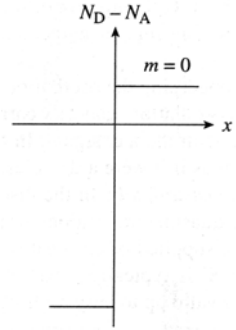
$$C_{Jo} = C_{junction}\Big|_{V_A=0} = A\sqrt{\frac{qK_S\varepsilon_o}{2}\frac{N_A N_D}{(N_A + N_D)}\frac{1}{(V_{bi})}} \quad and \quad C_J = \frac{C_{Jo}}{\sqrt{1 - \frac{V_A}{V_{bi}}}}$$

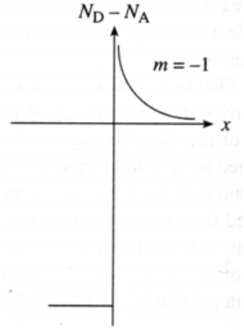
Junction capacitance is due to *majority carrier* charges displaced by the depletion width (I.e. similar to a parallel plate capacitor).

Completing the Large signal model of a diode

More generally for a profile with a constant doping on the heavily doped side of the junction and variable doping profile on the a low doped side that is described by: $N(x)=bx^m$ for all $x>0$







$$C_{junction} = \frac{K_s \varepsilon_o A}{W}$$

but...

$$W = x_p + x_n = \left[\frac{(m+2) K_S \varepsilon_o}{qb} \left(V_{bi} - V_A \right) \right]^{1/(m+2)}$$

$$C_{junction} = \frac{A K_S \varepsilon_o}{\left[\frac{(m+2) K_S \varepsilon_o}{qb} \left(V_{bi} - V_A \right) \right]^{1/(m+2)}}$$

Thus,

$$C_{Jo} = C_{junction}\Big|_{V_A=0} = \frac{A K_S \varepsilon_o}{\left[\frac{(m+2) K_S \varepsilon_o}{qb} \left(V_{bi} \right) \right]^{1/(m+2)}} \quad and \quad C_J = \frac{C_{Jo}}{\left(1 - \frac{V_A}{V_{bi}} \right)^{1/(m+2)}}$$

Junction capacitance is due to *majority carrier* charges displaced by the depletion width (I.e. similar to a parallel plate capacitor).

Completing the Large signal model of a diode

$$C_{Diffusion} = \frac{dQ_D}{dv'_D}$$

$$= \frac{dQ_D}{dt}\frac{dt}{dv'_D}$$

$$Q_D = qA\int_0^{\infty} p_{no}\left(e^{v'_D/V_T} - 1\right)e^{-x/L_p}dx + qA\int_0^{\infty} n_{po}\left(e^{v'_D/V_T} - 1\right)e^{-x/L_n}dx$$

$$= \left(e^{v'_D/V_T} - 1\right)\left[p_{no}L_p + n_{po}L_n\right]qA$$

$$\frac{dQ_D}{dt} = \frac{1}{V_T}\left(e^{v'_D/V_T}\right)\left[p_{no}L_p + n_{po}L_n\right]qA\frac{dv'_D}{dt}$$

$$\frac{dQ_D}{dt} = \frac{1}{V_T}\left[\frac{I_S\left(e^{v'_D/V_T} - 1 + 1\right)}{I_S}\right]\left[p_{no}L_p + n_{po}L_n\right]qA\frac{dv'_D}{dt}$$

Diffusion capacitance due to “excess injected” *minority carrier* charge at the depletion region edges. Since this charge results from minority carriers, this capacitance is negligible at zero or reverse biases.

Completing the Large signal model of a diode

$$\frac{dQ_D}{dt}=\frac{1}{V_T}\left[\frac{i_D+I_S}{I_S}\right]\left[p_{no}L_p+n_{po}L_n\right]qA\frac{dv_D^{'}}{dt}$$

$$\frac{dQ_D}{dt}=\left[\frac{i_D+I_S}{V_T}\right]\frac{\left[p_{no}L_p+n_{po}L_n\right]qA}{I_S}\frac{dv_D^{'}}{dt}$$

$i_D=I_D+i_d$

$i_D \sim I_D$

$$\frac{dQ_D}{dt}=g_d\frac{\left[p_{no}L_p+n_{po}L_n\right]qA}{I_S}\frac{dv_D^{'}}{dt}$$

$$C_{Diffusion}=\frac{dQ_D}{dt}\frac{dt}{dv_D^{'}}=g_d\frac{\left[p_{no}L_p+n_{po}L_n\right]qA}{I_S}\left(\frac{dv_D^{'}}{dt}\frac{dt}{dv_D^{'}}\right)$$

$$C_{Diffusion}=g_d\frac{\left[p_{no}L_p+n_{po}L_n\right]qA}{I_S}=g_d\left[\frac{cm^{-3}cm\ q\ cm^{2}}{\frac{q}{\sec}}\right]=g_d\left[\sec\right]$$

Unit analysis

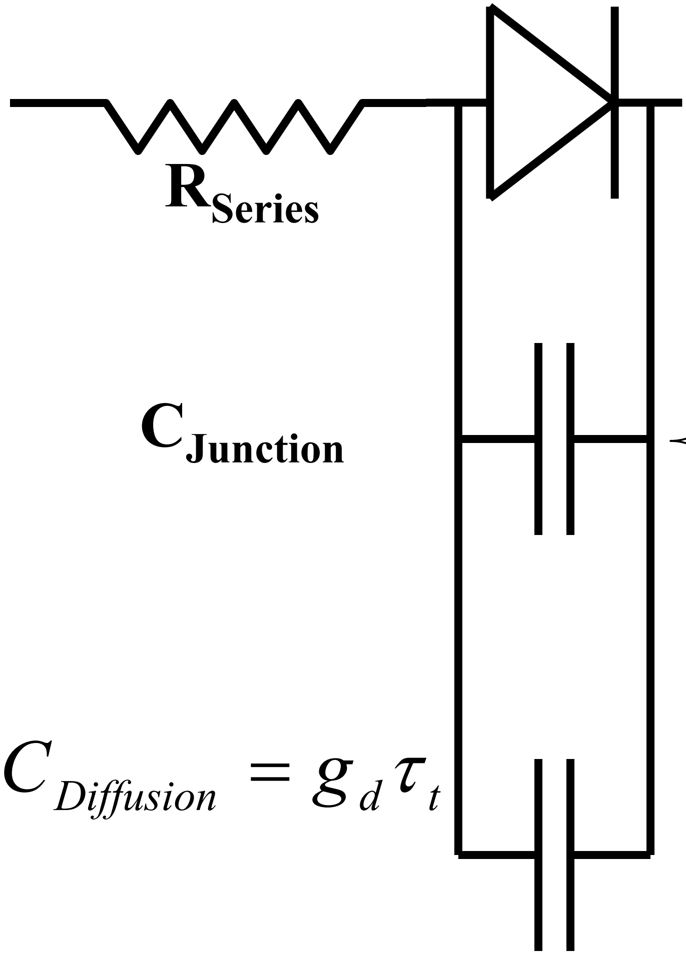
$$C_{Diffusion}=g_d\tau_t \quad where\ \tau_t=\frac{\left[p_{no}L_p+n_{po}L_n\right]qA}{I_S}$$ *is the transit time* or how quickly a carrier can respond to a change in voltage (physically the carriers have to move across the junction, requiring a finite time to do so)

$$or\ in\ SPICE,\quad C_{Diffusion}=\frac{\partial i_D}{\partial v_D}\tau_t$$

Diffusion capacitance due to "excess injected" *minority carrier* charge at the depletion region edges.

Summary of the Large signal model of a diode (SPICE Model)

$$i_D = I_S\left(e^{\left(v_D - i_D R_{Series}\right)/\eta V_T} - 1\right)$$

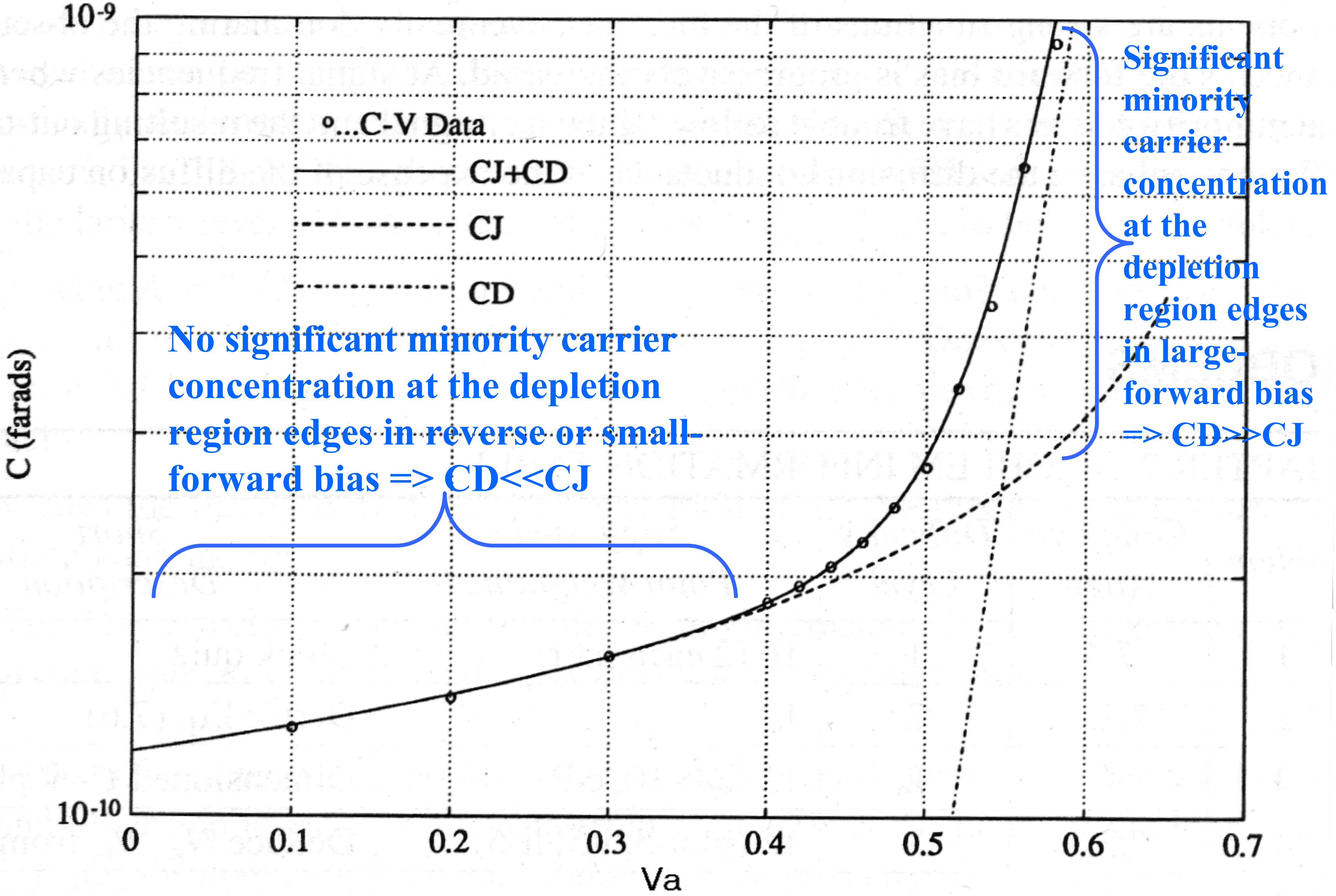


$$C_{Diffusion} = g_d \tau_t$$

$$\left\{ \begin{array}{l} C_{Jo} = C_{junction}\Big|_{V_A=0} = \dfrac{A K_S \varepsilon_o}{\left[\dfrac{(m+2) K_S \varepsilon_o}{qb}\left(V_{bi}\right)\right]^{1/(m+2)}} \\ \\ and \quad C_J = \dfrac{C_{Jo}}{\left(1 - \dfrac{V_A}{V_{bi}}\right)^{1/(m+2)}} \Rightarrow f\left(V_A\right) \end{array} \right.$$

1.) Mathematical model
2.) SPICE Model (this page)
3.) Ideal Diode Model
4.) Constant Voltage Drop (CVD) Model
5.) Graphical circuit model

Addition of Capacitance Components



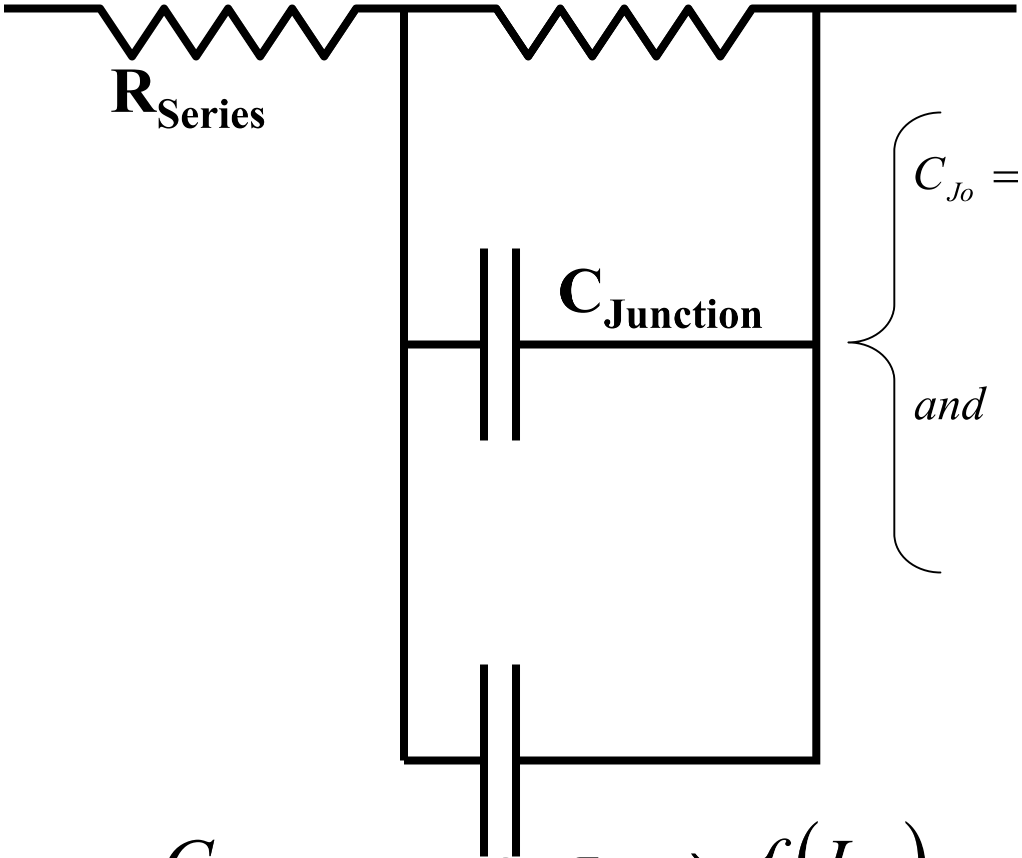
No significant minority carrier concentration at the depletion region edges in reverse or small-forward bias => CD<<CJ

Significant minority carrier concentration at the depletion region edges in large-forward bias => CD>>CJ

Summary of the Small signal model of a diode

$$i_D = I_D + g_d v_d \quad where \quad g_d = \frac{I_D + I_S}{V_T}$$

$$\mathrm{r_d} = 1/\mathrm{g_d} \quad \Rightarrow f\left(I_D\right)$$



$$\left\{ \begin{array}{l} C_{Jo} = C_{junction}\Big|_{V_A=0} = \dfrac{AK_S\varepsilon_o}{\left[\dfrac{(m+2)K_S\varepsilon_o}{qb}\left(V_{bi}\right)\right]^{1/(m+2)}} \\ and \quad C_J = \dfrac{C_{Jo}}{\left(1-\dfrac{V_A}{V_{bi}}\right)^{1/(m+2)}} \Rightarrow f\left(V_A\right) \end{array} \right.$$

$$C_{Diffusion} = g_d \tau_t \Rightarrow f\left(I_D\right)$$

Things we have added to account for "Non-ideal" behavior

- Series resistance to account for finite resistance of the quasi-neutral regions and metal contact resistance's.
- Diode "ideality factor", η, to account for thermal recombination-generation in the depletion region.
- Junction capacitance due to majority carrier charges displaced by the depletion width (I.e. similar to a parallel plate capacitor).
- Diffusion capacitance due to "excess injected" minority carrier charge at the depletion region edges. Since this charge results from minority carriers, this capacitance is negligible at zero or reverse biases.

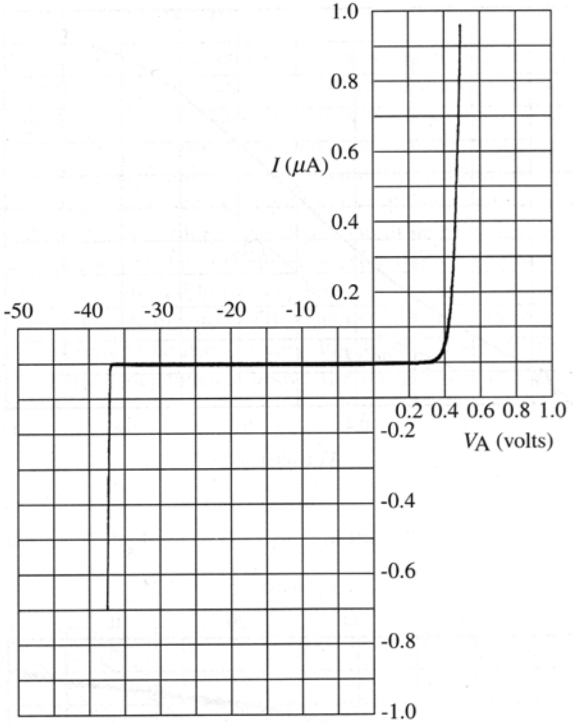
Things we still need to add to account for "Non-ideal" behavior

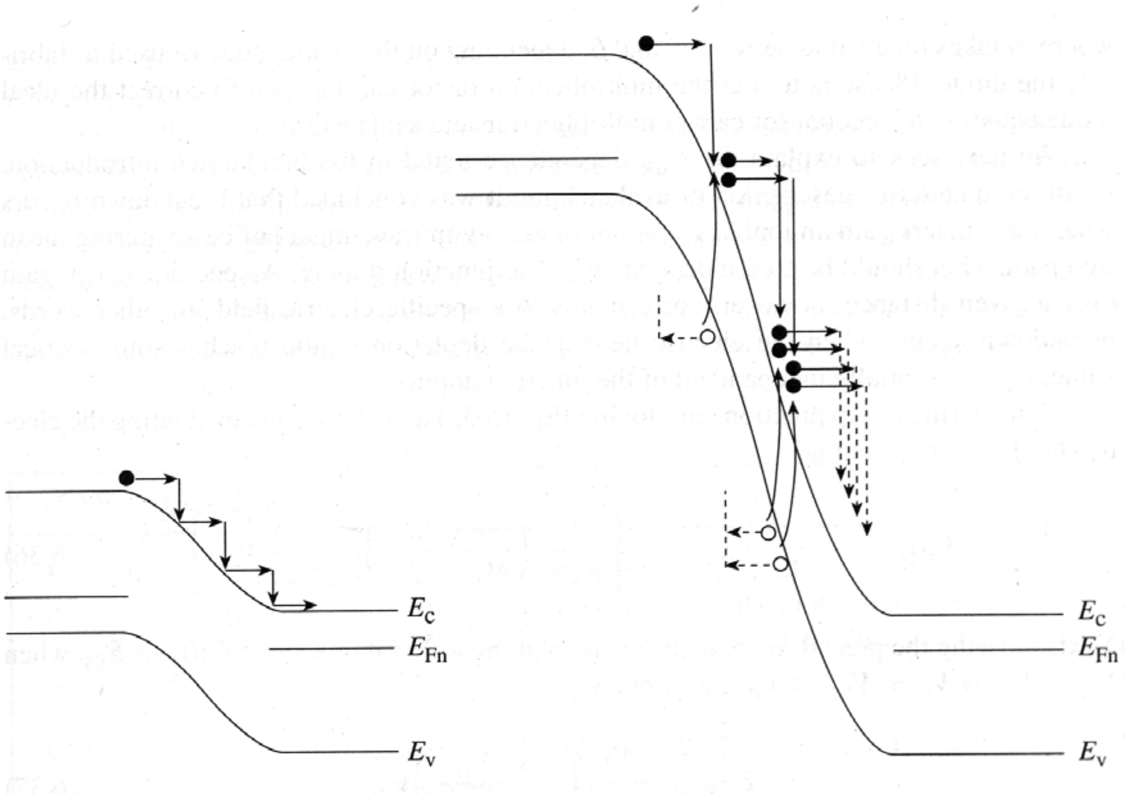
- Reverse "Breakdown" characteristics
  - "Breakdown" is a deceptive term because no damage typically occurs to the device. Often diodes are designed to operate in the breakdown mode.

Breakdown Mechanisms

Avalanche Breakdown:

Excess current flows due to electron-hole pair multiplication due to impact ionization. This current rapidly increases with increasing reverse bias.





(a) Small reverse bias

(b) $|V_A| \rightarrow V_{BR}$

Breakdown Mechanisms

Zener Breakdown:

Excess current flows due to bonding electrons "tunneling" into empty conduction band states. The "tunneling barrier" must be sufficiently thin. This current rapidly increases with increasing reverse bias.

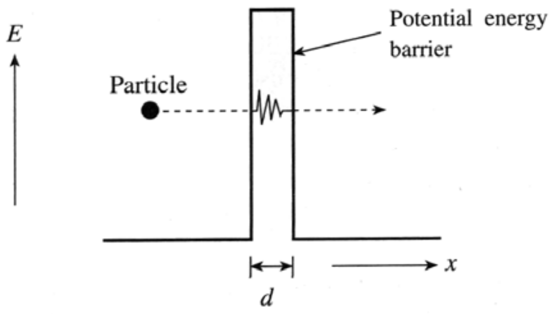
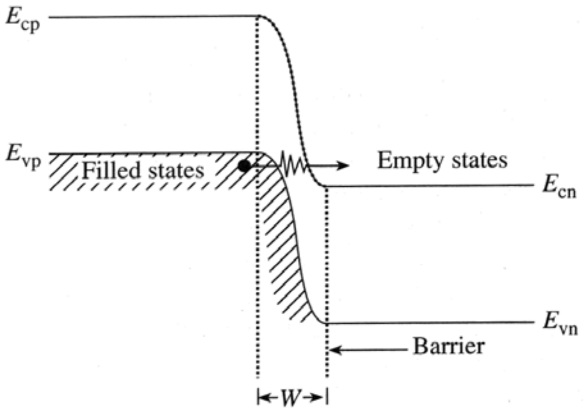


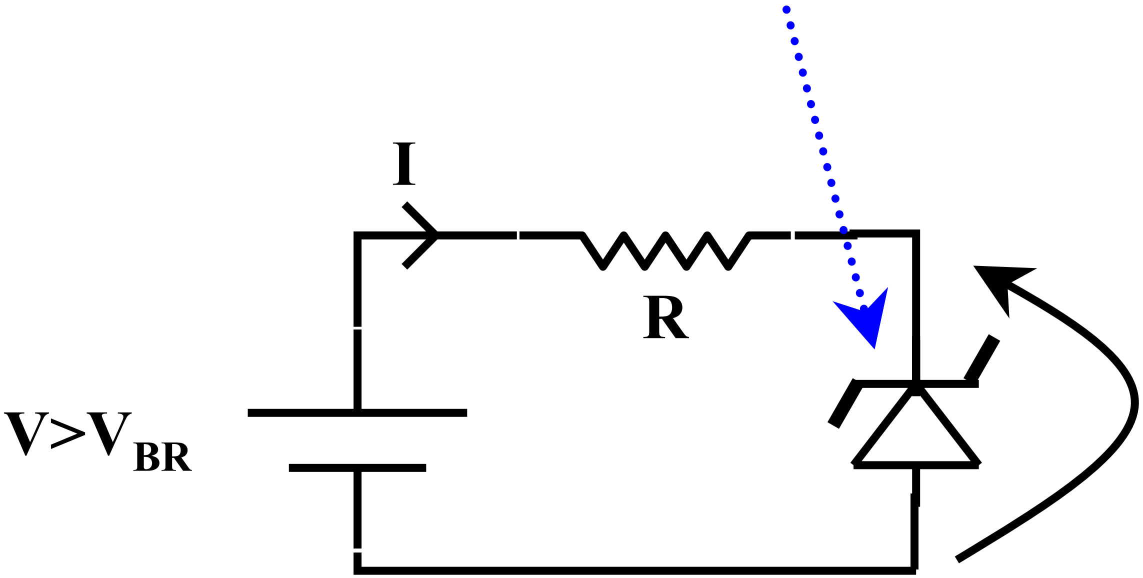
Figure 6.13 General visualization of tunneling.



“Zener” Diodes

Zener diodes may actually operate based on either avalanche or zener breakdown mechanisms.

Rule of thumb: $|V_{BR}|>6E_G/q$ is typically Avalanche Breakdown



Slightly different symbol

V_{BR} almost constant can act as a high voltage (~1V - 100 V) DC reference