Lecture 23

Metal Oxide Capacitors

Reading: Pierret 16.2-16.3

Notes

MOS Capacitor

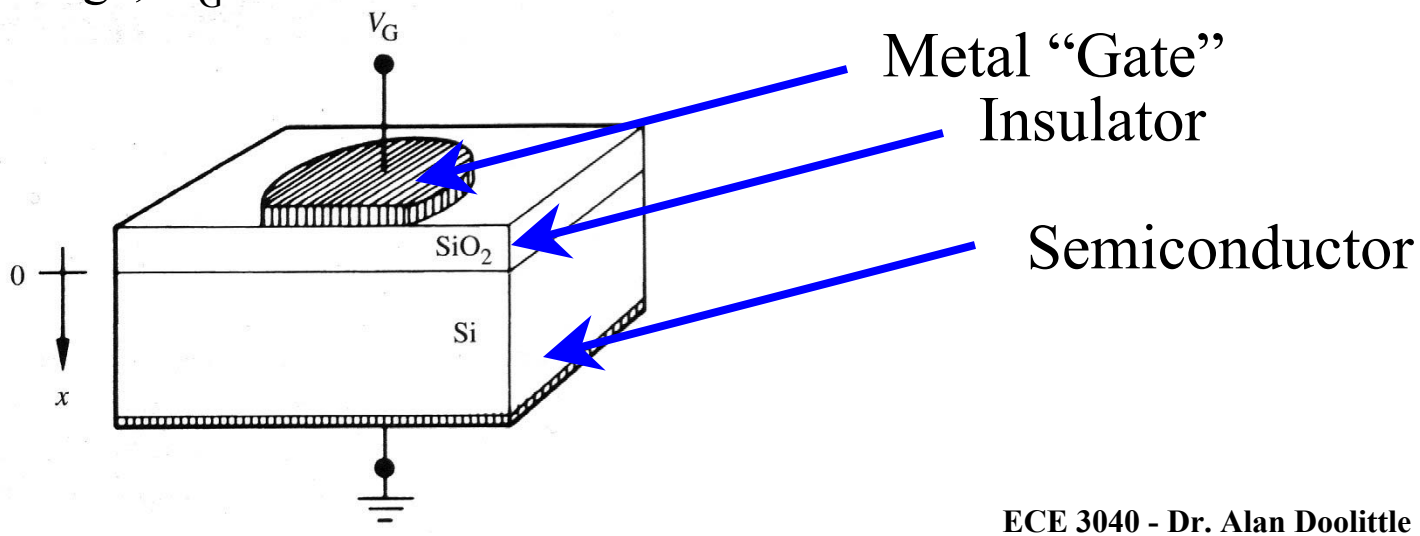
"MOS" = Metal- Oxide- Semiconductor

"MOS" actually refers to "Metal"– Silicon Dioxide – Silicon

Other material systems have similar "MIS" structures formed by Metal – Insulator – Semiconductor

The capacitor itself forms the basis of digital logic circuits, and DRAM storage units (storing charge) or can simply supply a capacitance for an analog integrated circuit. It will also be the building block for the most common transistor produced – the MOS transistor.

The substrate is normally taken to be grounded and the "Gate" electrode can be biased with a voltage, V_G



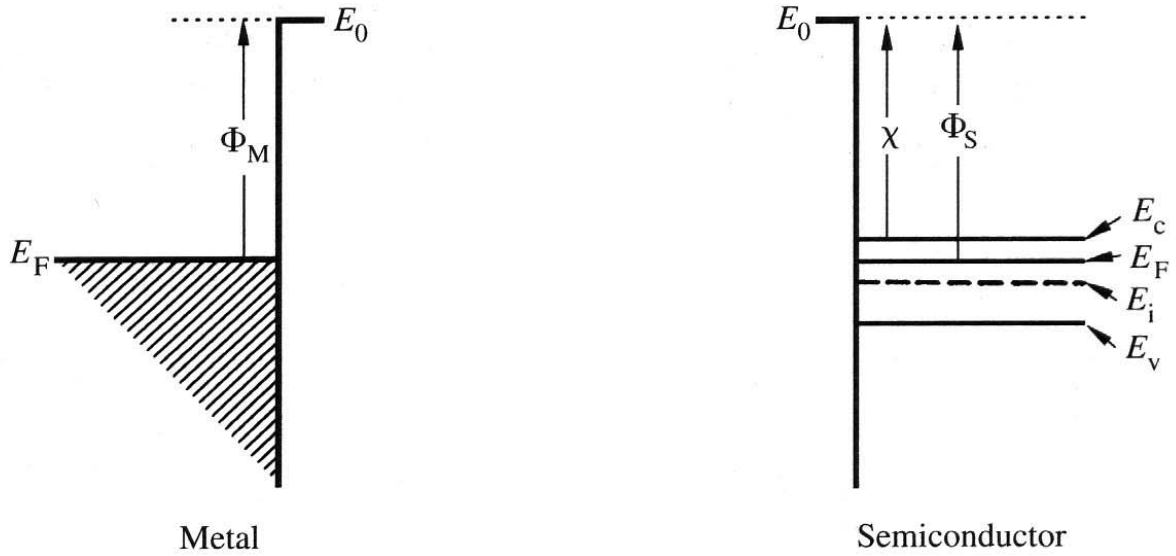
MOS Capacitor

Key assumptions:

1) Metal is an equipotential region.
2) Oxide is a perfect insulator with zero current flow.
3) Neither oxide nor oxide-semiconductor interface have charge centers.
4) Semiconductor is uniformly doped.
5) An ohmic contact has been established on the back side of the wafer.
6) Analysis will be one-dimensional.
7) The semiconductor is thick enough to have a quasi-neutral region (where electric field is zero and all energy bands are flat).
8) Certain energy relationships exist:

$$\Phi_M = \Phi_S = \chi + (E_C - E_F)_{FB}$$ (terms defined in next few slides)

MOS Capacitor



Metal Semiconductor

E_O= Vacuum Energy Level. The minimum energy an electron must have to free itself from the material.

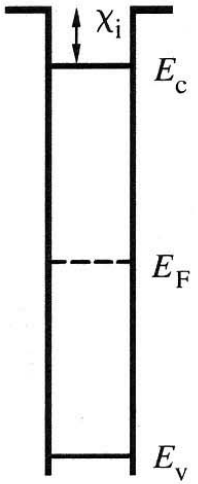
Φ_M = "Work function" of the metal. This is the energy difference from the fermi energy (average energy) of an electron in the metal to the vacuum energy level.

Φ_S = "Work function" of the semiconductor. This is the energy difference from the fermi energy (average energy) of an electron in the semiconductor to the vacuum energy level. Note that this energy depends on doping since E_F depends on doping

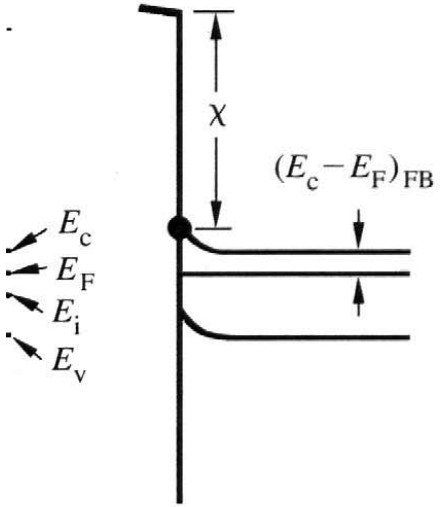
χ = Electron Affinity of the semiconductor. This is the energy difference from the conduction band minimum in the semiconductor to the vacuum energy level. Note that this energy does NOT depend on doping

$(E_C - E_F)_{FB} = \Phi_S - \chi$ in the quasi-neutral region where the bands are not bent or are in "flat band"

MOS Capacitor



Insulator

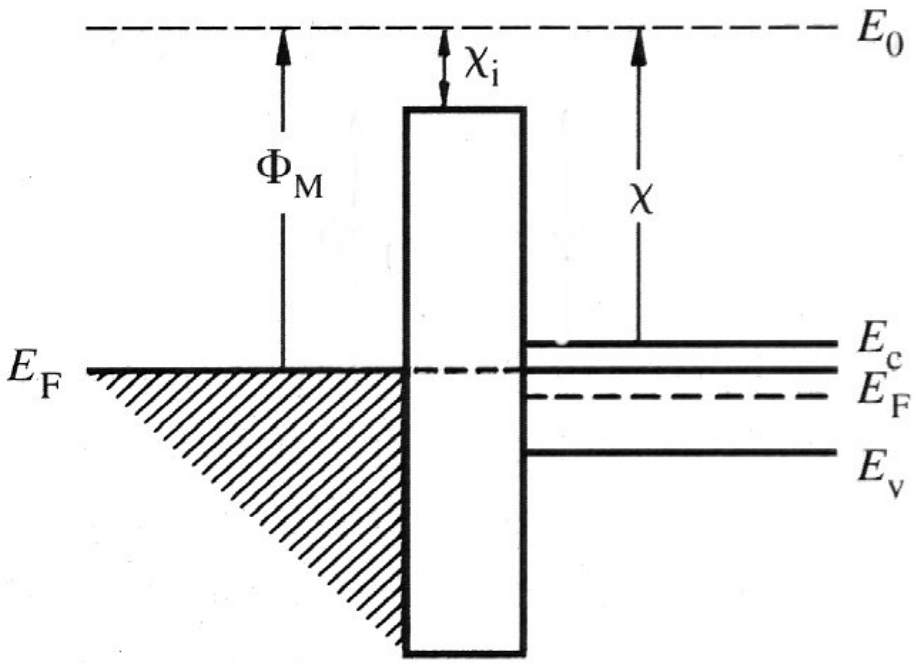


Semiconductor with band bending

The insulator is simply a very wide bandgap, intrinsically doped semiconductor characterized by an electron affinity, χ_i .

The semiconductor can have an electric field near the insulator that forces the energy bands to bend near the insulator-semiconductor interface.

MOS Capacitor

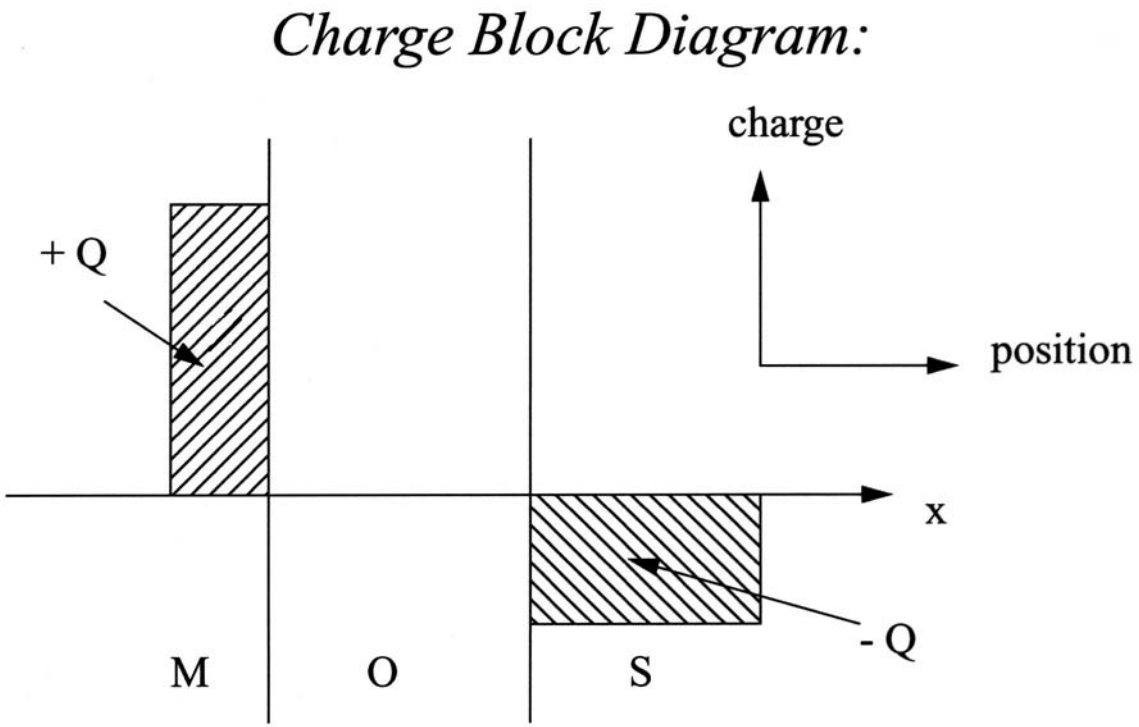


Since the insulator prevents any current from flowing, when we bring the materials together, the fermi-energy must be flat.

Likewise, if no charges are stored on the "plates" (metal and semiconductor regions near the insulator) of the capacitor, the bands are not bent in the insulator nor semiconductor. Note the assumption of an equipotential surface in the metal simply states that a perfect conductor can not support and electric field (electrostatics).

MOS Capacitor

Capacitor under bias



A positive voltage on the gate puts positive charge on the gate electrode. Gauss's law forces an equal negative charge to form near the semiconductor-insulator interface.

Charge separated by a distance implies an electric field across the insulator.

MOS Capacitor

Capacitor under bias

If V_G = bias voltage applied to the gate (metal).

For all V_G the Fermi level *in the each layer* remains flat due to zero current through the structure.

The applied bias separates the Fermi levels at the metal and semiconductor ends by qV_G

$$E_F(\text{metal}) - E_F(\text{semiconductor}) = -qV_G$$

If the semiconductor is grounded (fixed at any constant potential we can call ground):

- metal side Fermi level moves downward if $V_G > 0$
- metal side Fermi level moves upward if $V_G < 0$

Applying Poisson's equation to the oxide, since there are no charges in the oxide,

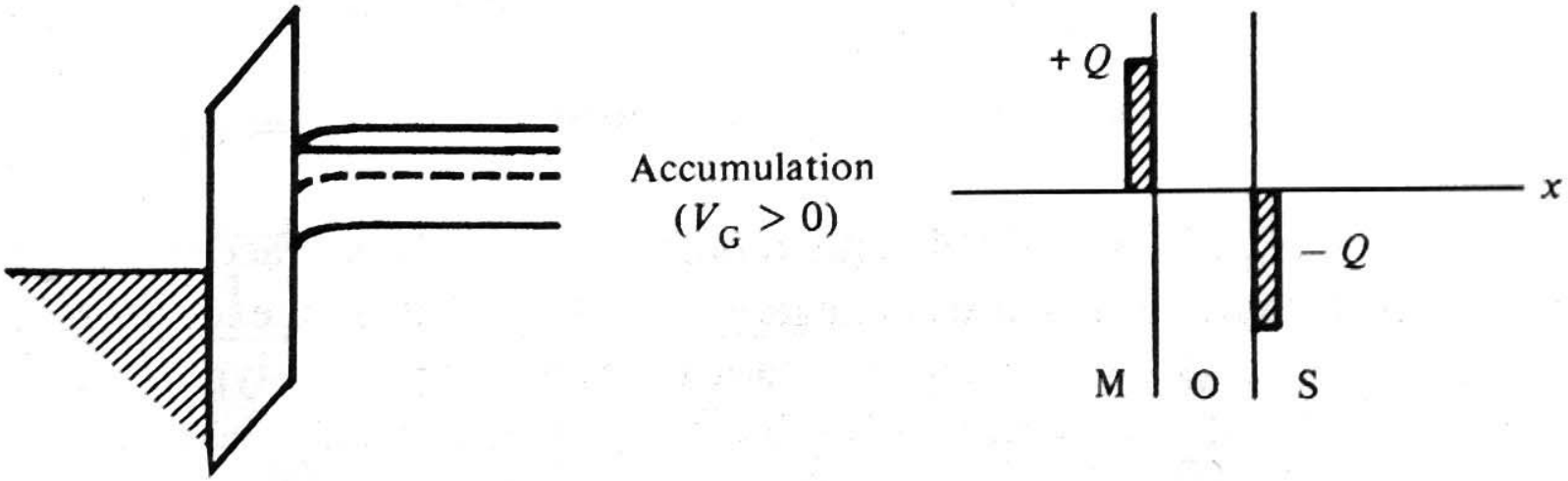
$$\frac{dE_{oxide}}{dx} = \rho = 0 \quad \Rightarrow \quad E_{oxide} = Cons\tan t$$

$$V = \int E_{oxide} dx \Rightarrow Potential \text{ varies linearly with x}$$

Since the potential varies linearly with x, so does the energy bands

MOS Capacitor

Capacitor under bias



For an n-type semiconductor.

•When $V_G > 0$ the metal fermi-energy is lowered (E=-qV), the insulator has an electric field across it that terminates almost immediately in the near perfectly conducting metal, but terminates over a finite distance in the semiconductor of "finite resistivity".

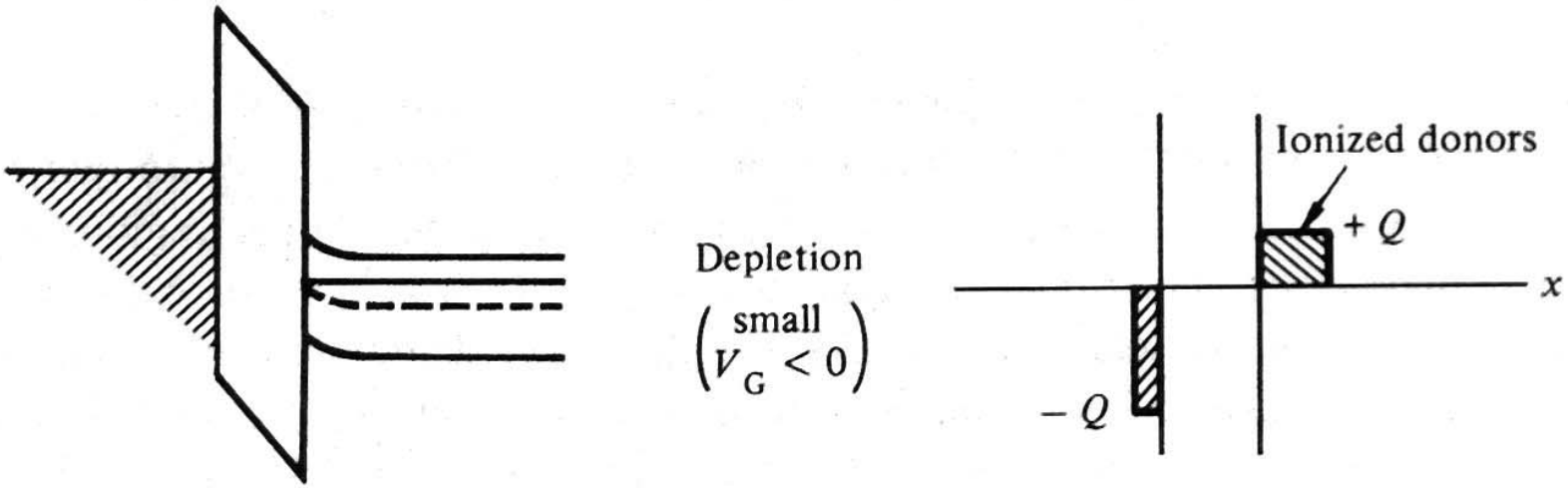
•The charge model indicates that negative charge must be created in the semiconductor near the interface. This charge is in the form of electrons.

•Since $n = n_i \exp[(E_F - E_i)/ kT]$, the electron concentration in the semiconductor near interface increases.

•This is called ***accumulation***

MOS Capacitor

Capacitor under bias



For an n-type semiconductor.

•When $V_G < 0$ the metal fermi-energy is **raised** (E=-qV), the insulator has an electric field across it that terminates almost immediately in the near perfectly conducting metal, but terminates over a finite distance in the semiconductor of "finite resistivity".

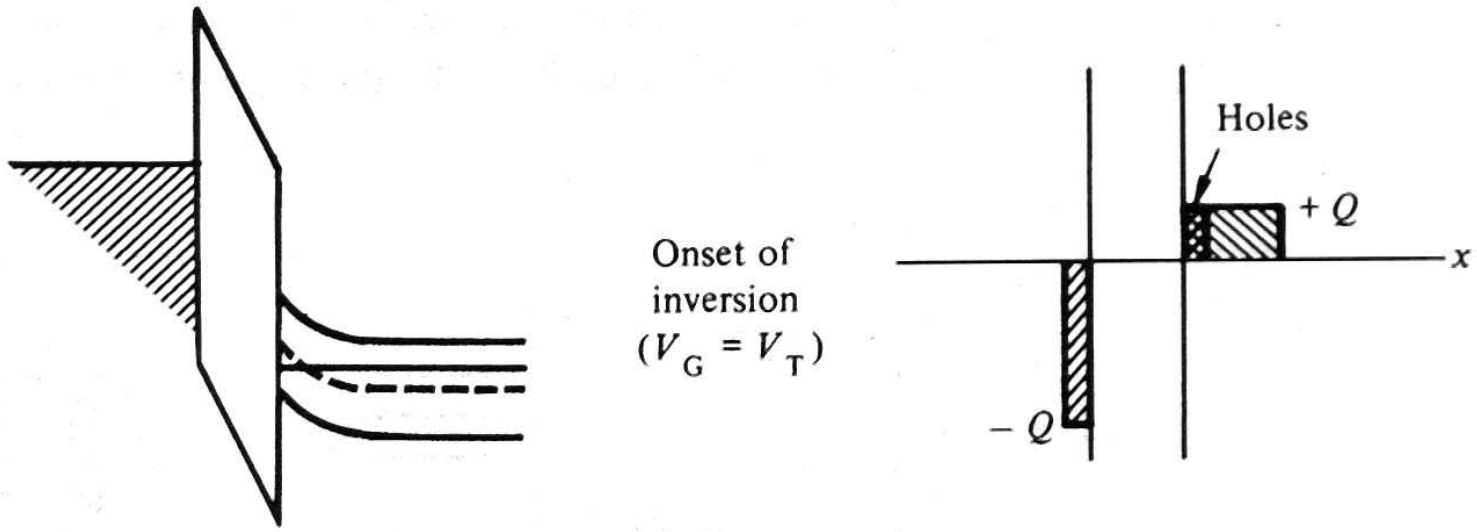
•The charge model indicates that positive charge must be created in the semiconductor near the interface. This charge is in the form of ionized donors.

•Since $n = n_i \exp[(E_F - E_i)/ kT]$, the electron concentration in the semiconductor near interface decreases.

•This is called ***depletion***.

MOS Capacitor

Capacitor under bias



For an n-type semiconductor.

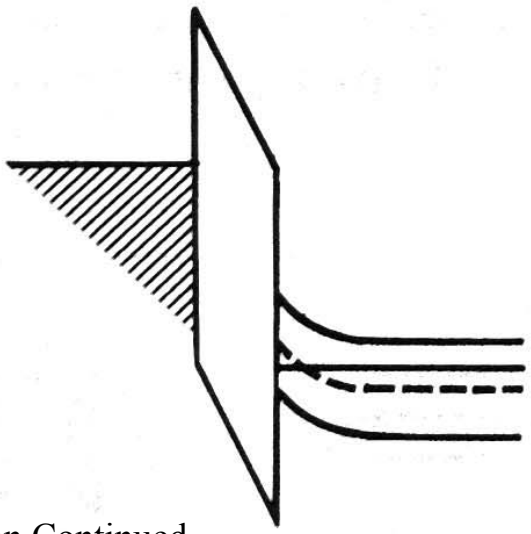
•For higher magnitudes of bias ($V_G < 0$) the fermi-energy near the interface crosses-the intrinsic energy and the "type" of material swaps from n-type to p-type (only locally near the interface).

•The charge model indicates that positive charge must be created in the semiconductor near the interface. This charge is in the form of ionized donors and holes.

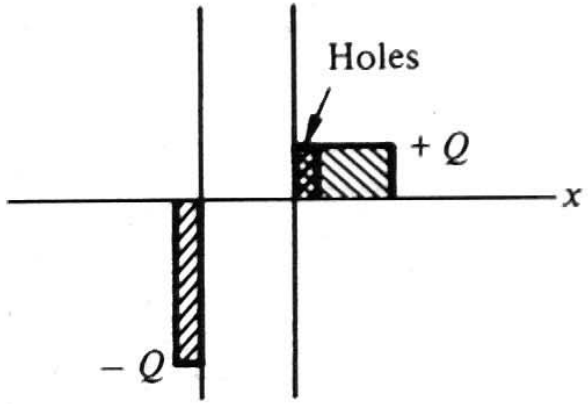
Inversion continued on next slide…

MOS Capacitor

Capacitor under bias



Onset of inversion ($V_G = V_T$)



Inversion Continued…

•The hole concentration near the interface must equal the donor concentration. Thus,

$$p_{interface} = N_D$$

$$p_{interface} = n_i \exp[(E_{i\text{-}INTERFACE} - E_F)/ kT] = n_i \exp[(E_F - E_{i\text{-}BULK})/ kT]$$

•This is called ***inversion***.

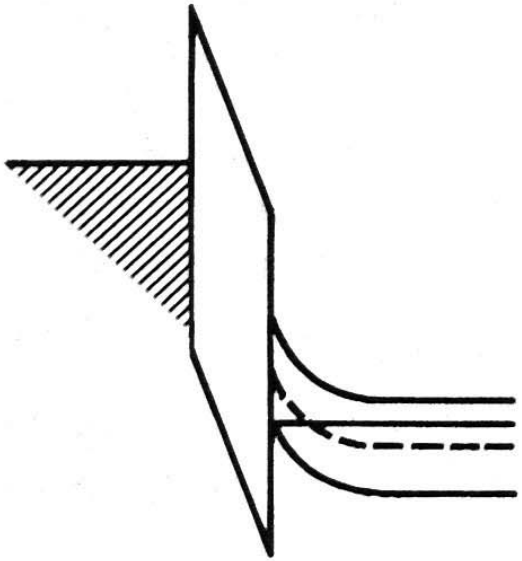
•The onset of inversion occurs for a voltage called the ***threshold voltage*** V_T (not thermal voltage)

•Detailed calculations taking into account the charge distribution as a function of position in the semiconductor indicates that inversion occurs when,

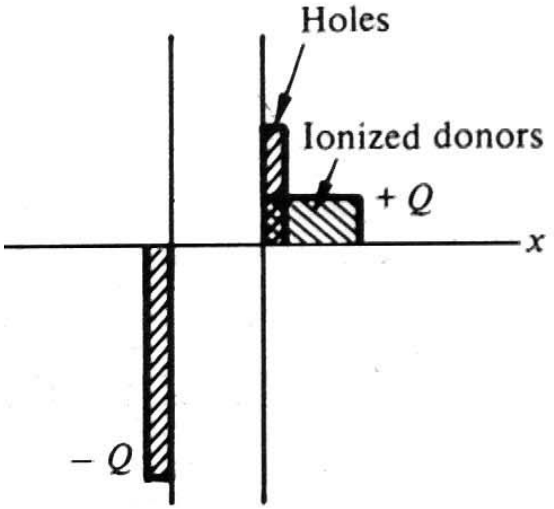
$$E_{i\text{-}INTERFACE} - E_{i\text{-}BULK} = 2 (E_F - E_{i\text{-}BULK})$$

MOS Capacitor

Capacitor under bias



Strong Inversion
($V_G < V_T$)



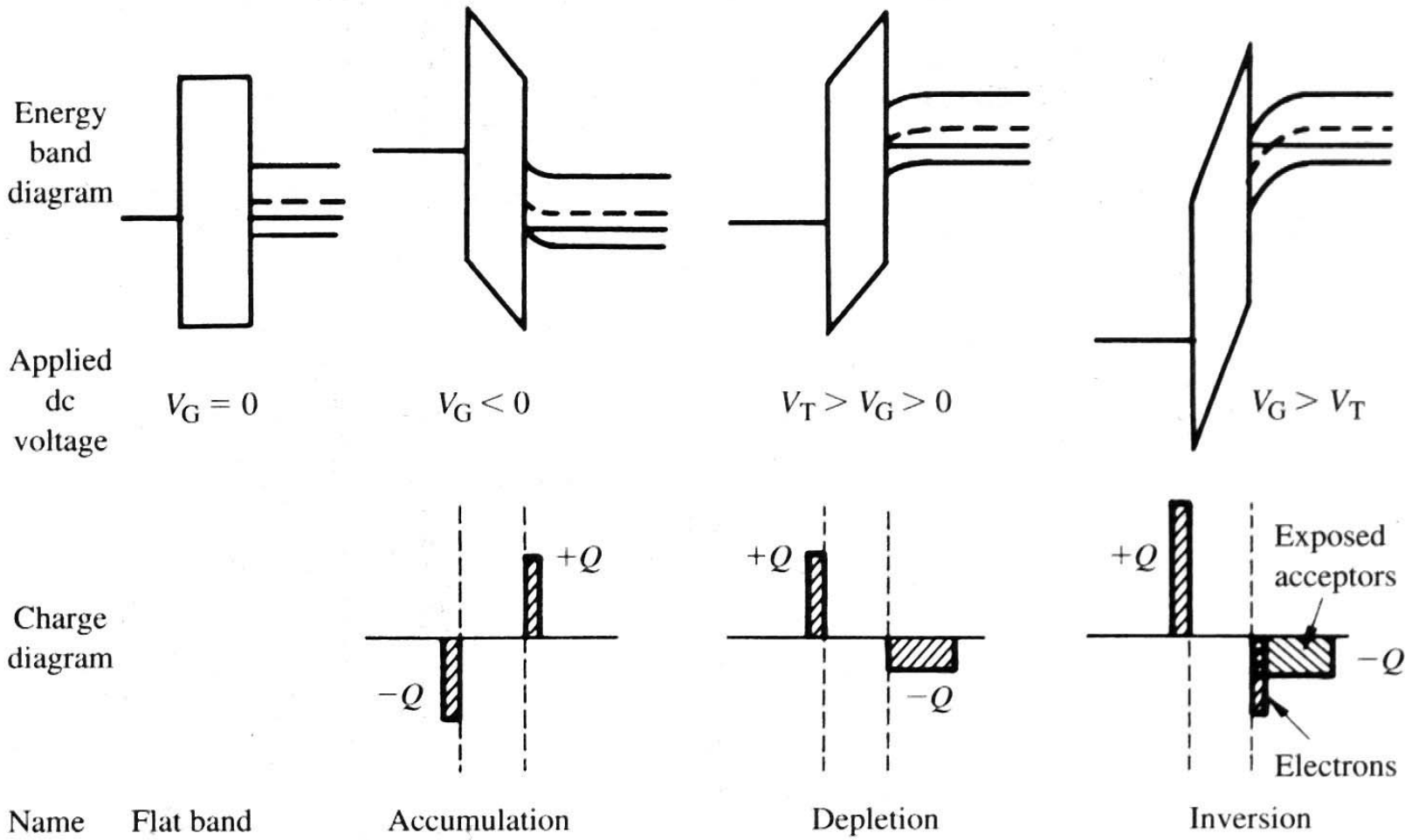
For an n-type semiconductor.

•For still higher magnitudes of bias ($V_G < 0$) the hole concentration continues to increase resulting in a very high concentration of holes near the interface.

•This is known as strong inversion.

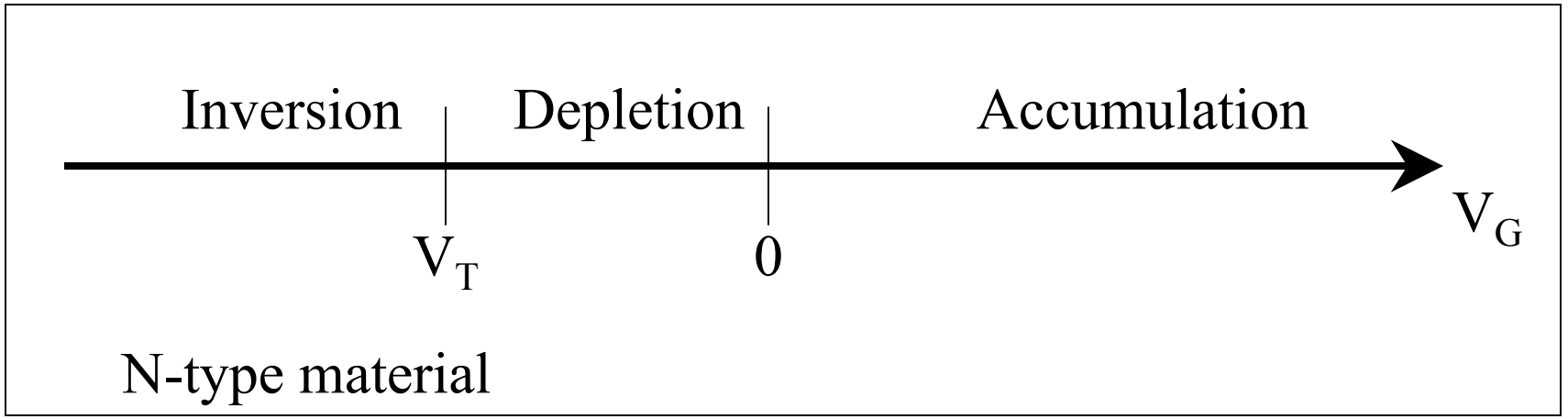
MOS Capacitor

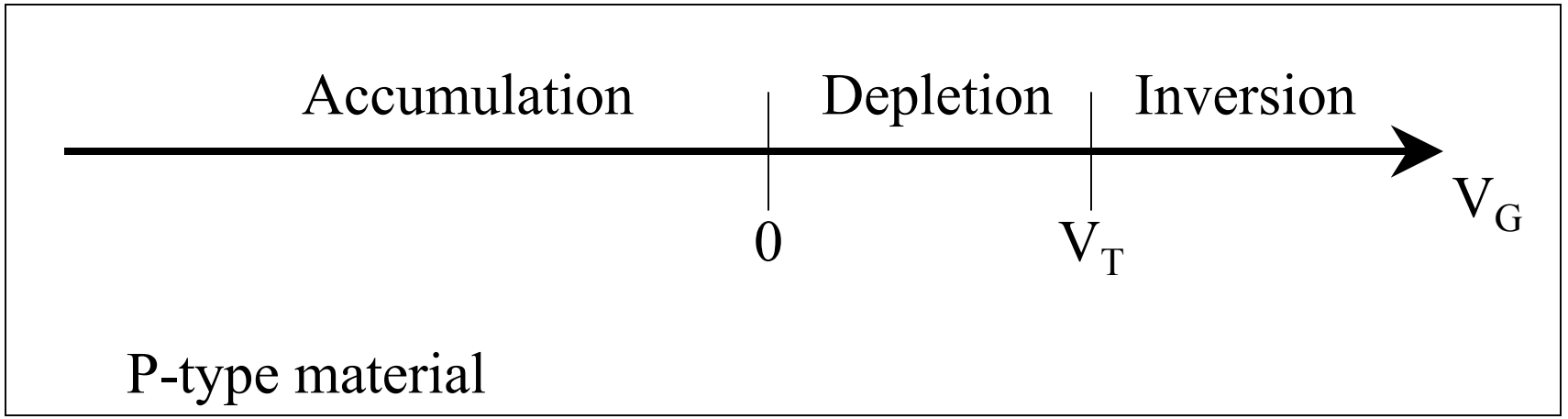
Capacitor under bias for P-type material



MOS Capacitor

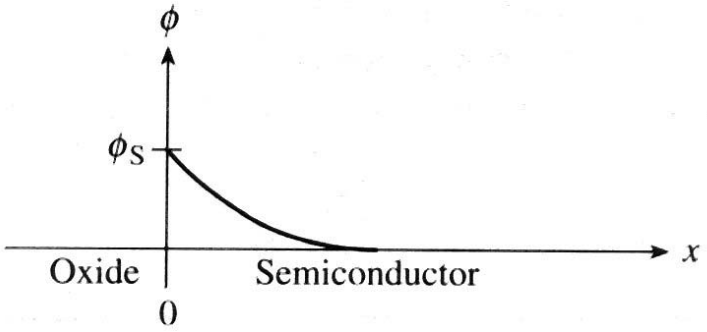
Capacitor under bias Summary





MOS Capacitor
Quantitative Solution

Let $\phi(x)$ = electrostatic potential inside the semiconductor at a depth x (measured from the oxide interface)



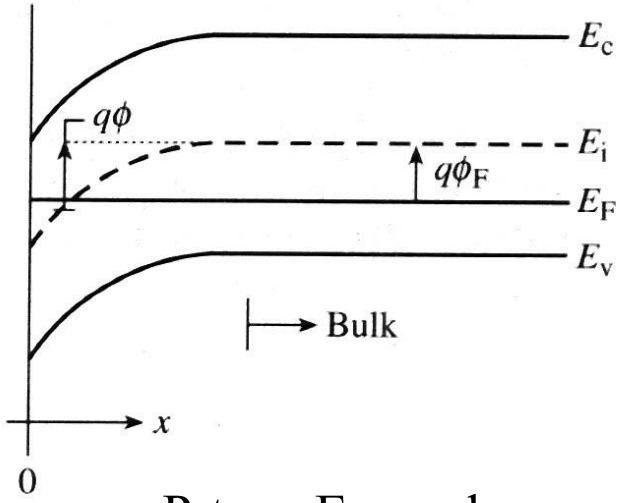
$$\phi(x) = \frac{1}{q}\left[E_{i-BULK} - E_i(x)\right] \equiv \text{electrostatic potential}$$

and

$$\phi_S = \frac{1}{q}\left[E_{i-BULK} - E_{i-INTERFACE}\right] \equiv \textit{surface potential}$$

along with,

$$\phi_F = \frac{1}{q}\left[E_{i-BULK} - E_F\right]$$



P-type Example

MOS Capacitor
Quantitative Solution

Since,

$$p_{BULK} = n_i e^{(E_{i-BULK} - E_F)/kT} = N_A \quad and \quad n_{BULK} = n_i e^{(E_F - E_{i-BULK})/kT} = N_D$$

$$\phi_F = \begin{cases} \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) & \text{for a p - type semiconductor} \\ -\frac{kT}{q}\ln\left(\frac{N_D}{n_i}\right) & \text{for a n - type semiconductor} \end{cases}$$

Thus,

$$\phi_S = 2\phi_F \quad \text{at the depletion - invertion transition point, } V_G = V_T$$

MOS Capacitor
Quantitative Solution

Since the MOS-Capacitor is symmetric (equal charge on metal as is in the semiconductor) and has no charge in the oxide, we can solve for the electrostatic variables using only the semiconductor section of material.

Things to note:

Charge due to accumulation bias and inversion bias results in a very narrow charge distribution near the interface.

Charge due to depletion bias results in a wide “depletion width”, W

MOS Capacitor
Quantitative Solution

Once again, if we apply the "Depletion Region Approximation" (neglect all charges but those due to ionized dopants) and assume p-type material,

$$\rho = q\left(p - n + N_D - N_A\right) \cong -qN_A \quad \text{for } (0 \le x \le W) \quad \text{where W is the depletion width}$$

And from Poisson's equation using a boundary condition that the electric field goes to zero at the depletion region edge,

$$\frac{dE}{dx} = \frac{-qN_A}{K_S\varepsilon_o} \quad \Rightarrow \quad \boxed{E(x) = -\frac{d\phi}{dx} = \frac{qN_A}{K_S\varepsilon_o}\left(W - x\right)}$$

And finally, the electrostatic potential can be found by integrating using a boundary condition that the electrostatic potential goes to zero at the depletion region edge,

$$\boxed{\phi = \frac{qN_A}{2K_S\varepsilon_o}\left(W - x\right)^2}$$

MOS Capacitor
Quantitative Solution

The depletion width, W, can be found by noting that $\phi=\phi_S$ at x=0

$$W = \sqrt{\frac{K_S \varepsilon_o}{qN_A}\phi_S}$$

The depletion width at the inversion-depletion transition, W_T, can be found by noting that $2\phi_F=\phi_S$

$$W_T = \sqrt{\frac{K_S \varepsilon_o}{qN_A} 2\phi_F} = \sqrt{\frac{K_S \varepsilon_o 2kT}{q^2 N_A} \ln\left(\frac{N_A}{n_i}\right)}$$

NOTE: To obtain the equations for n-type substrates, we simply repeat the above procedure replacing N_A with $-N_D$

MOS Capacitor
Quantitative Solution

How is the gate voltage V_G distributed throughout the structure?

$$V_G = \phi_S + \phi_{oxide} \quad \text{(no drop in the metal)}$$

From before, we said,

$$\frac{dE_{oxide}}{dx} = \rho = 0 \quad \Rightarrow \quad E_{oxide} = Cons\tan t = -\frac{d\phi_{oxide}}{dx}$$

$$\phi_{oxide} = \int_{-x_{oxide\ thickness}}^{0} E_{oxide}\,dx = \left(x_{oxide\ thickness}\right)E_{oxide}$$

But, Gauss's Law states that the electric displacement,

$D = \varepsilon E$ must be continuous in the direction normal to the interface.

Thus,

$$\frac{E_{oxide}}{E_{Semiconductor\ at\ the\ Interface}} = \frac{K_S\,\varepsilon_o}{K_{ox}\varepsilon_o} = \frac{K_S}{K_{ox}}$$

where K_S and K_{ox} are the relative dielectric constants in the semiconductor and the oxide

MOS Capacitor

Quantitative Solution

Thus,

$$\phi_{oxide} = \frac{K_S}{K_{ox}}\left(x_{oxide\ thickness}\right)E_{Semiconductor\ at\ the\ Interface}$$

And using the previous expressions,

$$V_G = \phi_S + \frac{K_S}{K_{ox}}\left(x_{oxide\ thickness}\right)E_{Semiconductor\ at\ the\ Interface}$$

but using $W = \sqrt{\frac{K_S \varepsilon_o}{qN_A}\phi_S}$ *and* $E(x) = \frac{qN_A}{K_S \varepsilon_o}(W - x)$ at x = 0

$$E_{Semiconductor\ at\ the\ Interface} = \sqrt{\frac{2qN_A}{K_S \varepsilon_o}\phi_S}$$

Thus,

$$V_G = \phi_S + \frac{K_S}{K_{ox}}\left(x_{oxide\ thickness}\right)\sqrt{\frac{2qN_A}{K_S \varepsilon_o}\phi_S} \quad \text{for } 0 \le \phi_S \le 2\phi_F$$

Relates the applied gate voltage to the surface potential!

MOS Capacitor
Quantitative Solution

But what about in inversion and accumulation?

For inversion and accumulation we can not invoke the depletion approximation due to a significant amount of charge near the interface due to sources other than just ionized dopants (these charges are the electrons and holes).

In inversion and accumulation , the vast majority of the gate voltage is dropped across the oxide

In inversion, the depletion width remains ~ constant

Thus, ϕ_S can not be much less (greater) than 0 for p-type (n-type)

Thus, ϕ_S can not be much greater (less) than $2\phi_F$ for p-type (n-type)

See discussion centered around figure 16.10 in Pierret if interested in more detail.