Lecture 25

MOSFET Basics (Understanding with Math)

Reading: Pierret 17.1-17.2 and Jaeger 4.1-4.10 and Notes

MOS Transistor I-V Derivation

With our expression relating the Gate voltage to the surface potential and the fact that $\phi_S=2\phi_F$ we can determine the value of the threshold voltage

$$V_T = 2\phi_F + \frac{\varepsilon_S}{C_{ox}}\sqrt{\frac{2qN_A}{\varepsilon_S}(2\phi_F)} \quad \text{(for n - channel devices)}$$

$$V_T = 2\phi_F - \frac{\varepsilon_S}{C_{ox}}\sqrt{\frac{2qN_D}{\varepsilon_S}(-2\phi_F)} \quad \text{(for p - channel devices)}$$

where,

$C_{ox} = \frac{\varepsilon_{ox}}{x_{ox}}$ is the oxide capacitance per unit area

Where we have made use of the use of the expression,

$$\varepsilon_S = K_S\varepsilon_o$$

MOS Transistor I-V Derivation

Coordinate Definitions for our "NMOS" Transistor

x=depth into the semiconductor from the oxide interface.

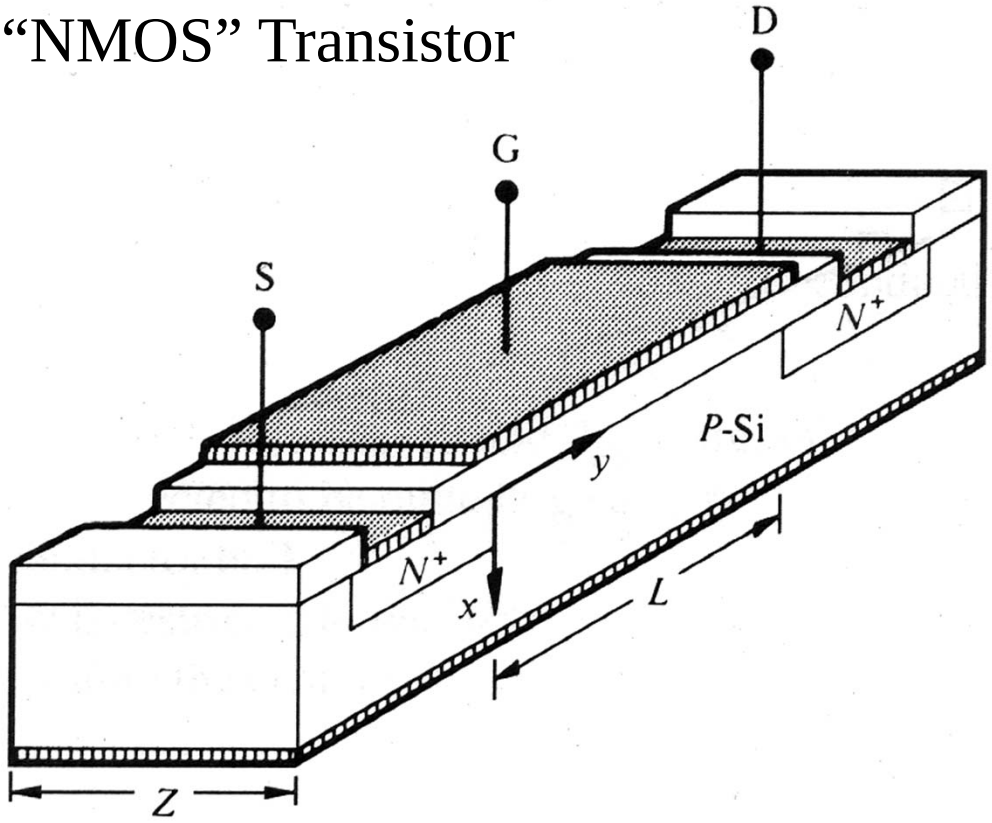
y=length along the channel from the source contact

z=width of the channel

$x_c(y)$ = channel depth (varies along the length of the channel).

n(x,y)= electron concentration at point (x,y)

$\mu_n(x,y)$=the mobility of the carriers at point (x,y)



Device width is Z

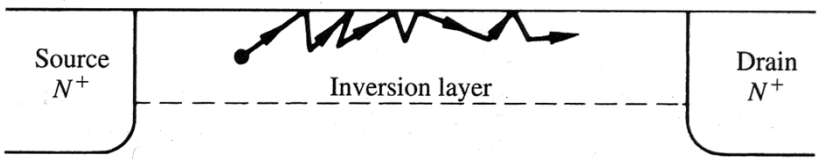
Channel Length is L

Assume a "Long Channel" device (for now do not worry about the channel length modulation effect)

MOS Transistor I-V Derivation

Concept of Effective mobility

The mobility of carriers near the interface is significantly lower than carriers in the semiconductor bulk due to interface scattering.



Since the electron concentration also varies with position, the average mobility of electrons in the channel, known as the effective mobility, can be calculated by a weighted average,

$$\overline{\mu_n} = \frac{\int_{x=0}^{x=x_c(y)} \mu_n(x,y)n(x,y)dx}{\int_{x=0}^{x=x_c(y)} n(x,y)dx}$$

or defining,

$$Q_N(y) = -q\int_{x=0}^{x=x_c(y)} n(x,y)dx \quad \left[charge/cm^2\right]$$

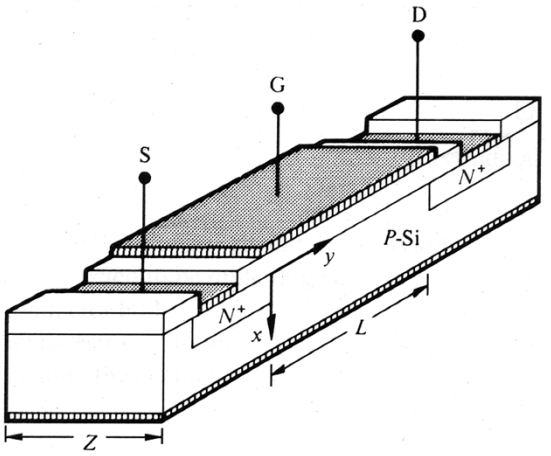
$$\overline{\mu_n} = \frac{-q}{Q_N(y)}\int_{x=0}^{x=x_c(y)} \mu_n(x,y)n(x,y)dx$$

Empirically

$$\overline{\mu_n} = \frac{\mu_o}{1+\theta\left(V_{GS}-V_T\right)}$$

where, μ_o *and* θ are constants

Drain Current-Voltage Relationship



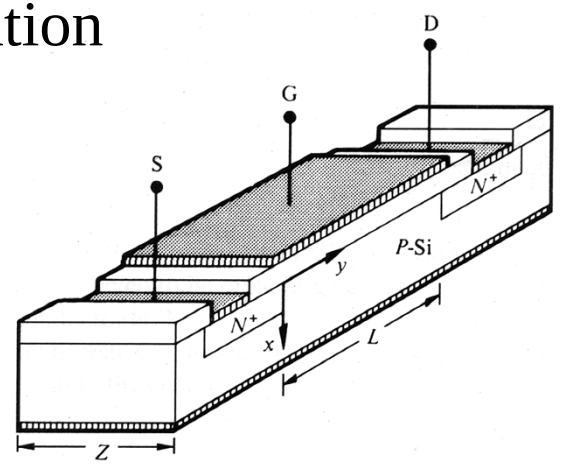
In the Linear Region, $V_{GS}>V_T$ and $0<V_{DS}<V_{dsat}$

$$J_N = q\mu_n nE + qD_N \nabla n$$

Neglecting the diffusion current, and recognizing the current is only in the y-direction,

$$J_N \cong J_{Ny} \cong q\mu_n nE_y \cong -q\mu_n n\frac{d\phi}{dy}$$

Drain Current-Voltage Relationship



In the Linear Region, $V_{GS}>V_T$ and $0<V_{DS}<V_{dsat}$

$$I_D = -\int\int J_{Ny}\,dx\,dz = Z\int_{x=0}^{x=x_c(y)} J_{Ny}\,dx$$

$$= \left(-Z\frac{d\phi}{dy}\right)\left(-q\int_{x=0}^{x=x_c(y)} \mu_n(x,y)n(x,y)\,dx\right)$$

$$= -Z\overline{\mu_n}Q_N\frac{d\phi}{dy}$$

$$\int_{y=0}^{y=L} I_D\,dy = -Z\overline{\mu_n}\int_{\phi=0}^{\phi=V_{DS}} Q_N\,d\phi$$

$$I_D L = -Z\overline{\mu_n}\int_{\phi=0}^{\phi=V_{DS}} Q_N\,d\phi$$

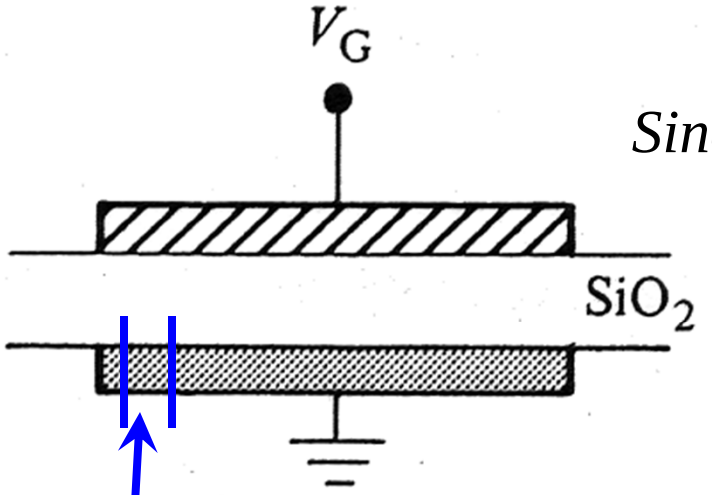
$$I_D = \frac{-Z\overline{\mu_n}}{L}\underbrace{\int_{\phi=0}^{\phi=V_{DS}} Q_N\,d\phi}$$

To find I_D, we need an expression relating the electrostatic potential, ϕ, and Q_N

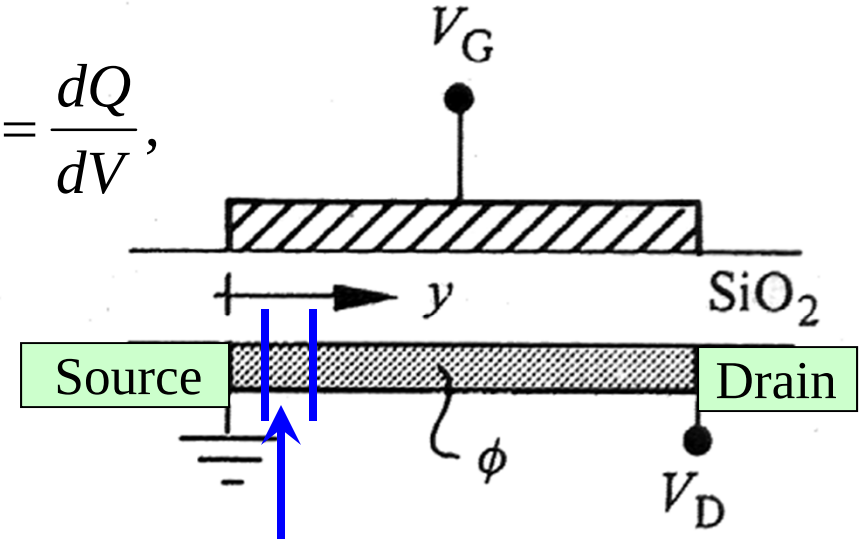
"Capacitor-Like" Model for Q_N

Assumptions:

- Neglect all but the mobile inversion charge (valid for deep inversion)
- For the MOSFET, the charge in the semiconductor is a linear function of position along the semiconductor side of the plate. Thus, ϕ varies from 0 to V_{DS}



$$Since \quad C_{ox} = \frac{dQ}{dV},$$



MOS Capacitor

Only voltages above threshold create inversion charge

$$Q_N \cong -C_{ox}\left(V_{GS} - V_T\right) \quad \text{for } V_{GS} \geq V_T$$

Neglect the depletion region charge

MOS Transistor

$$Q_N \cong -C_{ox}\left(V_{GS} - V_T - \phi\right)$$

for $V_{GS} \geq V_T$

Note: Assuming a linear variation of potential along the channel leads to an underestimation of current but is a good estimate for hand calculations.

MOS Transistor I-V Derivation

Using "Capacitor-Like" Model for Q_N we can estimate I_D as:

$$I_D = \frac{-Z\overline{\mu_n}}{L}\int_{\phi=0}^{\phi=V_{DS}} Q_N \, d\phi$$

$$I_D = \frac{-Z\overline{\mu_n}}{L}\int_{\phi=0}^{\phi=V_{DS}} -C_{ox}\left(V_G - V_T - \phi\right) d\phi$$

$$I_D = \frac{Z\overline{\mu_n}C_{ox}}{L}\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{V_{DS}^2}{2}\right] \qquad 0 \le V_{DS} \le V_{Dsat} \quad \textit{and} \quad V_{GS} \ge V_T$$

This is known as the "square law" describing the Current-Voltage characteristics in the "Linear" or "Triode" region.

Note the linear behavior for small V_{DS} (can neglect V_{DS}^2 term). Note the negative parabolic dependence for larger V_{DS} but still $V_{DS}<V_{Dsat}$ (can NOT neglect V_{DS}^2 term).

"Capacitor-Like" Model for Q_N

But what about the saturation region?

For $V_{DS}>V_{dsat}$ the voltage drop across our channel is V_{Dsat} with the remaining voltage (V_{DS}-V_{Dsat}) dropped across the pinch-off region

$$I_D = I_{Dsat} = \frac{Z\overline{\mu_n}C_{ox}}{L}\left[(V_{GS}-V_T)V_{Dsat} - \frac{V_{Dsat}^2}{2}\right] \qquad V_{Dsat} \le V_{DS}$$

But the charge at the end of the channel is zero due to the pinched off channel,

$$Q_N(y=L) \cong -C_{ox}\left(V_{GS}-V_T-V_{Dsat}\right) = 0$$

or

$$\boxed{V_{GS}-V_T = V_{Dsat}}$$

Thus,

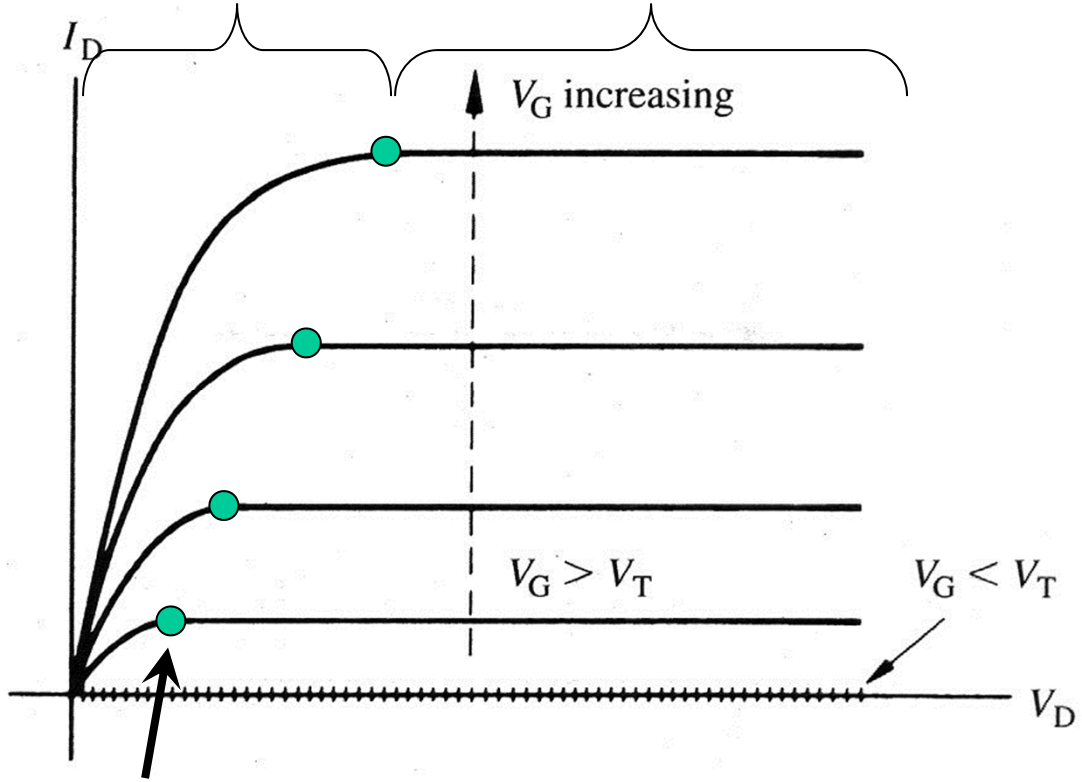
$$\boxed{I_D = I_{Dsat} = \frac{Z\overline{\mu_n}C_{ox}}{2L}\left[(V_{GS}-V_T)^2\right] \qquad V_{Dsat} \le V_{DS}}$$

MOS Transistor I-V Derivation
Summary of MOSFET IV Relationship

$$I_D = \frac{Z\overline{\mu_n}C_{ox}}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$0 \le V_{DS} \le V_{Dsat} \quad and \quad V_{GS} \ge V_T$$

$$I_D = I_{Dsat} = \frac{Z\overline{\mu_n}C_{ox}}{2L}\left[(V_{GS} - V_T)^2\right] \qquad V_{Dsat} \le V_{DS}$$



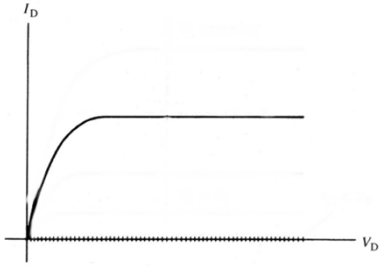
$$V_{Dsat} = V_{GS} - V_T$$

Voltage variable Resistor

An n-channel MOSFET has a gate width to length ratio of Z/L=100, $\bar{u}_n$=200 cm^2/Vsec, Cox=0.166 uF/cm^2 and V_T=1V. We want to develop a resistor that has a resistance that is controlled by an external voltage. Such a device would be used in "variable gain amplifiers", "automatic gain control devices", "compressors" and many other electronic devices. Define what range of V_{DS} must be maintained to achieve proper "voltage variable resistance" operation. Find the "On-resistance" (V_{DS}/I_D) of the transistor from 1.5V<V_{GS}<4Vfor small V_{DS} .

First, to achieve voltage variable resistance operation, we must operate in the linear region. Otherwise, the current is either a constant regardless of drain voltage (saturation region) or is approximately zero (cutoff due to the capacitor being in either accumulation and depletion).

Thus, V_{GS} -V_T>V_{DS}. Given the values above, 0<V_{DS}<0.5V



Continued...

Voltage variable Resistor

Using the linear region I_D equation:

$$I_D = \frac{Z\overline{\mu_n}C_{ox}}{L}\left[(V_{GS}-V_T)V_{DS}-\frac{V_{DS}^2}{2}\right] \approx \frac{Z\overline{\mu_n}C_{ox}}{L}\left[(V_{GS}-V_T)V_{DS}\right] \quad \text{for small } V_{DS}$$

$$R_{DS} = \frac{V_{DS}}{I_D} = \frac{V_{DS}}{\frac{Z\overline{\mu_n}C_{ox}}{L}\left[(V_{GS}-V_T)V_{DS}\right]} = \frac{L/Z}{\overline{\mu_n}C_{ox}\left[(V_{GS}-V_T)\right]}$$

$$R_{DS} = \frac{0.01}{200\left(0.166e-6F/cm^2\right)\left[(V_{GS}-1)\right]}$$

Thus,

$$100\ \Omega \le R_{DS} \le 600\ \Omega$$

Current Source

The same transistor is to be used for a "Current Source". Define the range of drain-source voltage that can be used to achieve a fixed current of 50 uA.

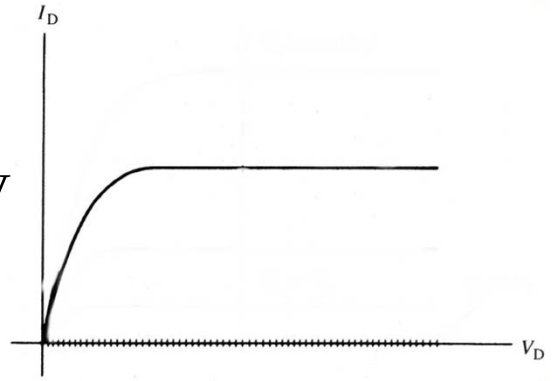
For a constant current regardless of Drain-Source voltage, we must use the saturation region:

$$I_D = I_{Dsat} = \frac{Z\overline{\mu_n} C_{ox}}{2L}\left[\left(V_{GS} - V_T\right)^2\right] \qquad V_{Dsat} \le V_{DS}$$

$$50uA = \frac{100\left(200cm^2/VSec\right)0.166uF/cm^2}{2}\left(V_{GS} - 1\right)^2$$

$$V_{GS} = 1.173V$$

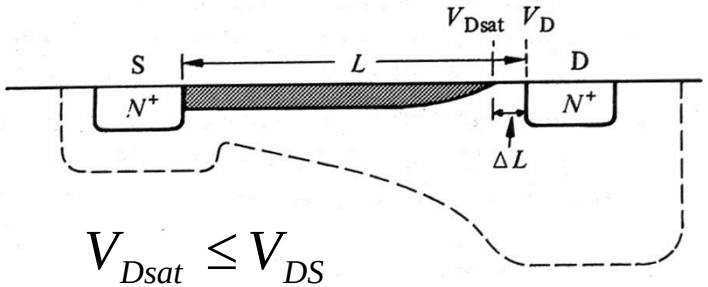
This source will operate over a $V_{DS} > V_{GS} - V_T$ or $V_{DS} > 0.173$ V



MOS Transistor: Deviations From Ideal

Channel Length Modulation Effect

Above "pinch-off" (when $V_{DS}>V_{Dsat}=V_{GS}-V_T$) the channel length reduces by a value ΔL.



Thus, the expression for drain current,

$$I_D = I_{Dsat} = \frac{Z\overline{\mu_n}C_{ox}}{2L}\left[\left(V_{GS}-V_T\right)^2\right] \qquad V_{Dsat} \le V_{DS}$$

Becomes,

$$I_D = I_{Dsat} = \frac{Z\overline{\mu_n}C_{ox}}{2\left(L-\Delta L\right)}\left[\left(V_{GS}-V_T\right)^2\right] \qquad V_{Dsat} \le V_{DS}$$

or since* $\Delta L \langle L$, $\quad \frac{1}{L-\Delta L} \cong \frac{1}{L}\left(1+\frac{\Delta L}{L}\right)$

$$I_D = I_{Dsat} = \frac{Z\overline{\mu_n}C_{ox}}{2L}\left[\left(V_{GS}-V_T\right)^2\right]\left(1+\frac{\Delta L}{L}\right) \qquad V_{Dsat} \le V_{DS}$$

*In many modern devices, this assumption does not hold. Thus, the channel length modulation parameter we are deriving does not describe the IV expressions well.

MOS Transistor: Deviations From Ideal

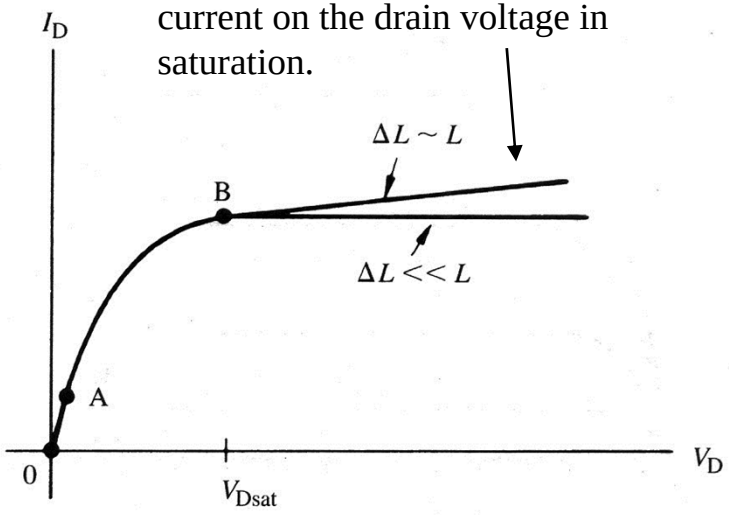
Channel Length Modulation Effect

But the fraction of the channel that is pinched off depends linearly on V_{DS} because the voltage across the pinch-off region is $(V_{DS}-V_{Dsat})$ so,

$$\frac{\Delta L}{L} = \lambda V_{DS}$$

where λ is known as the ***Channel-Length Modulation parameter*** and is typically:
$0.001\ V^{-1} < \lambda < 0.1\ V^{-1}$

Channel Length Modulation causes the dependence of drain current on the drain voltage in saturation.

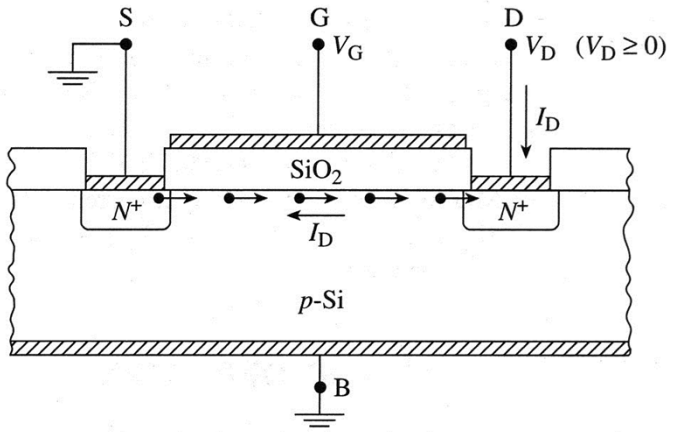


$$I_D = I_{Dsat} = \frac{Z\overline{\mu_n} C_{ox}}{2L}\left[(V_{GS} - V_T)^2\right](1+\lambda V_{DS}) \qquad V_{Dsat} \le V_{DS}$$

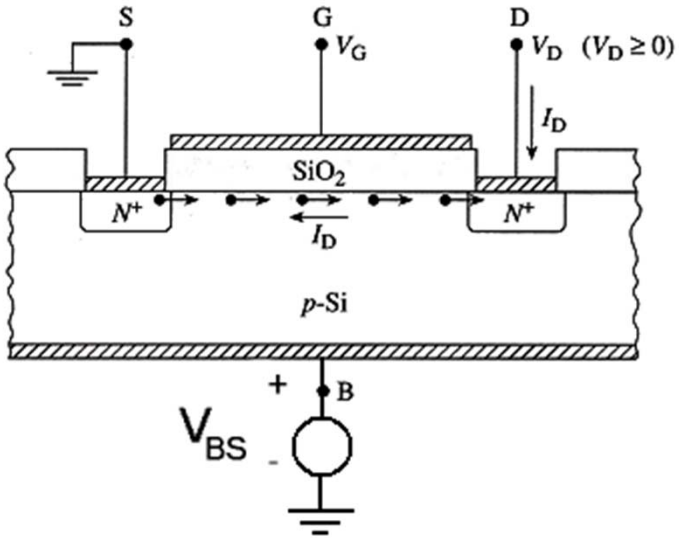
MOS Transistor: Deviations From Ideal

Body Effect (Substrate Biasing)

Until now, we have only considered the case where the substrate (Body) has been grounded….



…but the substrate (Body) is often intentionally biased such that the Source-Body and Drain-Body junctions are reversed biased.



The body bias, V_{BS}, is known as the ***backgate bias*** and can be used to modify the threshold voltage.

Note that now our channel potential has an offset equal to V_{BS}, ….

MOS Transistor: Deviations From Ideal

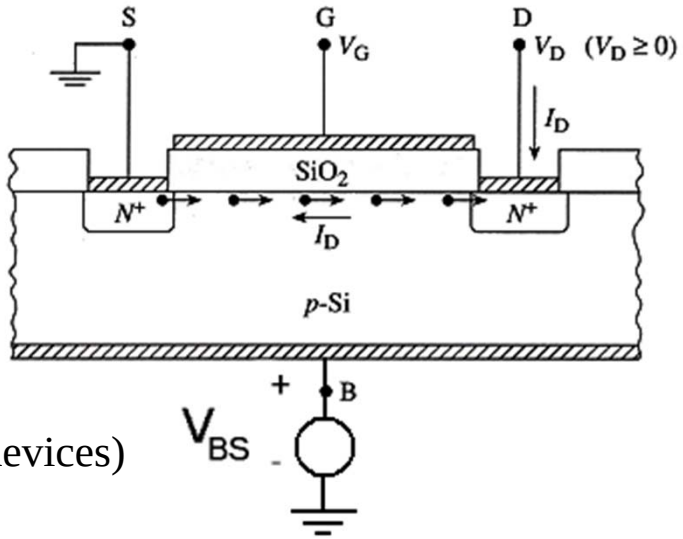
Body Effect (Substrate Biasing)

Thus, our threshold potential with the body grounded,

$$V_T = 2\phi_F + \frac{\varepsilon_S}{C_{ox}}\sqrt{\frac{2qN_A}{\varepsilon_S}(2\phi_F)} \quad \text{(for n - channel devices)}$$

$$V_T = 2\phi_F - \frac{\varepsilon_S}{C_{ox}}\sqrt{\frac{2qN_D}{\varepsilon_S}(-2\phi_F)} \quad \text{(for p - channel devices)}$$

Surface Potential ϕ_S



The Gate- Body Threshold becomes,

$$V_{GB|_{Threshold}} = 2\phi_F - V_{BS} + \frac{\varepsilon_S}{C_{ox}}\sqrt{\frac{2qN_D}{\varepsilon_S}(2\phi_F - V_{BS})} \quad \text{(for p - channel devices)}$$

$$V_{GB|_{Threshold}} = 2\phi_F - V_{BS} - \frac{\varepsilon_S}{C_{ox}}\sqrt{\frac{2qN_A}{\varepsilon_S}(-2\phi_F + V_{BS})} \quad \text{(for n - channel devices)}$$

But we would like to have this in terms of V_{GS} instead of V_{GB}.

Since, $V_{GS} = V_{GB} + V_{BS}$

$$V_T = \begin{cases} V_{GS|_{Threshold}} = 2\phi_F + \frac{\varepsilon_S}{C_{ox}}\sqrt{\frac{2qN_A}{\varepsilon_S}(2\phi_F - V_{BS})} & \text{(for n - channel devices)} \\ V_{GS|_{Threshold}} = 2\phi_F - \frac{\varepsilon_S}{C_{ox}}\sqrt{\frac{2qN_D}{\varepsilon_S}(-2\phi_F + V_{BS})} & \text{(for p - channel devices)} \end{cases}$$

MOS Transistor: Deviations From Ideal

Body Effect (Substrate Biasing)

This can be rewritten in the following form (more convenient to reference the threshold voltage to the V_{BS}=0 case).

$$V_T(Pierret) = V_{TN}(Jaeger) = V_{TO} + \gamma\left(\sqrt{(2\phi_F - V_{BS})} - \sqrt{2\phi_F}\right) \quad \text{(for n - channel devices)}$$

$$V_T(Pierret) = V_{TP}(Jaeger) = V_{TO} - \gamma\left(\sqrt{(2\phi_F + V_{BS})} - \sqrt{2\phi_F}\right) \quad \text{(for p - channel devices)}$$

where,

$$\gamma = \frac{\sqrt{2qN_A\varepsilon_S}}{C_{ox}}$$ is known as the ***body effect parameter***

MOS Transistor:

Enhancement Mode verses Depletion Mode MOSFET

We have been studying the “enhancement mode” MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor). It is called “enhancement” because conduction occurs only after the channel conductance is “improved” or “enhanced”. In this case,

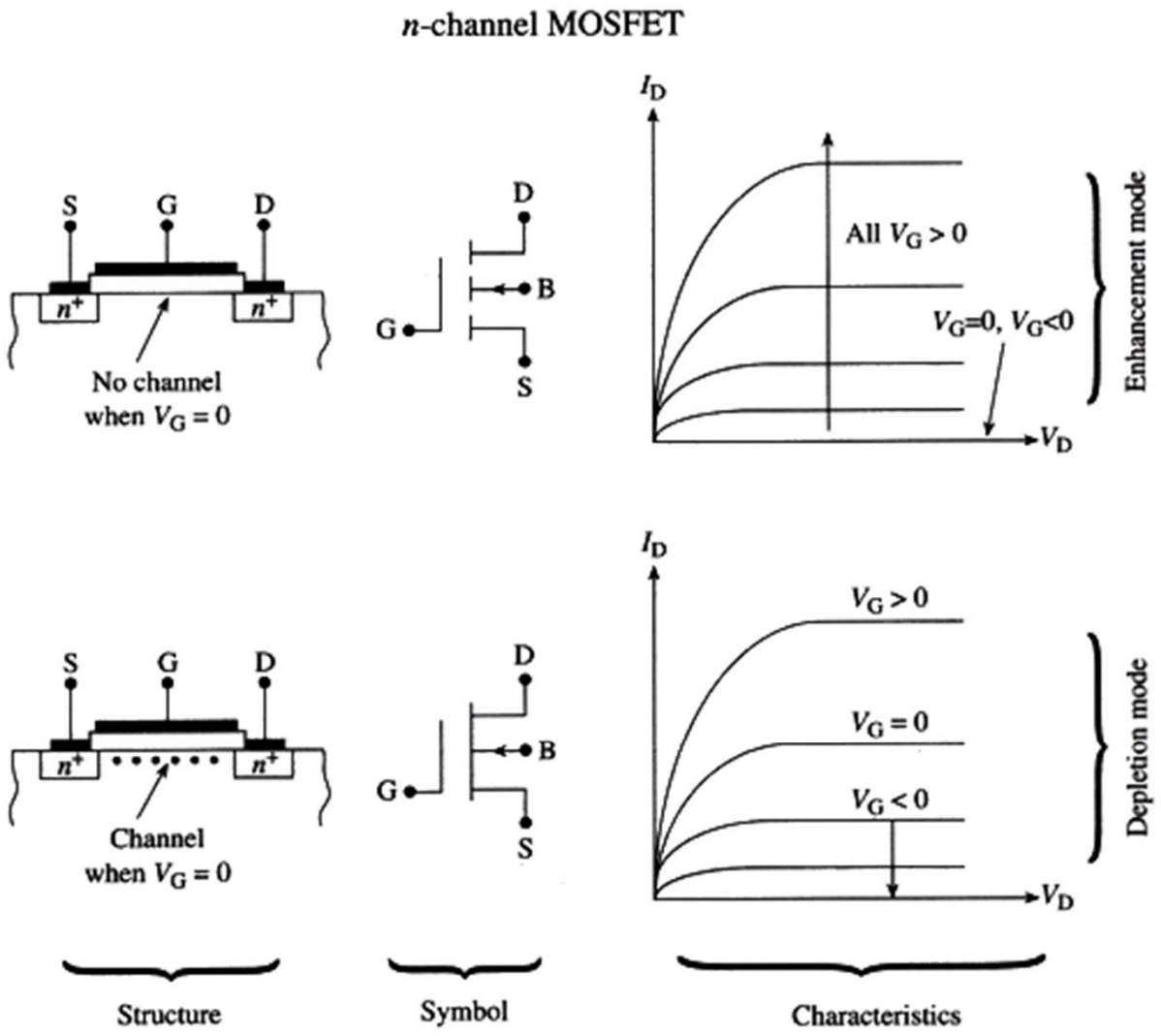
$V_{TN}>0$ and $V_{TP}<0$

Transistors can be fabricated such that: $V_{TN} \leq 0$ and $V_{TP} \geq 0$

These transistors have conduction for $V_{GS}=0$ due to a channel already existing without the need to “invert the near surface region”. To modulate currents, a field must applied to the gate that depletes the channel. Thus, transistors of this nature are called “Depletion mode MOSFETs”.

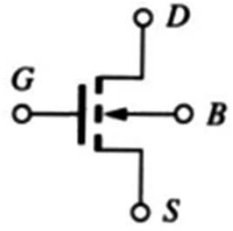
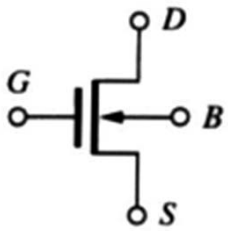
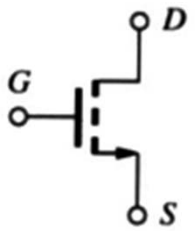
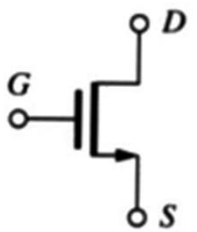
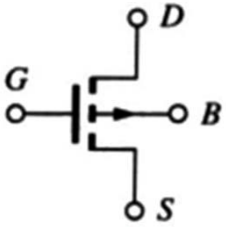
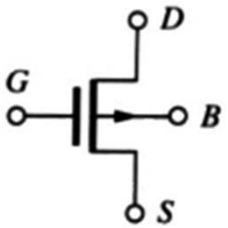
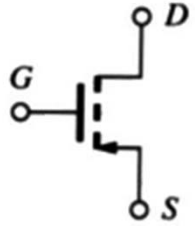
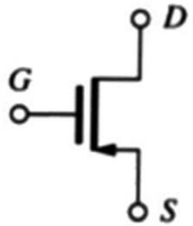
MOS Transistor:

Enhancement Mode verses Depletion Mode MOSFET



MOSFET operational modes. $V_G = 0$ channel status, circuit symbol, and I_D–V_D characteristics of n-channel enhancement-mode and depletion-mode MOSFETs.

MOS Transistor: Summary

	4-Terminal		3-Terminal	
	Enhancement	**Depletion**	**Enhancement**	**Depletion**
NMOS (n-channel)				
PMOS (p-channel)				

Jaeger uses the notation:

NMOS

$K_n = K_n' \frac{W}{L} = \overline{\mu_n}\, C_{ox} \frac{W}{L}$ where W is the Gate Width (Z in Pierret)

PMOS

$K_p = K_p' \frac{W}{L} = \overline{\mu_p}\, C_{ox} \frac{W}{L}$ where W is the Gate Width (Z in Pierret)

MOS Transistor: Summary

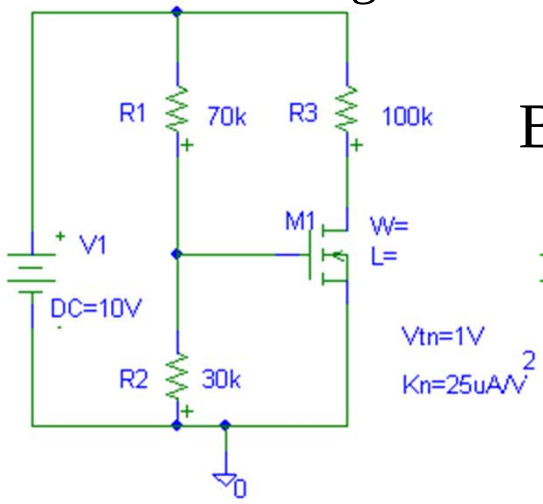
	NMOS	**PMOS**
Regardless of Mode	$K_n = K_n' \frac{W}{L} = \overline{\mu_n}\, C_{ox} \frac{W}{L}$ (Note : W = Z in Pierret)	$K_p = K_p' \frac{W}{L} = \overline{\mu_p}\, C_{ox} \frac{W}{L}$ (Note : W = Z in Pierret)
Cutoff	$I_{DS} = 0 \qquad for\ V_{GS} \le V_{TN}$	$I_{DS} = 0 \qquad for\ V_{GS} \ge V_{TP}$
Linear	$I_{DS} = \frac{Z\overline{\mu_n} C_{ox}}{L}\left[(V_{GS} - V_{TN})V_{DS} - \frac{V_{DS}^2}{2}\right]$ $V_{GS} \ge V_{TN} \quad and \quad V_{GS} - V_{TN} \ge V_{DS} \ge 0$	$I_D = \frac{Z\overline{\mu_n} C_{ox}}{L}\left[(V_{GS} - V_{TP})V_{DS} - \frac{V_{DS}^2}{2}\right]$ $V_{GS} \le V_{TP} \quad and \quad \lvert V_{GS} - V_{TP}\rvert \ge \lvert V_{DS}\rvert \ge 0$
Saturation	$I_{DS} = \frac{Z\overline{\mu_n} C_{ox}}{2L}\left[(V_{GS} - V_{TN})^2\right](1 + \lambda\ V_{DS})$ $V_{GS} \ge V_{TN} \quad and \quad V_{DS} \ge V_{GS} - V_{TN} \ge 0$	$I_{DS} = \frac{Z\overline{\mu_n} C_{ox}}{2L}\left[(V_{GS} - V_{TP})^2\right](1 + \lambda\ \lvert V_{DS}\rvert)$ $V_{GS} \le V_{TP} \quad and \quad \lvert V_{DS}\rvert \ge \lvert V_{GS} - V_{TP}\rvert \ge 0$
Threshold Voltage	$V_{TN} = V_{TO} + \gamma\left(\sqrt{(2\phi_F + V_{SB})} - \sqrt{2\phi_F}\right)$	$V_{TP} = V_{TO} - \gamma\left(\sqrt{(2\phi_F + V_{BS})} - \sqrt{2\phi_F}\right)$
V_T for Enhancement Mode	$V_{TN} > 0$	$V_{TP} < 0$
V_T for Depletion Mode	$V_{TN} \le 0$	$V_{TP} \ge 0$

MOS Transistor:

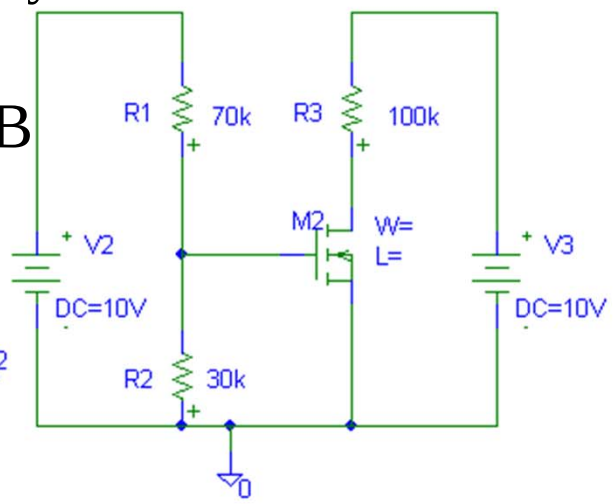
Bias Circuitry-Enhancement Mode NMOS

Due to zero DC current flow in the gate, the bias analysis of a MOSFET is significantly easier than a BJT.

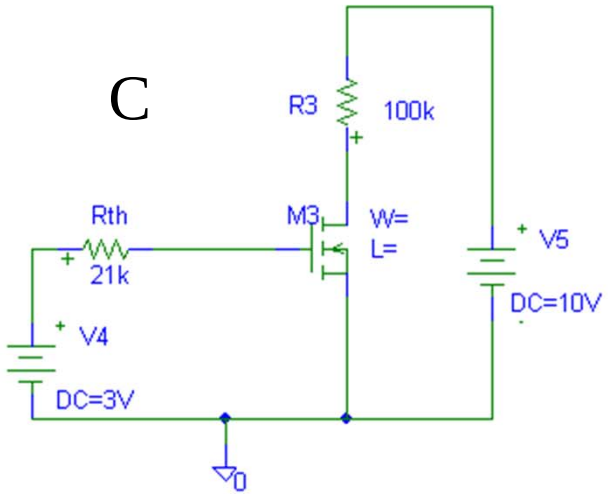
A



B



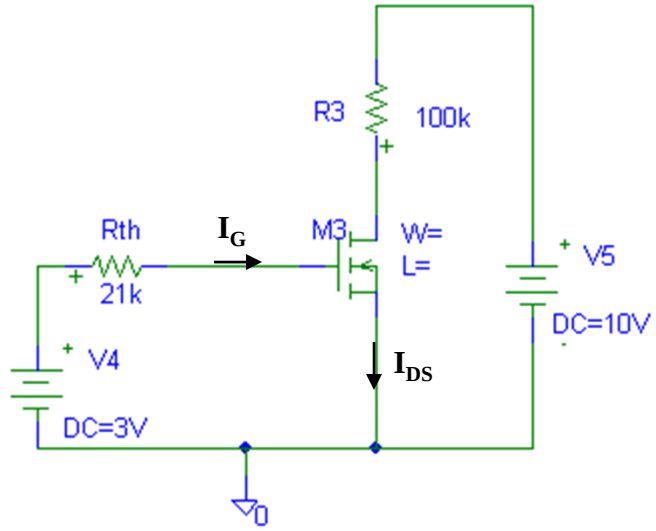
C



•Form Thevenin circuits looking out the gate, drain, and source

MOS Transistor:
Bias Circuitry-Enhancement Mode NMOS

$$3V = I_G R_{th} + V_{GS}$$
$$10V = I_{DS} R3 + V_{DS}$$



•But I_G=0 so V_{GS}=3V

•Assume Saturation operation (selected for easy math because I_{DS} does not depend on V_{DS} since no γ was given – γ=0):

$$i_{DS} = \frac{K_n}{2}\left[(v_{GS} - V_{TN})^2\right] \text{ for } \quad v_{DS} \geq v_{GS} - V_{TN} \geq 0$$

$$i_{DS} = \frac{25x10^{-6}}{2}\left[(3-1)^2\right] = 50\mu\ A$$

Check V_{DS}

$$10V = 50uA(100k) + V_{DS}$$

$$V_{DS} = 5V > V_{GS} - V_{TN} = 2V$$

•Assumption of Saturation operation was correct! If it were not correct simply make another assumption (I.e. linear region) and resolve.

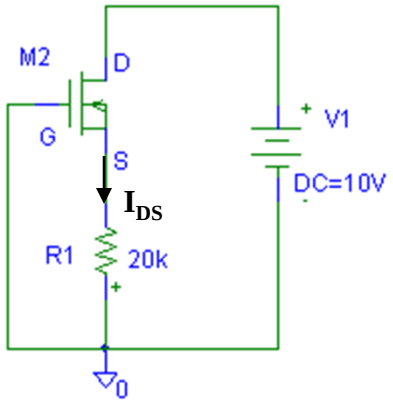
MOS Transistor:
Bias Circuitry-Depletion Mode NMOS

•Bias circuit of a depletion mode device is much simpler due to the fact that the device conducts drain current for V_{GS}=0V

$$V_{TO} = -3V$$

$$\gamma = 0\sqrt{V}$$

$$K_n = 200 \ uA/V^2$$



•What value of R1 results in 100 uA drain current?

•Again Assuming saturation:

$$i_{DS} = \frac{K_n}{2}\left[(v_{GS} - V_{TN})^2\right] \ for \quad v_{DS} \geq v_{GS} - V_{TN} \geq 0$$

$$V_{GS} = V_{TN} + \sqrt{\frac{2I_{DS}}{K_n}} = -3V + \sqrt{\frac{2\,(100uA)}{200uA/V^2}} = -2V$$

$$R1 = -\frac{V_{GS}}{I_{DS}} = -\frac{-2}{100uA} = 20 \ K\Omega$$

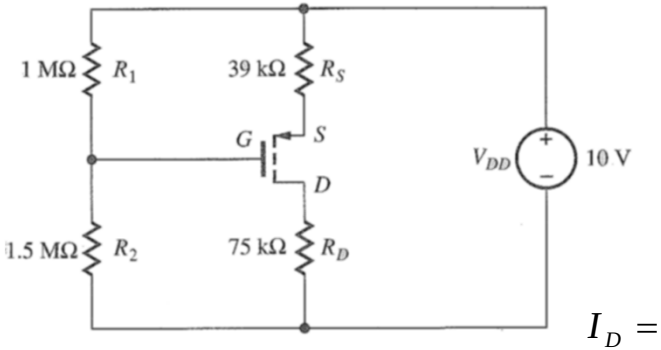
Check V_{DS}

$$10V = I_{DS}R1 + V_{DS} = 100uA(20k) + V_{DS}$$

$$V_{DS} = 8V > V_{GS} - V_{TN} = -2V - (-3V) = +1V$$

•Assumption of Saturation operation was correct! If it were not correct simply make another assumption (I.e. linear region) and resolve.

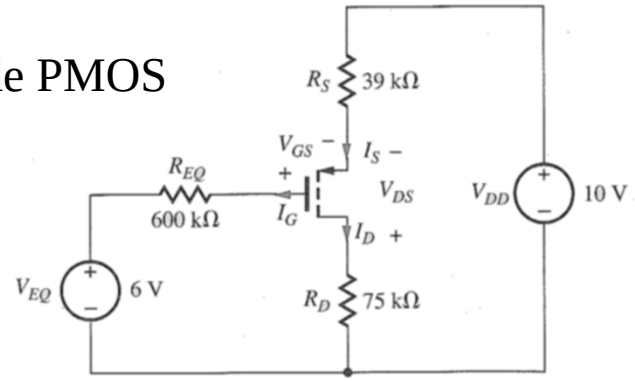
PMOS Transistor:
Bias Circuitry-Enhancement Mode PMOS



$$V_{TO} = -1V$$

$$\gamma = 0\sqrt{V}$$

$$K_p = 25 \ \ uA/V^2$$



$$I_D = I_S = \frac{Z\overline{\mu_n}C_{ox}}{2L}\left[(V_{GS} - V_{TP})^2\right](1 + \lambda \ |V_{DS}|) = \frac{K_p}{2}\left[(V_{GS} - V_{TP})^2\right]$$

$$V_{GS} \le V_{TP} \qquad and \qquad |V_{DS}| \ge |V_{GS} - V_{TP}| \ge 0$$

$$V_{EQ} = 10V\frac{1.5M}{1.5M + 1M} = 6V \quad R_{EQ} = 1M \,||\, 1.5M = 600K\Omega$$

$$V_{DD} = I_S R_S - V_{GS} + I_G R_G + V_{EQ}$$

$$V_{DD} - V_{EQ} = R_S\frac{K_p}{2}\left[(V_{GS} - V_{TP})^2\right] - V_{GS}$$

$$10 - 6 = 4 = 39{,}000\frac{25E-6}{2}\left[(V_{GS} + 1)^2\right] - V_{GS}$$

$$V_{GS}^2 - 0.051V_{GS} - 7.21 = 0 \quad \Rightarrow V_{GS} = +2.71 \, or \, -2.66V$$

$$I_D = \frac{25E-6}{2}\left[(-2.66 + 1)^2\right] = 34.4\mu A$$

$$V_{DD} = I_D R_S - V_{DS} + I_D R_D \quad \Rightarrow V_{DS} = -6.08V$$

Check V_{DS}

$$|V_{DS}| \ge |V_{GS} - V_{TP}| \ge 0 \quad \Rightarrow |-6.08| \ge |-2.66 - (-1)| \ge 0$$

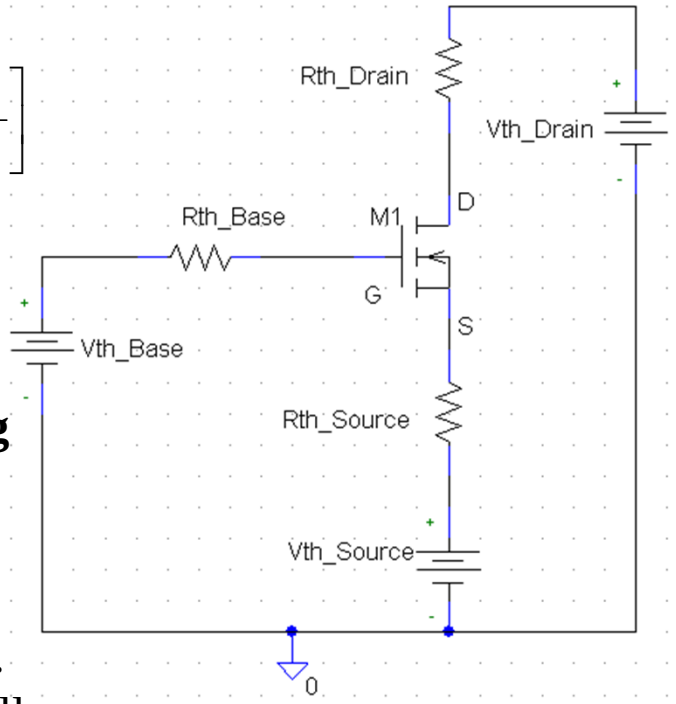
MOS Transistor:
Bias Circuitry-Possible Combinations

1) $V_{th\_Base} = V_{GS} + I_{DS}R_{th\_Source} + V_{th\_Source}$

2) $I_{DS} = \frac{K_n}{2}\left[(V_{GS} - V_{TN})^2(1+\lambda V_{DS})\right]$ *or* $I_{DS} = K_n\left[(V_{GS} - V_{TN})V_{DS} - \frac{V_{DS}^2}{2}\right]$

and optionally, **Assume either saturated or linear/triode.**

3) $V_{th\_Drain} = V_{DS} + I_{DS}\left(R_{th\_Source} + R_{th\_Drain}\right) + V_{th\_Source}$



- **Always: Solve 1) for V_{GS} and plug into 2).**
- **In certain cases, V_{DS} will need to be eliminated by using 3) solved for V_{DS} and plugged into 2).**

- Case A: Saturated, and λ=0 and no source resistor – only 1 and 2 required. Results in 1st order polynomial.
- Case B: Saturated, and λ>0 and no source resistor – all 3 equations needed. Results in 1st order polynomial.
- Case C: Saturated, and λ=0 and a source resistor – all 3 equations needed. Results in 2nd order polynomial.
- Case D: Saturated, and λ>0 and a source resistor – all 3 equations needed. Results in 3rd order polynomial.
- Case E: Linear/Triode, with or without a source resistor – all 3 equations needed. Results in 2nd order polynomial.

Useful Formulas for DC Bias Solutions

If a 3rd order polynomial results, try factoring it into a linear and quadratic term 1st. If this is not easy for your case, a longer but sure fire way is listed below.

QUADRATIC EQUATIONS

Any quadratic equation may be reduced to the form,—

$$ax^2 + bx + c = 0$$

Then

$$x = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

If a, b, and c are real then:
If $b^2 - 4ac$ is positive, the roots are real and unequal;
If $b^2 - 4ac$ is zero, the roots are real and equal;
If $b^2 - 4ac$ is negative, the roots are imaginary and unequal.

CUBIC EQUATIONS

A cubic equation, $y^3 + py^2 + qy + r = 0$ may be reduced to the form,—

$$x^3 + ax + b = 0$$

by substituting for y the value, $x - \frac{p}{3}$. Here

$$a = \tfrac{1}{3}(3q - p^2) \text{ and } b = \tfrac{1}{27}(2p^3 - 9pq + 27r).$$

For solution let,—

$$A = \sqrt[3]{-\frac{b}{2} + \sqrt{\frac{b^2}{4} + \frac{a^3}{27}}}, \qquad B = -\sqrt[3]{+\frac{b}{2} + \sqrt{\frac{b^2}{4} + \frac{a^3}{27}}},$$

then the values of x will be given by,

$$x = A + B, \quad -\frac{A+B}{2} + \frac{A-B}{2}\sqrt{-3}, \quad -\frac{A+B}{2} - \frac{A-B}{2}\sqrt{-3}.$$

If p, q, r are real, then:

If $\frac{b^2}{4} + \frac{a^3}{27} > 0$, there will be one real root and two conjugate complex roots;

If $\frac{b^2}{4} + \frac{a^3}{27} = 0$, there will be three real roots of which at least two are equal;

If $\frac{b^2}{4} + \frac{a^3}{27} < 0$, there will be three real and unequal roots.