Lecture 32

Digital Logic Gates

Reading: Jaeger 6.1-6.4 and Notes

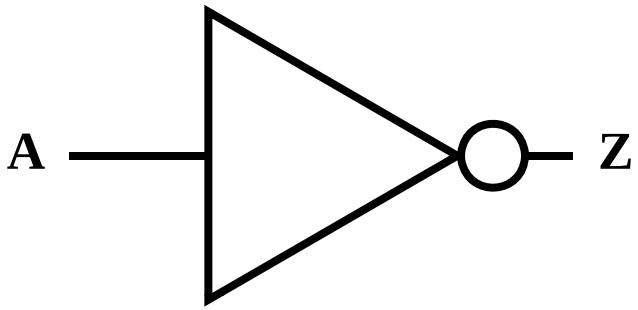
Basic Logic Gates

NOT or Inverter Gate: (Asks, is the input false?)

False=State “0”

True=State “1”

Input **Output**



Logic Function: $Z = \overline{A}$

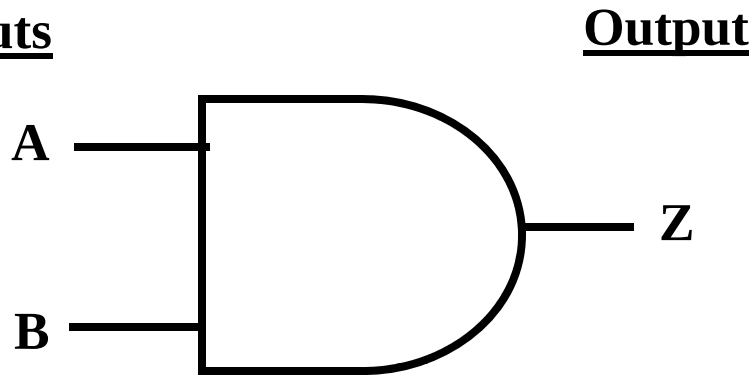
Truth Table:

Input **Output**

A	Z
0	1
1	0

Basic Logic Gates

AND Gate: (Asks, are all inputs true?)



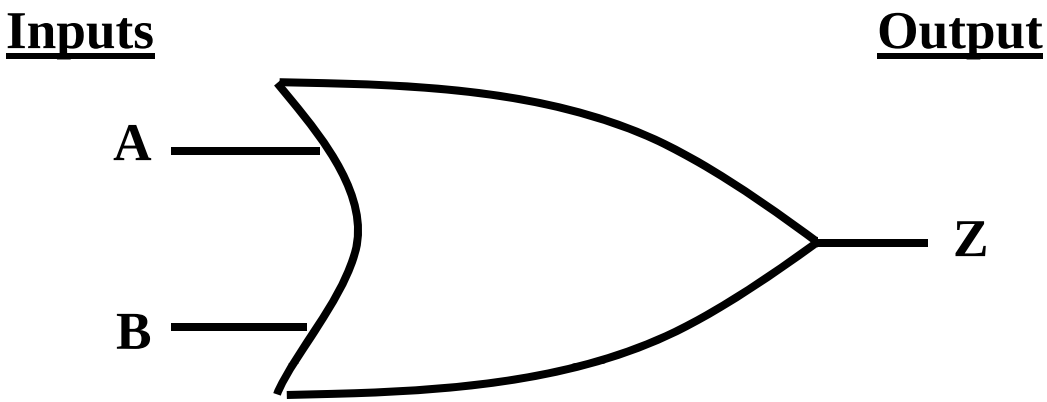
Logic Function: $Z = AB$

Truth Table:

Inputs		Output
A	**B**	**Z**
0	0	0
0	1	0
1	0	0
1	1	1

Basic Logic Gates

OR Gate: (Asks, is any input true?)



Logic Function: $Z = A + B$

Truth Table:

Inputs		Output
A	**B**	**Z**
0	0	0
0	1	1
1	0	1
1	1	1

Basic Logic Gates

Any more complex functionality can be constructed from the three basic gates by using DeMorgan's Law:

$$\overline{ABC...N} = \overline{A} + \overline{B} + \overline{C} ... + \overline{N}$$

The complement of the product is replaced with the sum of the complements

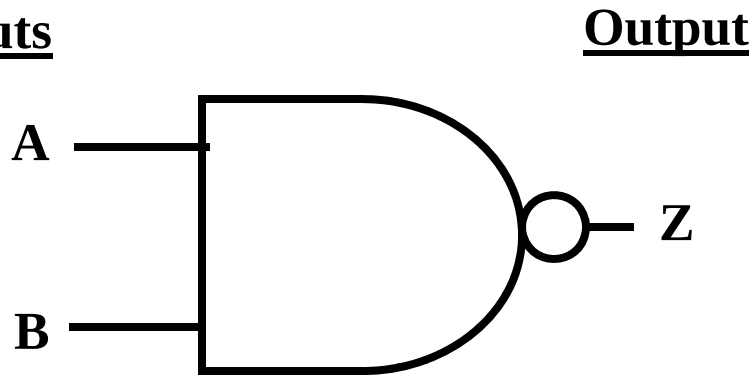
$$\overline{A + B + C + ... + N} = \overline{A}\,\overline{B}\,\overline{C}...\overline{N}$$

The complement of the sum is replaced with the product of the complements

Note: Only the AND, OR and Inverter gates are considered "Basic" logic Gates

Non-Basic Logic Gates

NAND Gate: (Asks, is any input false?)



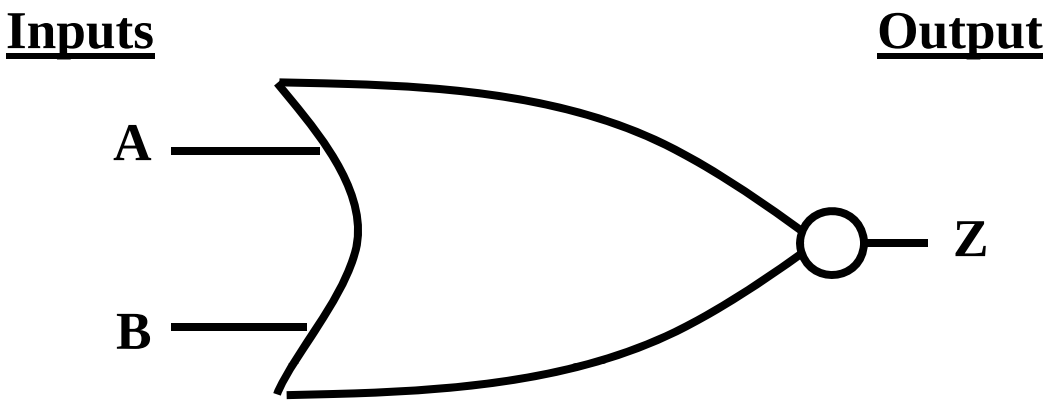
Logic Function: $Z = \overline{AB}$

Truth Table:

Inputs		Output
A	**B**	**Z**
0	0	1
0	1	1
1	0	1
1	1	0

Non-Basic Logic Gates

NOR Gate: (Asks, are all inputs false?)



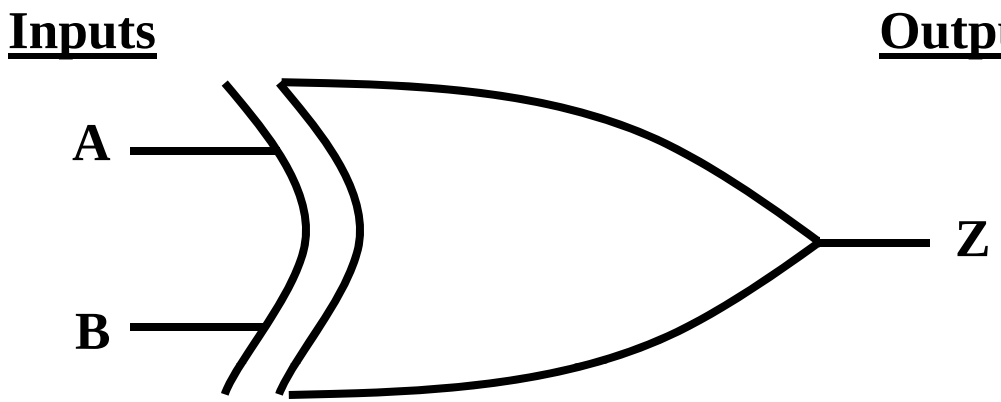
Logic Function: $Z = \overline{A + B}$

Truth Table:

Inputs		Output
A	**B**	**Z**
0	0	1
0	1	0
1	0	0
1	1	0

Non-Basic Logic Gates

XOR Gate, Exclusive OR Gate: (Asks, are the inputs not equal? Inequality test)



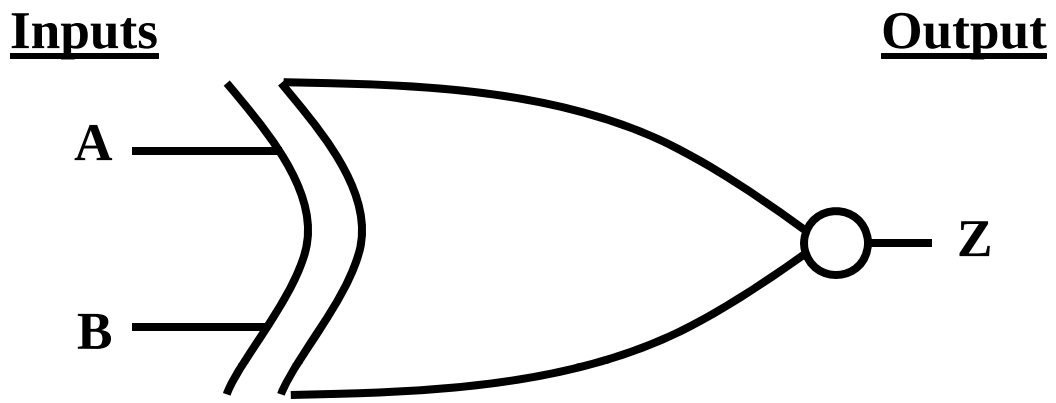
Logic Function: $Z = \overline{A}B + A\overline{B}$

Truth Table:

Inputs		Output
A	**B**	**Z**
0	0	0
0	1	1
1	0	1
1	1	0

Non-Basic Logic Gates

XNOR Gate, Exclusive NOR Gate: (Asks, are the inputs equal? An equality test)



Logic Function: $Z = \overline{\overline{A}B + A\overline{B}} = \left(\overline{A} + B\right)\left(A + \overline{B}\right)$

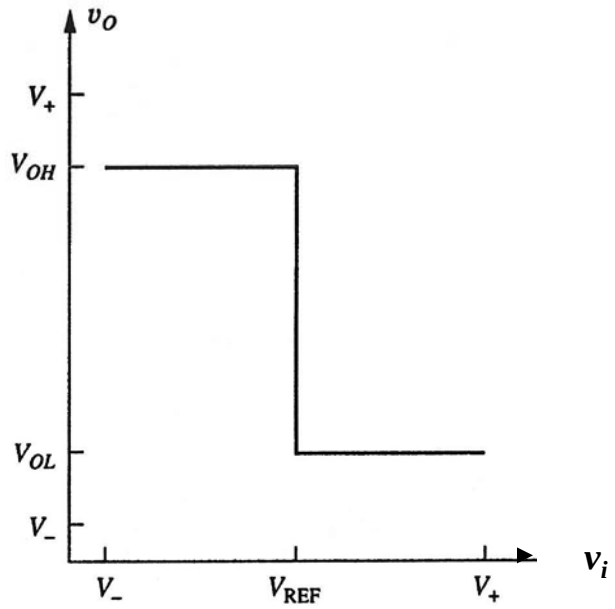
Truth Table:

Inputs		Output
A	**B**	**Z**
0	0	1
0	1	0
1	0	0
1	1	1

Ideal Inverter Characteristics

•The easiest gate to analyze is the inverter (NOT) gate. By looking at the inverter we can learn a great deal about all gate physical implementations.

•The *Voltage Transfer Characteristic* (**VTC**) of an ideal inverter is:



Definitions:

•V_{OH}=Logic state “1” or “True”. The highest possible output voltage.

•V_{OL}=Logic state “0” or “False”. The Lowest possible output voltage.

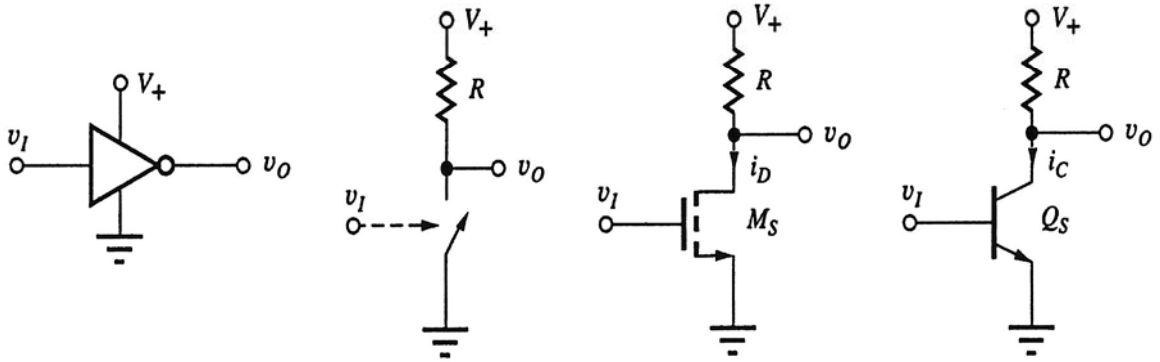
•V_{REF}=Voltage for which the inverter switches from Logic state “1” to Logic state “0”

•The transition is abrupt.

Actual Inverter Implementation

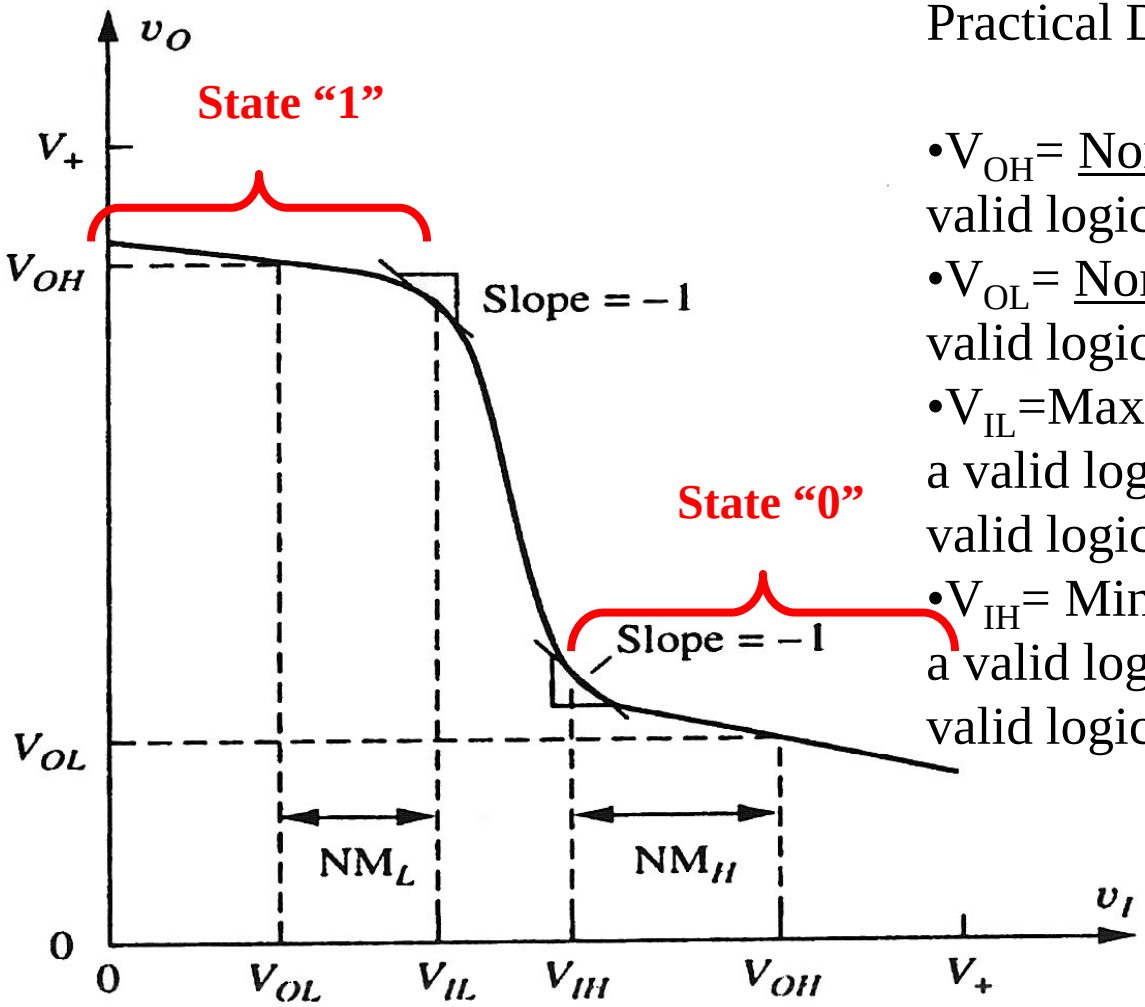
•The simplest implementation of the inverter consists of a resistor and a switch.

•The switch can be an actual switch (user interaction required) or a transistor that is electrically “turned on or off”.



Closed Switch, Vo=V_{OL}	**Vo=0V**	**Vo=V_{DS} of Ms**	**Vo=V_{CE} of Qs**
Open Switch, Vo=V_{OH}	**Vo=V+**	**Vo=V+**	**Vo=V+**

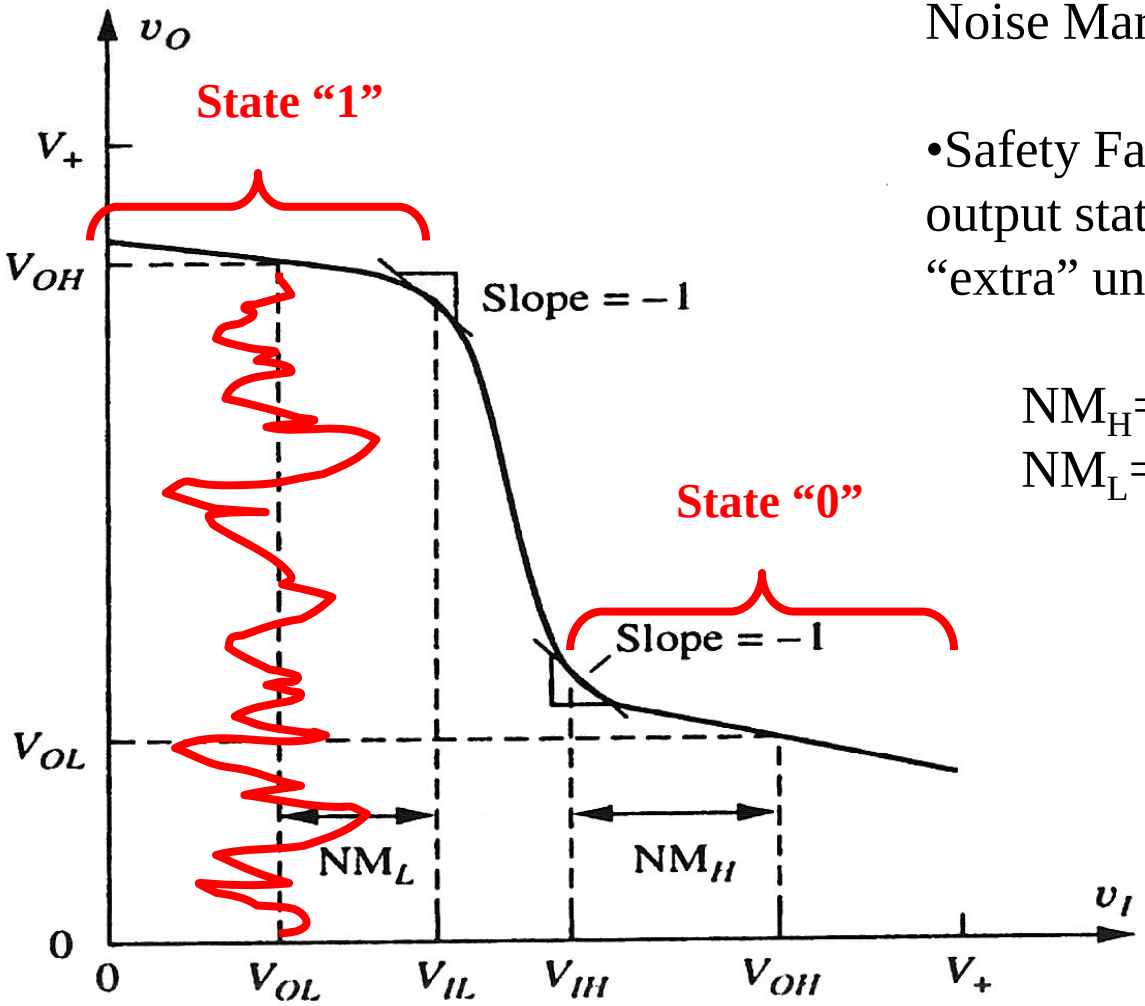
Actual Inverter Characteristics



Practical Definitions:

- V_{OH}= Nominal output voltage defining a valid logic state "1" at the output
- V_{OL}= Nominal output voltage defining a valid logic state "0" at the output
- V_{IL}=Maximum input voltage resulting in a valid logic state "0" at the input (or a valid logic state "1" at the output).
- V_{IH}= Minimum input voltage resulting in a valid logic state "1" at the input (or a valid logic state "0" at the output)

Actual Inverter Characteristics



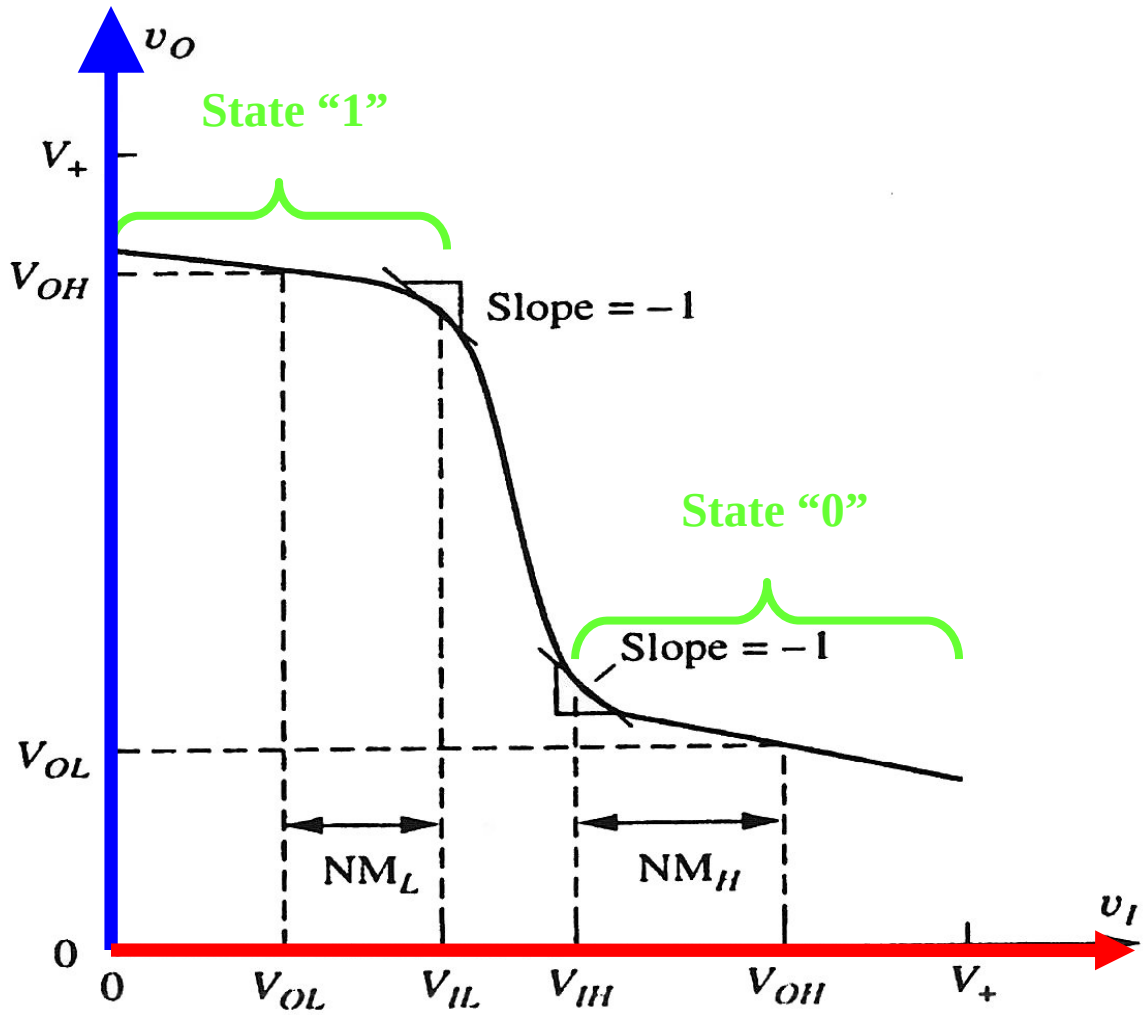
Noise Margins

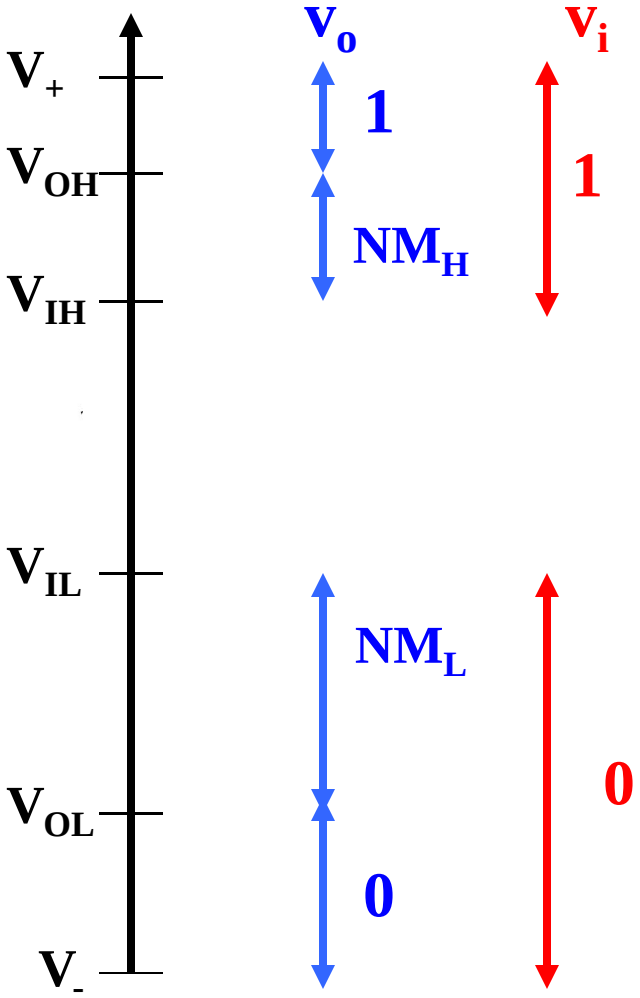
•Safety Factor to insure that the output state does not change due to "extra" unwanted signals.

$NM_H = V_{OH} - V_{IH}$

$NM_L = V_{IL} - V_{OL}$

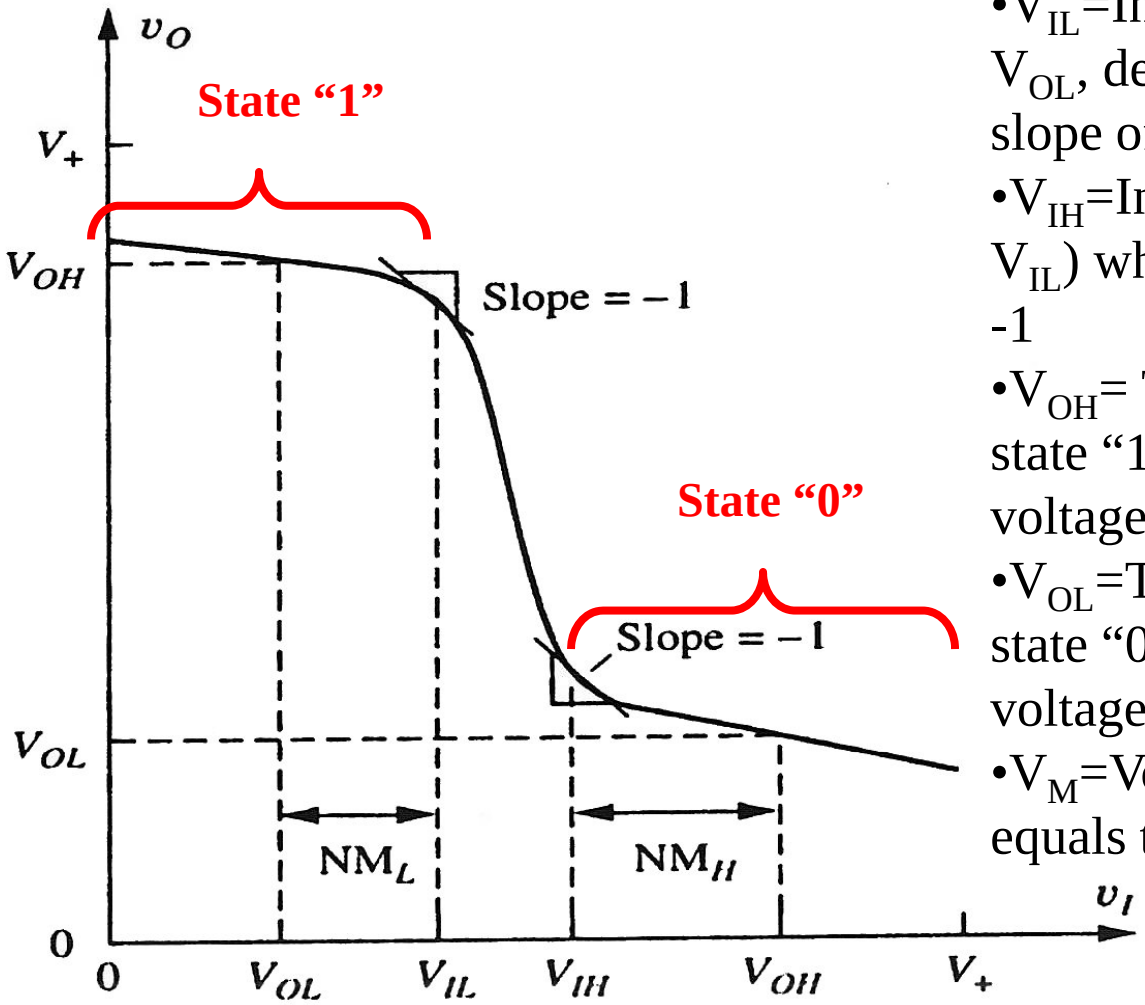
Actual Inverter Characteristics





Actual Inverter Characteristics

Actual inverter transitions from V_{OH} to V_{OL} is not abrupt.

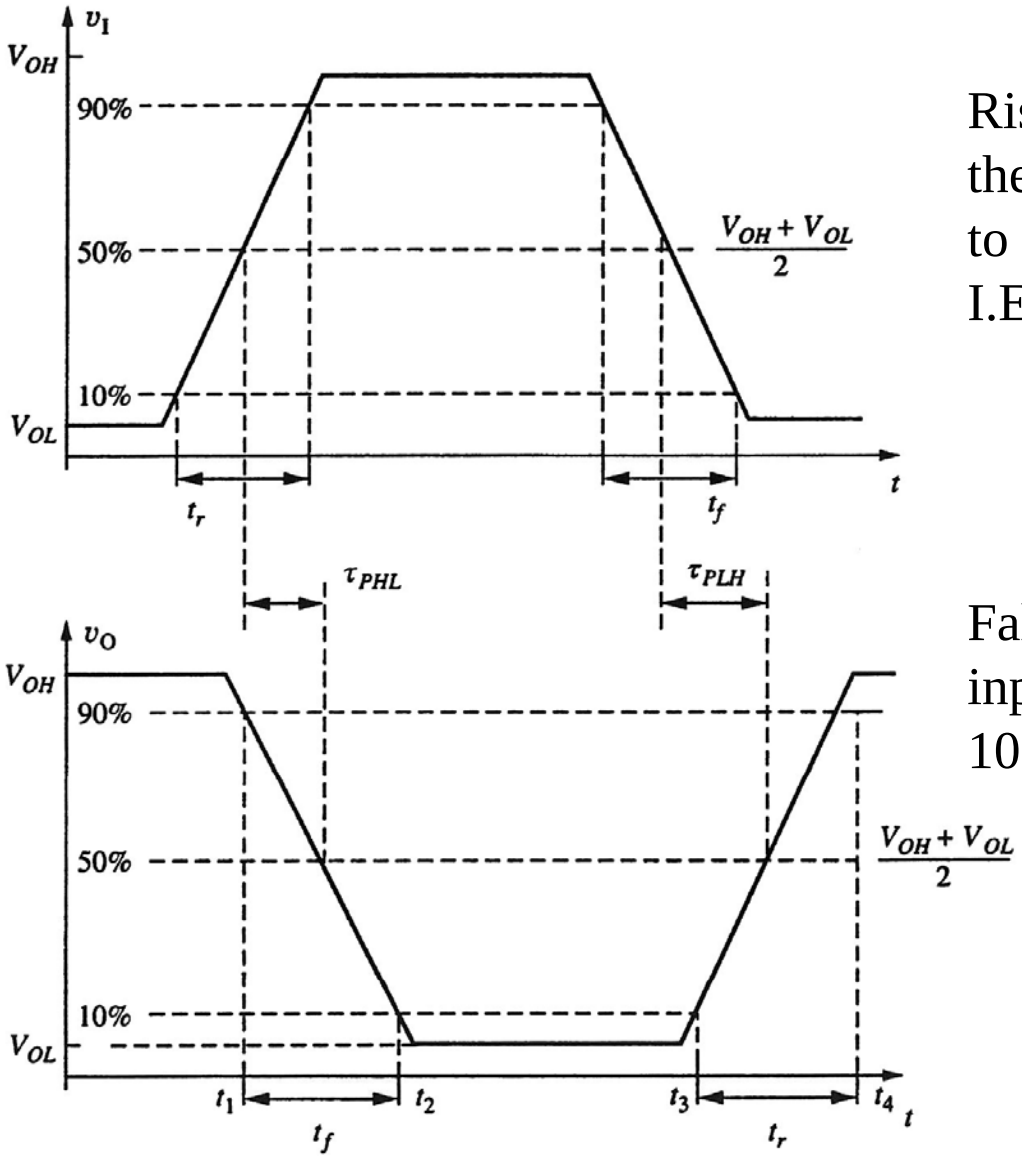


Definitions:

- V_{IL}=Input voltage value (Larger than V_{OL}, defined in a moment) where the slope of the VTC equals -1
- V_{IH}=Input voltage value (Larger than V_{IL}) where the slope of the VTC equals -1
- V_{OH}= The nominal output voltage for a state "1" at the output when the input voltage is V_{OL}
- V_{OL}=The nominal output voltage for a state "0" at the output when the input voltage is V_{OH}
- V_M=Voltage where the output voltage equals the input voltage

Inverter Time Response

State transitions require finite amounts of time to occur. Thus, we can characterize the Rise, and Fall of the signals by:



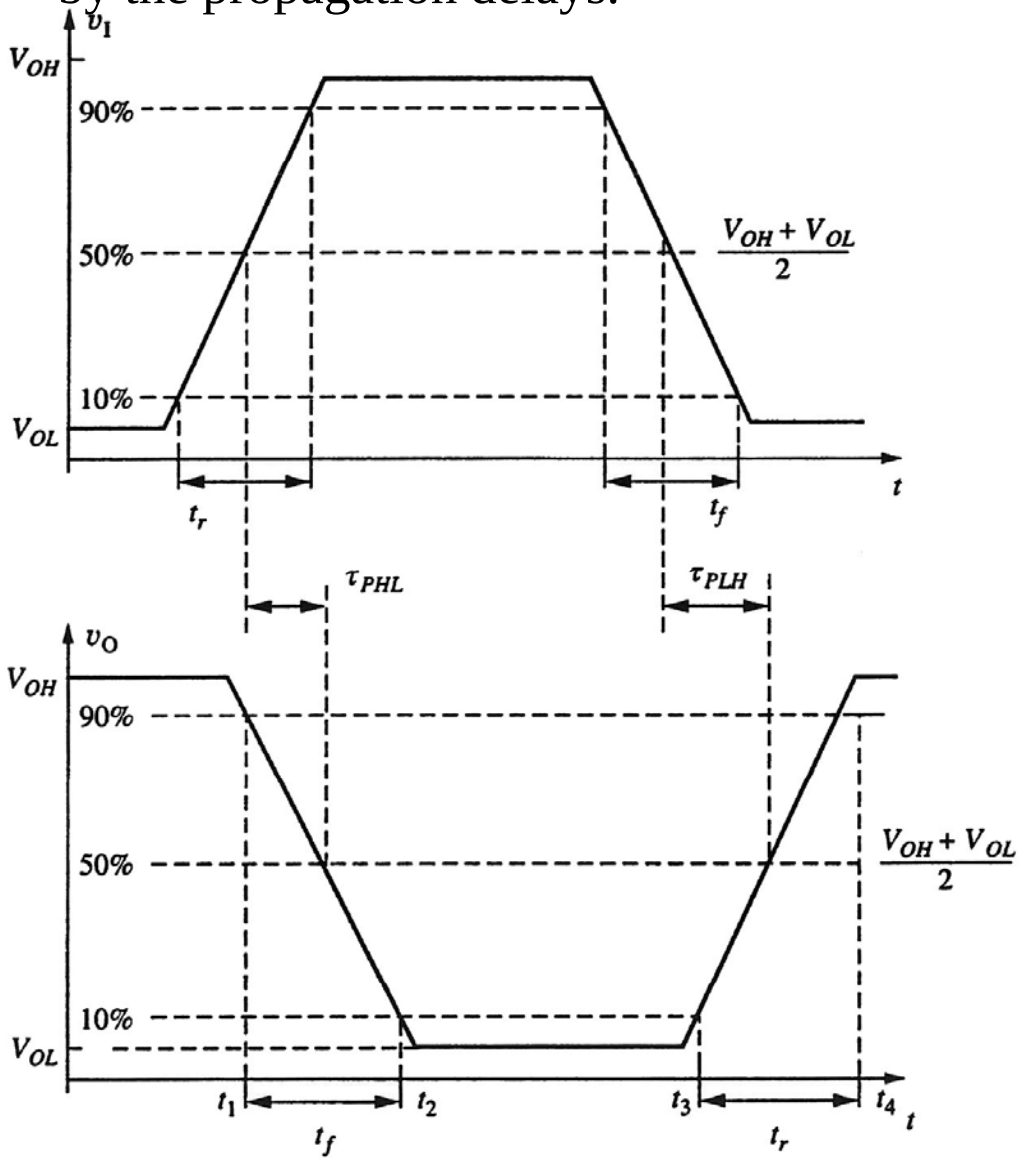
Rise Time, t_r, = The time required for the input/output to transition from 10% to 90% of its total voltage excursion. I.E.:

$$\Delta V = V_{OH} - V_{OL}$$
$$V_{10\%} = V_{OL} + 0.1\Delta V$$
$$V_{90\%} = V_{OL} + 0.9\Delta V$$

Fall Time, t_f, = The time required for the input/output to transition from 90% to 10% of its total voltage excursion.

Inverter Time Response

State transitions require finite amounts of time to pass from the input of the gate to the output of the gate. This "time required for a state change" can be characterized by the propagation delays.



Propagation Delay from high-to-low, τ_{PHL}, = The time delay between the 50% points on the input and output waveforms during the high-to-low output transition

Propagation Delay from low-to-high, τ_{PLH}, = The time delay between the 50% points on the input and output waveforms during the low-to-high output transition

Average Propagation Delay, $\tau_P=0.5(\tau_{PHL}+\tau_{PLH})$

The 50% points are:

$$V_{50\%}=0.5(V_{OH}+V_{OL})$$

Rise and Fall Time Dependence on Power

Since larger currents can charge a capacitor faster, high speed requires higher power (for a fixed capacitor load).

Thus, there is a fundamental tradeoff in power and speed:

Need high speed = Need higher power

Need low power operation (example battery device) = will need to operate slower.