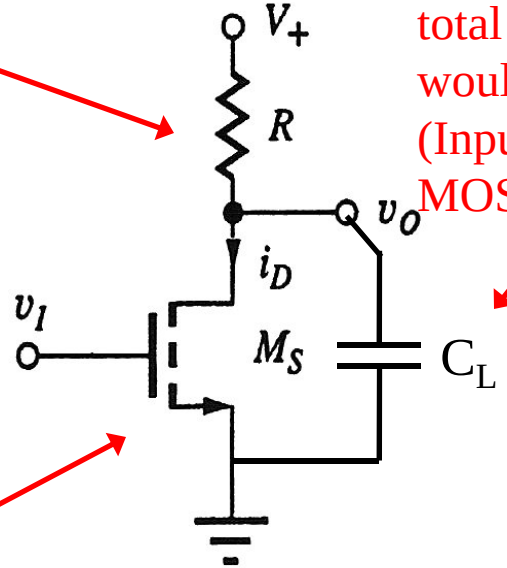
Lecture 33

Digital Logic Gates

Reading: Jaeger 6.6-6.9, 7.1-7.5 and Notes

Resistive Load Inverter

"Pull Up" Resistor provides current to Charge up the Load Capacitor, C_L



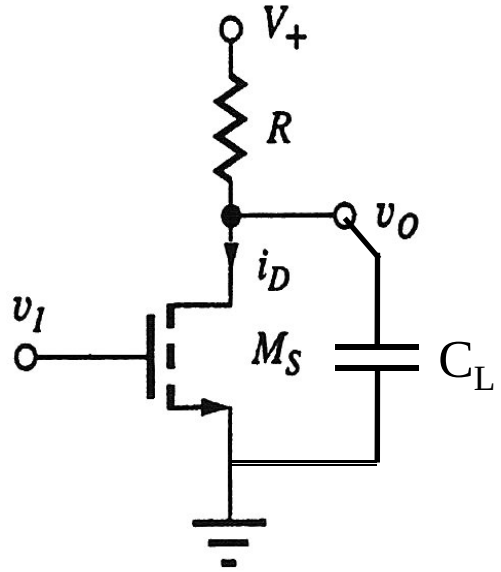
Load Capacitor, C_L, represents the total capacitance of all gates that would be connected to the output (Input capacitance's of the MOSFETS)

Switching transistor will "Pull down" the output voltage by discharging the Load Capacitor, C_l when the transistor is conducting.

Note: $V_{BS}=0$

Resistive Load Inverter

Inverter State:
Input is Low
Output is High



$$v_o = v_{DS} = V_{DD} - i_D R$$

For $v_i = v_{GS} = V_{OL} < V_T$

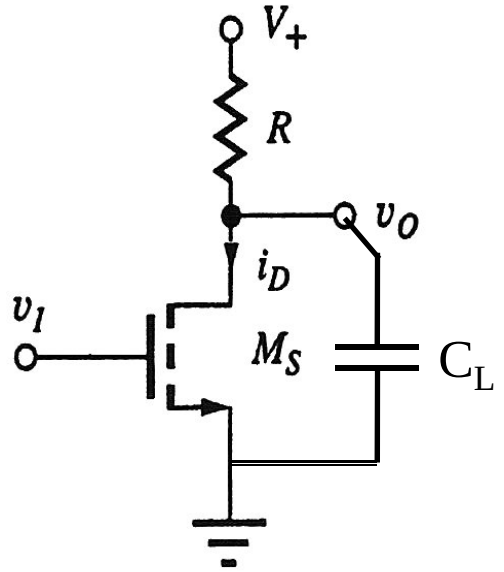
$$i_D = 0 \quad \Rightarrow \quad v_o = V_{DD} = V_{OH}$$

$V_{OL} < V_T$ is our first design criteria!

For a nominal V_T = 1, we would typically make V_{OL}~0.25V to insure adequate noise margin.

Resistive Load Inverter

Inverter State:
Input is High
Output is Low



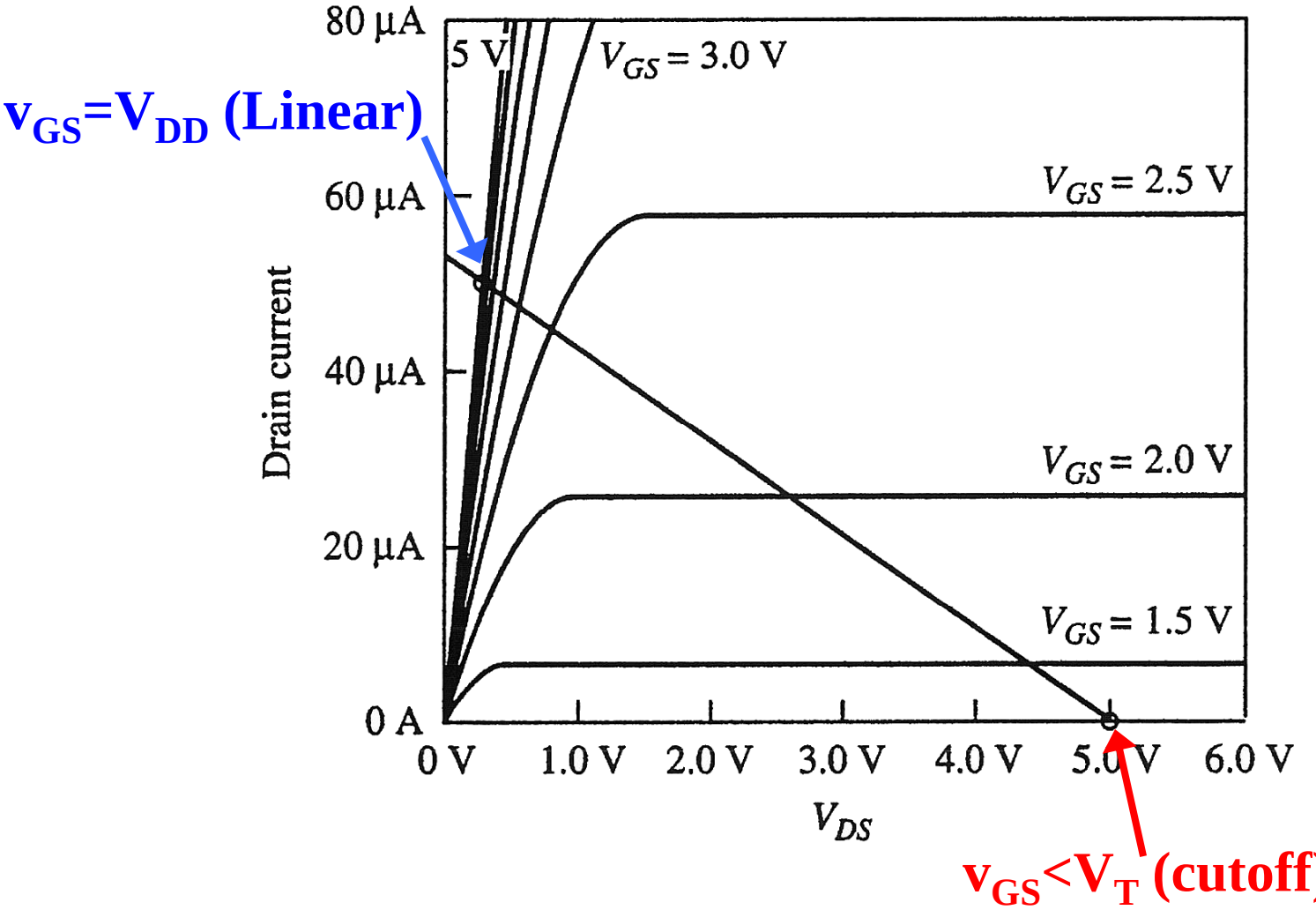
$$v_o = v_{DS} = V_{DD} - i_D R$$

For $v_i=v_{GS}=V_{OH}=V_{DD}$ from previous page, $v_o=V_{OL}$

Since $v_{GS} = V_{DD} > v_{DS} \quad \Rightarrow \quad$ *we must be in the linear region*!

Resistive Load Inverter

The MOSFET switches between the two operating points, $v_{GS}<V_T$ (cutoff) and $v_{GS}=V_{DD}$ (Linear) along a "Resistive" (linear IV characteristic) "Load Line" passing through the saturation region during the transition.



Resistive Load Inverter

Example: If we wanted the gate to dissipate 0.25 mW using a V_{TN}=1V and K_n'=25e-6 A/V^2, and having a V_{OL}=0.25V, what W/L ratio would be needed? What load resistance is required?

Since,

$$Power = V_{DD} x i_{DS}$$

$$0.25e-3 = 5 i_{DS}$$

$$i_{DS} = 50\mu A$$

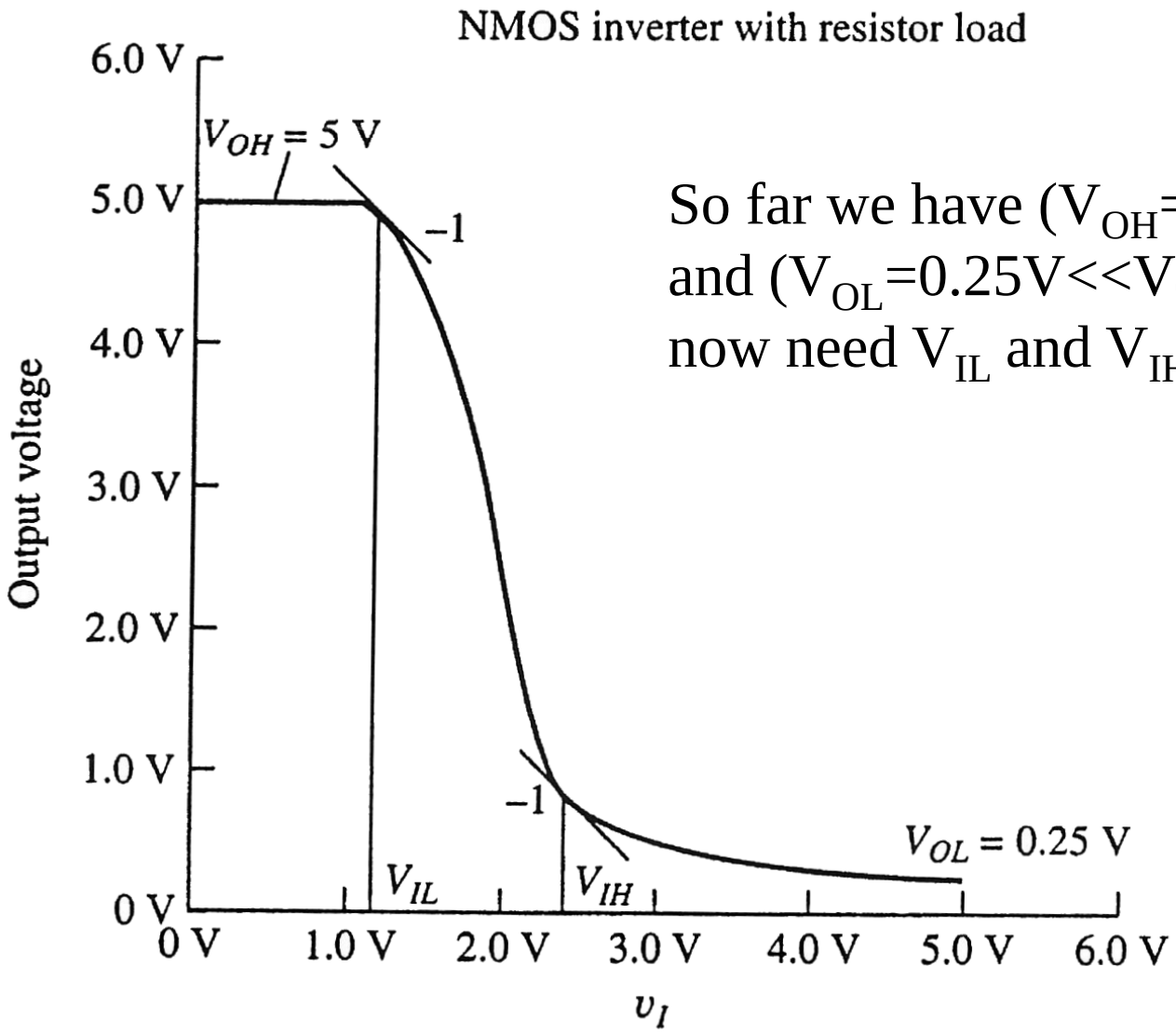
$$i_{DS} = K_n' \left(\frac{W}{L}\right)\left(v_{GS} - V_{TN} - 0.5 v_{DS}\right) v_{DS}$$

$$50e-6 = 25e-6 \left(\frac{W}{L}\right)\left(5-1-.125\right)0.25$$

$$\left(\frac{W}{L}\right) = \frac{2.06}{1}$$

$$R = \frac{V_{DD} - V_{OL}}{i_{DS}} = \frac{5-0.25}{50e-6} = 95\ K\Omega$$

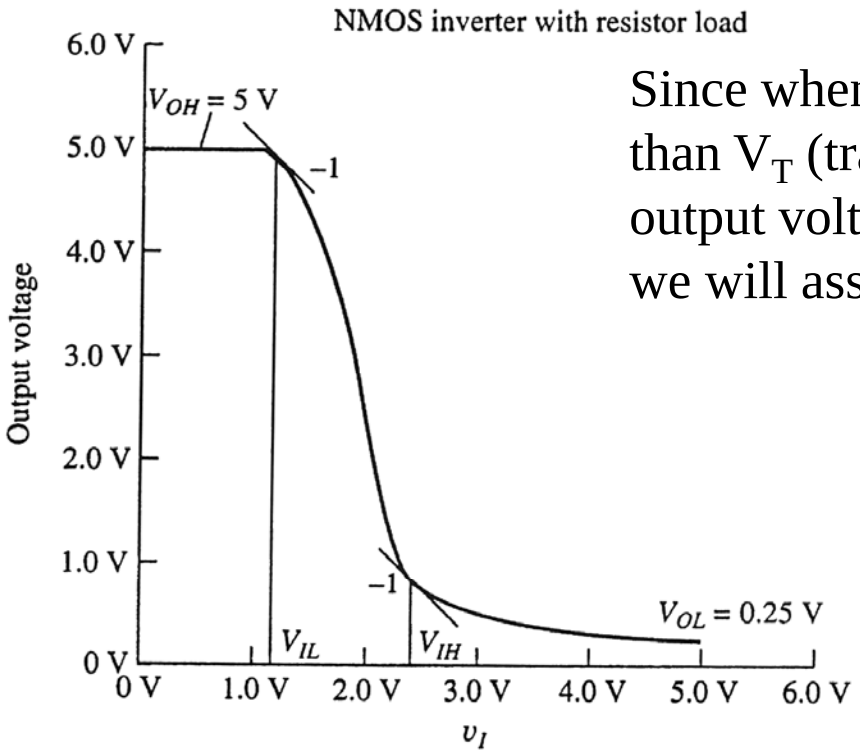
Resistive Load Inverter



So far we have (V_{OH}=5V) and (V_{OL}=0.25V<<V_T). We now need V_{IL} and V_{IH}.

Resistive Load Inverter

Calculating V_{IL}



Since when $v_i=V_{IL}$, v_{GS} is small but clearly greater than V_T (transistor is conducting as observed from the output voltage being reduced) and since v_{DS} is large, we will assume saturation.

$$i_{DS} = 0.5K_n\left(V_{GS} - V_{TN}\right)^2 \quad and \quad v_o = V_{DD} - i_{DS}R$$

$$v_o = V_{DD} - 0.5K_n\left(v_i - V_{TN}\right)^2 R$$

$$\left.\frac{dv_o}{dv_i}\right|_{v_i=V_{IL}} = -K_n\left(v_i - V_{TN}\right)R = -1$$

$$\boxed{v_i = V_{IL} = V_{TN} + \frac{1}{K_n R}}$$

Also,

$$\boxed{v_o = V_{DD} - \frac{1}{2K_n R}}$$

Inverter Transitional State:
Input is Low
Output is High

Resistive Load Inverter

Example (cont'd): For our previous example,

$$v_i = V_{IL} = V_{TN} + \frac{1}{K_n R} = 1 + \frac{1}{25\ e-6\left(\frac{2.06}{1}\right)95{,}000} = 1.2V$$

and,

$$v_o = V_{DD} - \frac{1}{2K_n R} = 5 - \frac{1}{2\left[25\ e-6\left(\frac{2.06}{1}\right)\right]95{,}000} = 4.9V$$

Verifying our assumption of Saturation:

$$v_{GS} - V_{TN} = 1.2 - 1 < v_{DS} = 4.9$$

Resistive Load Inverter

Calculating V_{IH}

Since when $v_i=V_{IH}$, v_{GS} is large and since v_{DS} is small, we will assume linear operation.

$$i_{DS} = K_n\left(v_{GS} - V_{TN} - 0.5v_{DS}\right)v_{DS} \quad and \quad v_o = V_{DD} - i_{DS}R$$

$$v_{GS} = v_i \quad and \quad v_{DS} = v_o$$

$$v_o = V_{DD} - K_n\left(v_i - V_{TN} - 0.5v_o\right)v_o R$$

$$\frac{v_o^{\,2}}{2} - v_o\left[v_i - V_{TN} + \frac{1}{K_n R}\right] + \frac{V_{DD}}{K_n R} = 0$$

$$Setting \left.\frac{dv_o}{dv_i}\right|_{v_i=V_{IH}} = -1 \; and \; solving \; for \; v_i$$

$$v_i = V_{IH} = \boxed{V_{TN} - \frac{1}{K_n R} + 1.63\sqrt{\frac{V_{DD}}{K_n R}}}$$

and,

$$\boxed{v_o = \sqrt{\frac{2V_{DD}}{3K_n R}}}$$

Inverter Transitional State:
Input is High
Output is Low

Resistive Load Inverter

Calculating V_{IH}

Example (cont'd): For our previous example,

$$V_{IH} = V_{TN} - \frac{1}{K_n R} + 1.63\sqrt{\frac{V_{DD}}{K_n R}} = 2.44V$$

and,

$$v_o = \sqrt{\frac{2V_{DD}}{3K_n R}} = 0.83V$$

Thus, our Noise Margins are:

$$NM_L = V_{IL} - V_{OL} = 1.2 - 0.25 = 0.95V$$

and,

$$NM_H = V_{OH} - V_{IH} = 5 - 2.44 = 2.56V$$

This approach is good for single gate or small numbers of gates on a chip, but the large amount of area required to make the resistors prevent it from being used for very dense digital circuits. ***We need a different approach!***

Procedure Summary

1. **Select a V_{OL}** based on a power specification or other design criteria such as noise margin, etc… This is a fairly open parameter.

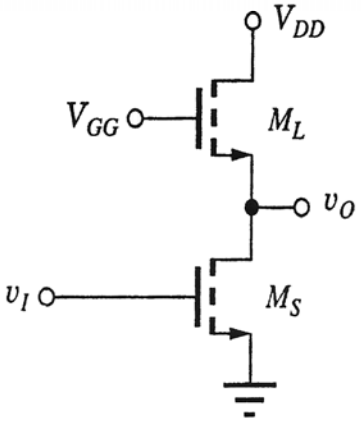
2. **Determine what V_{OH}** corresponds to this V_{OL} . When the switching transistor is off (v_i=this V_{OL}), what V_{OH} results at the output?

3. **Design the Switching Transistor for the required V_{OL}:** Determine the L/W ratio needed to achieve this V_{OL} at the output for this V_{OH} at the input. To do this you have to properly identify what bias region you are in (linear, cutoff or saturation). Lower V_{OL} will require a wider transistor (more conductive) in order to "pull the output low". Lower VOH at the input will not "turn on the transistor as hard" and thus will also need a more conductive (wider) switching transistor.

4. **Design the Load Resistor/Transistor for the required V_{OL}:** Determine the required load (resistor or transistor L/W) needed to achieve this V_{OL} at the output for this V_{OH} at the input. If the load is a transistor (later) you will need to determine the proper bias mode linear, cutoff or saturation.

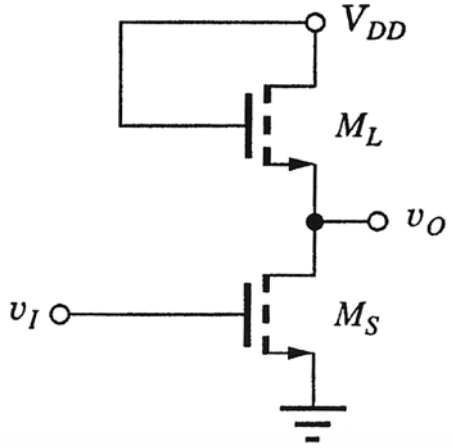
5. **Find the Intermediate State 1/0 Edge voltages V_{IL} and V_{IH} :** For V_{IL} and V_{IH} they are each found the same way. 1st, determine an appropriate voltage transfer function (relating v_i to v_o) by setting the currents of the two devices equal. To do this, you will need to determine the proper bias mode linear, cutoff or saturation of each device. Next, take the derivative of the voltage transfer equation and set it equal to -1. Calculate the input voltage required for this slope to equal -1. This is by definition V_{IL} or V_{IH} . Note that V_{IL} and V_{IH} are two separate calculations and will have two different bias modes (i.e. different selections of linear, or saturation equations).

Our Options



Linear Load: $V_{GG}>V_{DD}$ so $V_{GS-L}>V_{DS-L}$

Requires an extra power supply and is therefore, expensive!

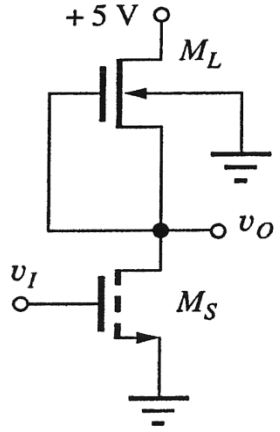


Saturated Enhancement Load:

$V_{GS-L}-V_{TN}<V_{DS-L}$

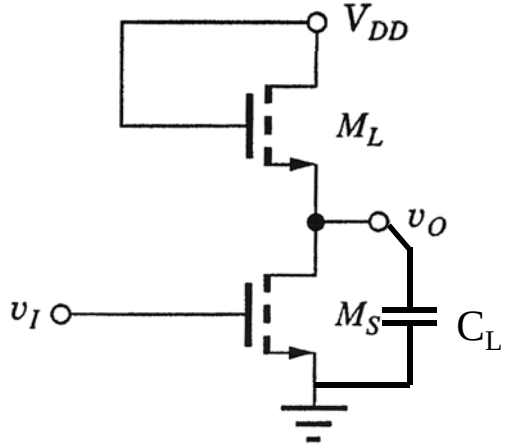
$-V_{TN}<0$

Always Saturated (when on)



Depletion Load:

Saturated Enhancement Load



$V_{GS-L}=V_{DS-L}$

Inverter State:
Input is Low
Output is High

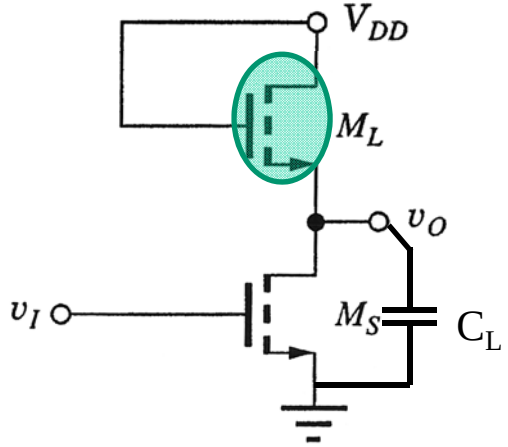
As before, for $v_i=v_{GS}=V_{OL}<V_T$

$$i_{DS-S} = 0$$

$V_{OL}<V_T$ is our first design criteria!

For a nominal V_T = 1, we would typically make V_{OL}~0.25V to insure adequate noise margin.

Saturated Enhancement Load



$V_{GS-L}=V_{DS-L}$

For $v_i=v_{GS}=V_{OH}$, M_S and M_L conduct their maximum amount of current.

$v_O=V_{OL}=0.25V$ so,

$V_{DS-L}=V_{DD}-v_O=4.75V$

$$i_{DS-L}=\frac{K_n'}{2}\left(\frac{W}{L}\right)\Big|_L\left(v_{GS-L}-V_{TN}\right)^2$$

Using the same power design spec (0.25mW) and device parameters as before,

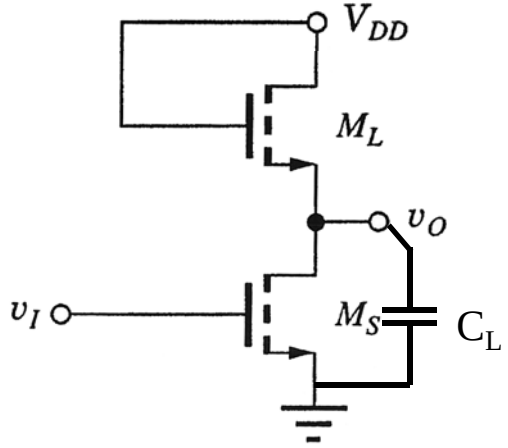
$$i_{DS-L}=50uA, \text{so}$$

Inverter State:
Input is High
Output is Low

$$50e-6=12.5e-6\left(\frac{W}{L}\right)\Big|_L\left(4.75-1\right)^2$$

$$\left(\frac{W}{L}\right)\Big|_L=0.284$$

Saturated Enhancement Load

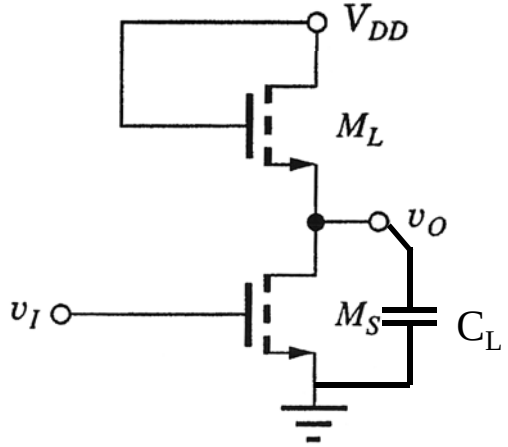


$$\left.\left(\frac{W}{L}\right)\right|_L = 0.284$$

Since we normally reference the width to length ratio in terms of it's "smallest dimension that we can fabricate" (as of 2001 this is ~0.07 um in the lab, 0.18 um in production) we can express this in an alternative form. For our discussion, we will assume (for mathematical simplicity) that this smallest feature size is 1um. Thus,

$$\left.\left(\frac{W}{L}\right)\right|_L = \frac{1}{3.52}$$

Saturated Enhancement Load



Inverter State:
Input is Low
Output is High

V_{OH}:

When M_S is off, C_L charges up through M_L, reducing V_{DS-L} until

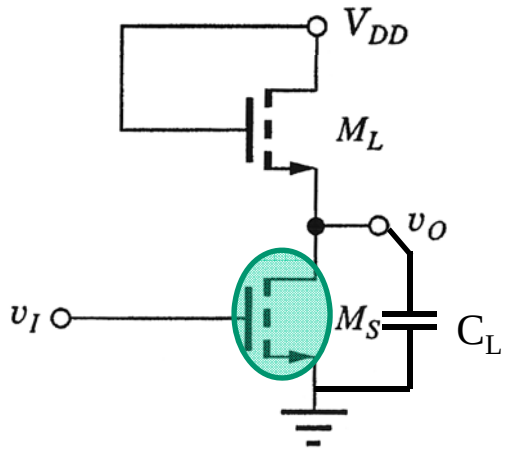
$$V_{TN} = V_{GS-L} = V_{DS-L}$$

At this point, M_L cuts off preventing further charging.

Thus, when $v_O=V_{OH}$, $v_{GS-L}=V_{DD}-V_{TN}$ or $V_{OH}=V_{DD}-V_{TN}=5-1=4V$

V_{OH} is significantly reduced from it's previous (with resistive load) value!

Saturated Enhancement Load



Since $v_i=V_{GS-S}=V_{OH}$ is the voltage that forces M_S to turn on and force the output to V_{OL}, we must provide the same amount of "pull-down current" (50uA) for a lower voltage (4V instead of 5V). Thus, we need to make the transistor wider to conduct more current at the lower voltage. (Remember, the switching transistor is in the linear region for $v_i=V_{OH}$ so it acts like a resistor. Providing less resistance will provide more drive current.).

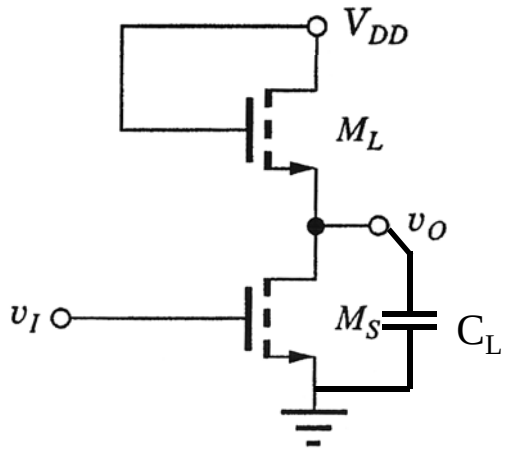
Inverter State:
Input is High
Output is Low

$$i_{DS-S} = K_n'\left(\frac{W}{L}\right)\Big|_S \left(v_{GS-S} - V_{TN} - 0.5v_{DS-S}\right)v_{DS-S}$$

$$50e-6A = 25e-6\left[\frac{A}{V^2}\right]\left(\frac{W}{L}\right)\Big|_S \left(4V - 1V - 0.5\left(0.25V\right)\right)0.25V$$

$$\left(\frac{W}{L}\right)\Big|_S = \frac{2.78}{1}$$

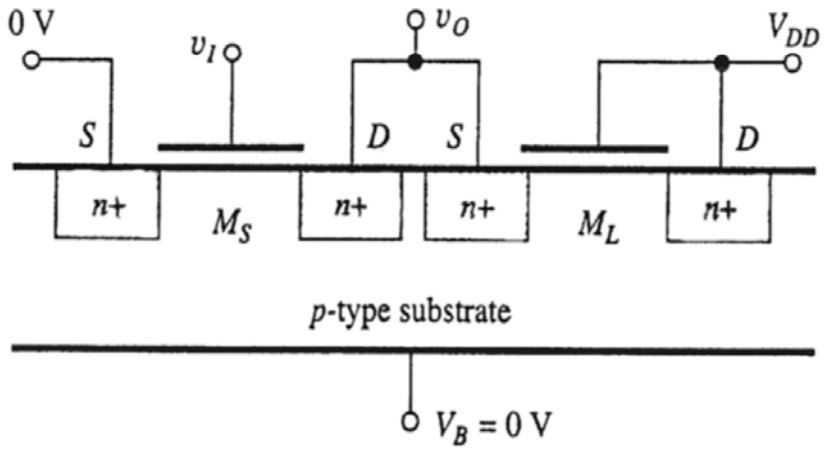
Saturated Enhancement Load

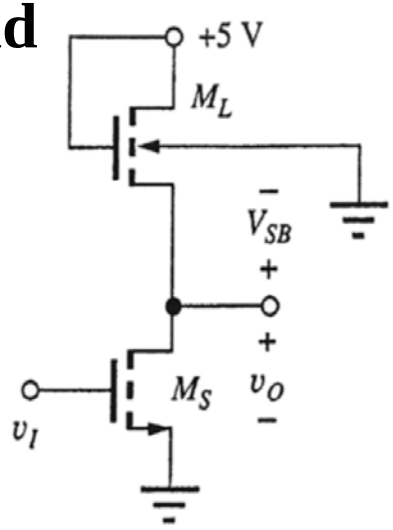


Combining the results from before we see that our Load Transistor is much longer than it is wide, while our switching transistor is wider than it is long.

$$\left.\left(\frac{W}{L}\right)\right|_L = \frac{1}{3.52} \qquad \left.\left(\frac{W}{L}\right)\right|_S = \frac{2.78}{1}$$

Saturated Enhancement Load





Since the substrate is common to both transistors, the body-to-source voltage, v_{SB}, varies as the output voltage varies. Thus, the threshold voltage varies resulting in a variation in V_{OH}

$$V_{OH} = V_{DD} - V_{TN-L}$$

$$V_{OH} = V_{DD} - \left[V_{TO} + \gamma\left(\sqrt{v_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right)\right]$$

$$V_{OH} = V_{DD} - \left[V_{TO} + \gamma\left(\sqrt{V_{OH} + 2\phi_F} - \sqrt{2\phi_F}\right)\right]$$

In writing the above equation we have only examined the condition when $v_{SB}=V_{OH}$. Since $v_{SB}=v_O$, the threshold voltage is continuously varying as the device is switched, introducing an additional level of "non-linearity" ($v_O=f(v_O)$ and $i_{DS}=f(v_O)$).

Saturated Enhancement Load

$$If\ \gamma = 0.5\sqrt{V} \quad and \quad 2\phi_F = 0.6V$$

$$V_{OH} = V_{DD} - \left[V_{TO} + \gamma\left(\sqrt{V_{OH} + 2\phi_F} - \sqrt{2\phi_F}\right)\right]$$

$$V_{OH} = 5 - \left[1 + 0.5\left(\sqrt{V_{OH} + 0.6} - \sqrt{0.6}\right)\right]$$

$$or$$

$$V_{OH}{}^2 - 9.03V_{OH} + 19.1 = 0$$

$$V_{OH} = 3.39V \ or \ 5.64V$$

Saturated Enhancement Load

Since the body effect changes V_{TN}, we need to readjust the width to length ratios of both transistors:

M_S: V_{OH} is lower than what we used before, so we need the same current at a lower voltage--make the switching transistor even wider!

$$i_{DS-S} = K_n' \left(\frac{W}{L}\right)\Big|_S \left(v_{GS-S} - V_{TN} - 0.5v_{DS-S}\right)v_{DS-S}$$

$$50e-6A = \ldots$$

$$\ldots 25e-6\left[\frac{A}{V^2}\right]\left(\frac{W}{L}\right)\Big|_S \left(3.39V - 1V - 0.5\left(0.25V\right)\right)0.25V$$

$$\left(\frac{W}{L}\right)\Big|_S = \frac{3.59}{1}$$

Inverter State:
Input is High
Output is Low

Saturated Enhancement Load

Inverter State:
Input is High
Output is Low

M_L: When $v_i=V_{OH}$, $v_o=V_{OL}=v_{SB}=0.25V$

$$V_{TN-L} = V_{TO} + \gamma\left(\sqrt{v_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right)$$
$$V_{TN-L} = 1 + 0.5\left(\sqrt{0.25 + 0.6} - \sqrt{0.6}\right)$$
$$V_{TN-L} = 1.07V$$

$$i_{DS-L} = \frac{K_n'}{2}\left(\frac{W}{L}\right)\Bigg|_L \left(v_{GS-L} - V_{TN-L}\right)^2$$

$$50e-6 = 12.5e-6\left(\frac{W}{L}\right)\Bigg|_L \left(4.75 - 1.07\right)^2$$

$$\left(\frac{W}{L}\right)\Bigg|_L = \frac{1}{3.39}$$

Saturated Enhancement Load

So the body effect requires that:

Without the Body Effect

$$\left.\left(\frac{W}{L}\right)\right|_L = \frac{1}{3.52}$$

$$\left.\left(\frac{W}{L}\right)\right|_S = \frac{2.78}{1}$$

$$V_{OH} = 4.0V$$

$$V_{OL} = 0.25V$$

With the Body Effect

$$\left.\left(\frac{W}{L}\right)\right|_L = \frac{1}{3.39}$$

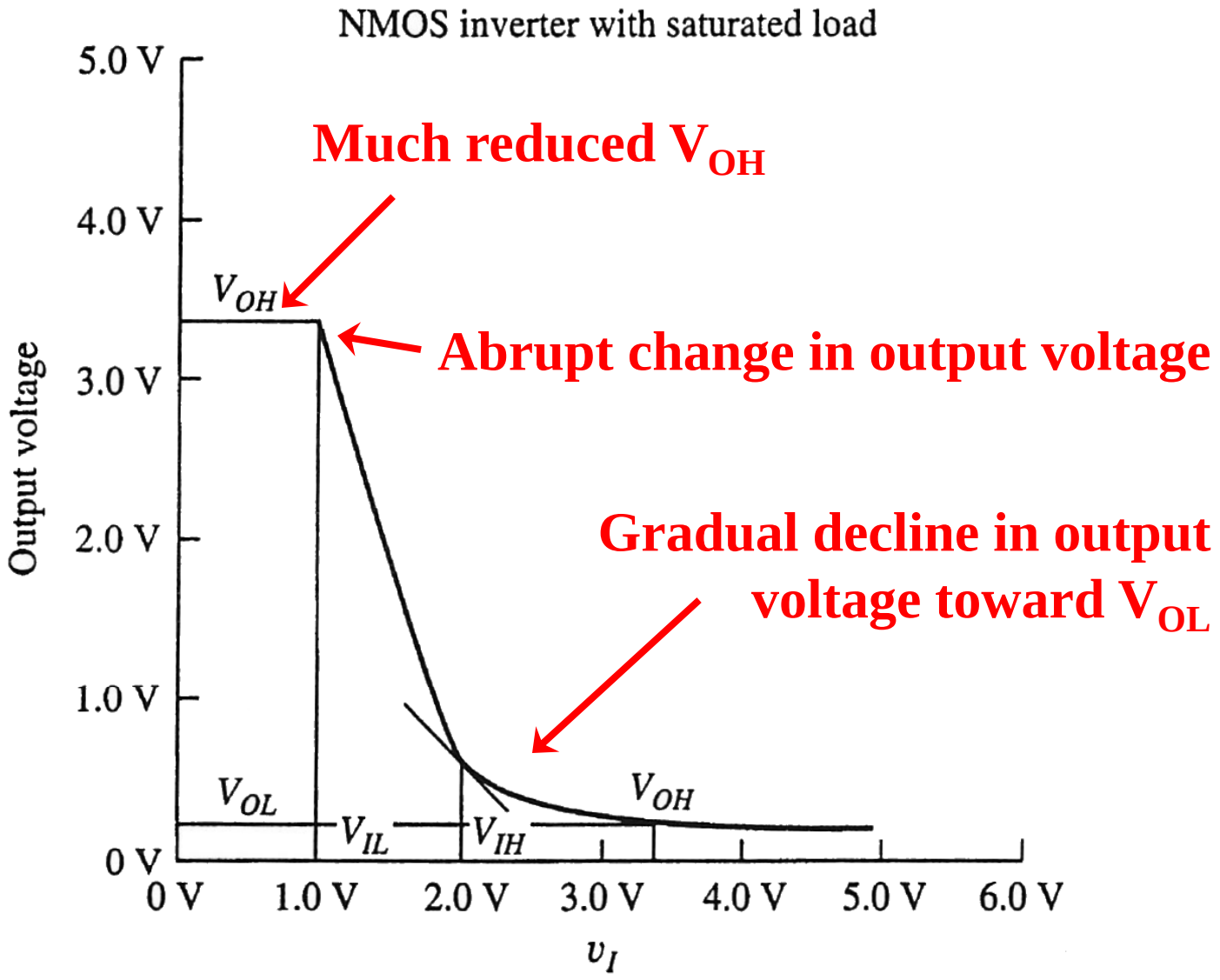
$$\left.\left(\frac{W}{L}\right)\right|_S = \frac{3.53}{1}$$

$$V_{OH} = 3.4V$$

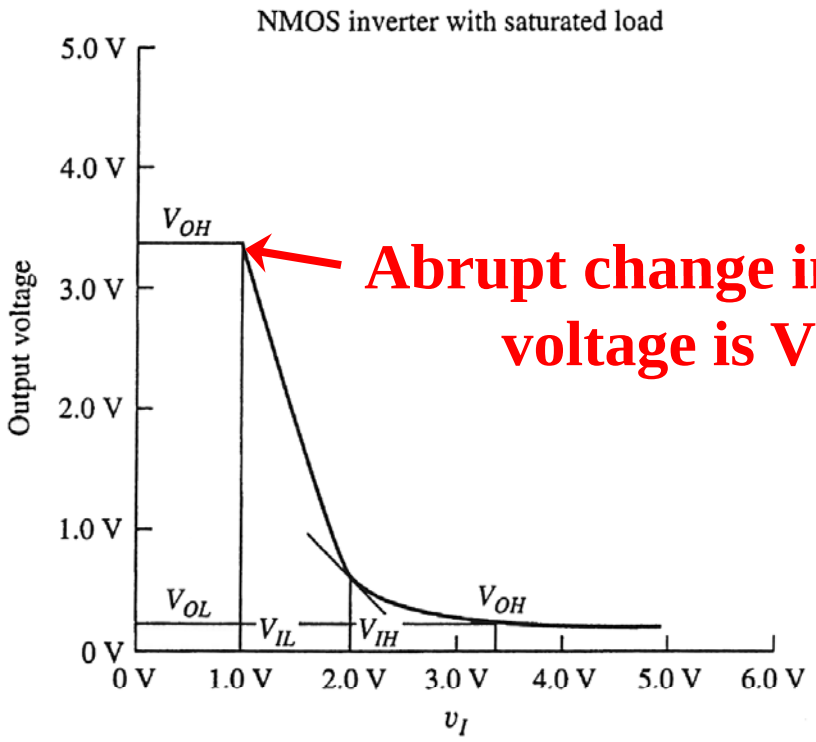
$$V_{OL} = 0.25V$$

Saturated Enhancement Load

Saturated load VTC



Saturated Enhancement Load



Abrupt change in output voltage is $V_{IL}=V_{TN-S}$

Inverter Transitional State:
Input is Low
Output is High

The abrupt nature of this transition is due to $V_{TN-S}<V_{TN-L}$ due to the body effect. Thus, as M_S begins to conduct, M_L is off.

Saturated Enhancement Load

Find V_{IH}:

Inverter Transitional State:
Input is High
Output is Low

$$i_{DS-S} = i_{DS-L}$$

$$K_{n-S}\left(v_{GS-S} - V_{TNS} - 0.5v_{DS-S}\right)v_{DS-S} = K_{n-L}\left(v_{GS-L} - V_{TNL}\right)^2$$

$$K_{n-S}\left(v_i - V_{TNS} - 0.5v_O\right)v_O = K_{n-L}\left(V_{DD} - v_O - V_{TNL}\right)^2$$

solving for v_i,

$$v_i = V_{TNS} + 0.5v_O + \frac{K_{n-L}}{2K_{n-S}}\left[\frac{V_{DD} - V_{TNL}}{v_O} - 2\left(V_{DD} - V_{TNL}\right) + v_o\right]$$

$$Assume\ \frac{dv_O}{dv_i} = \left(\frac{dv_i}{dv_O}\right)^{-1}$$

Neglect since the change in V_{TNL} with v_o is slow

$$\frac{dv_i}{dv_O} = 0.5 + \frac{K_{n-L}}{2K_{n-S}}\left[1 - \frac{\left(V_{DD} - V_{TNL}\right)^2}{{v_O}^2}\right] + \frac{K_{n-L}}{K_{n-S}}\left(\frac{dV_{TNL}}{dv_o}\right)$$

Saturated Enhancement Load

Setting this derivative=-1 and solving for v_o:

$$\frac{dv_i}{dv_O} = 0.5 + \frac{K_{n-L}}{2K_{n-S}}\left[1 - \frac{(V_{DD} - V_{TNL})^2}{v_O{}^2}\right] = -1$$

$$v_O = \frac{(V_{DD} - V_{TNL})}{\sqrt{1 + 3\frac{(W/L)_S}{(W/L)_L}}}$$

or in our case,

$$v_O = \frac{(5-1)}{\sqrt{1+3(3.53)(3.39)}} = 0.66V$$

Plugging this back into our expression for v_i,

$$v_i = V_{TNS} + 0.5v_O + \frac{K_{n-L}}{2K_{n-S}}\left[\frac{V_{DD} - V_{TNL}}{v_O} - 2(V_{DD} - V_{TNL}) + v_o\right]$$

$$v_i = 1 + 0.5(0.66) + \frac{1}{2(3.53)(3.39)}\left[\frac{5-1}{0.66} - 2(5-1) + 0.66\right] = 1.97V$$

$$V_{IH} = 1.97V$$

All assumptions can be checked and verified!

Saturated Enhancement Load

Noise Margins:

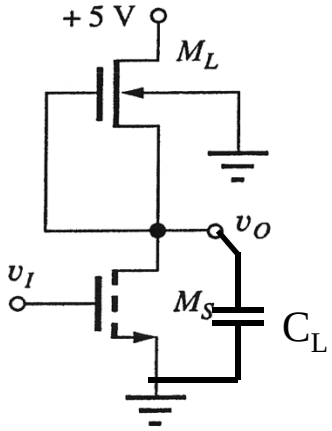
$$NM_L = V_{IL} - V_{OL}$$

$$and,$$

$$NM_H = V_{OH} - V_{IH}$$

Depletion Load

Recall that the depletion mode NMOS transistor has a threshold voltage that is negative, resulting it being on for v_{GS}=0.

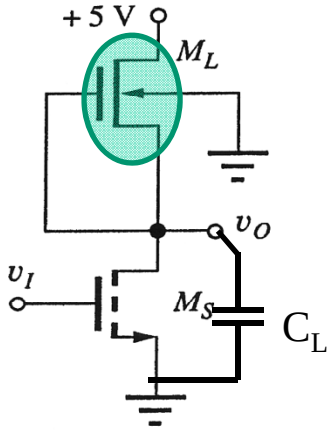


Once again, to insure that M_S is sufficiently cutoff, we choose V_{OL}<<V_{TN-S} or for our example where V_{TN-S}=1 V, V_{OL}=0.25 V. Thus, when v_i=V_{OL}, M_S is off.

Thus, when M_S is sufficiently cutoff, (v_i=V_{OL}<<V_{TN-S}) v_O=V_{OH}=V_{DD} due to the depletion load conducting for all output voltages allowing C_L to charge up to the power supply voltage. (I.e. unlike the enhancement case, the load transistor never cuts off).

Thus, the depletion load inverter allows V_{OH} to equal V_{DD}, a very nice improvement over the saturated Load case!

Depletion Load



Inverter State:
Input is High
Output is Low

Using $V_{DD} = 5V$, $V_{OL} = 0.25V$, $V_{TN\text{-}L} = -3V$,

$I_{DS} = 50uA$, $K_n' = 25\,uA/V^2$, $\gamma = 0.5\sqrt{V}$ *and* $2\phi_F = 0.6V$

and noting that when

$v_i = V_{OH}$, $v_O = V_{OL} = 0.25V$ means $v_{DS\text{-}L} = V_{DD} - v_O = 4.75V$ and

$v_{GS\text{-}S} = 0 \rightarrow M_L$ is saturated,

Thus,

$$i_{DS\text{-}L} = \frac{K_n'}{2}\left(\frac{W}{L}\right)\Bigg|_L (v_{GS-L} - V_{TN-L})^2$$

$$i_{DS\text{-}L} = \frac{K_n'}{2}\left(\frac{W}{L}\right)\Bigg|_L (V_{TN-L})^2$$

but due to the Body - Source voltage effect on M_L,

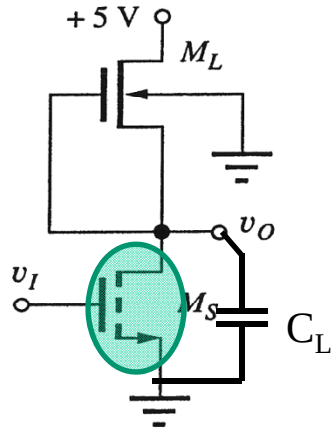
$V_{TN\text{-}L} = V_{TNO} + \gamma\left(\sqrt{v_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right)$ or in our case,

$V_{TN\text{-}L} = -3V + 0.5\sqrt{V}\left(\sqrt{0.25V + 0.6V} - \sqrt{0.6V}\right) = -2.93V$

Thus,

$$\left(\frac{W}{L}\right)\Bigg|_L = 0.466 = \frac{1}{2.15}$$

Depletion Load



Inverter State:
Input is High
Output is Low

Using $V_{DD} = 5V, V_{OL} = 0.25V, V_{TN\text{-}S} = 1V,$

$I_{DS} = 50uA, K_n' = 25\,uA/V^2, \gamma = 0.5\sqrt{V}$

and noting that when

$v_i = V_{OH}, v_O = V_{OL} = 0.25V$ means $v_{DS\text{-}S} = v_O = 0.25V$ and

$v_{GS\text{-}S} = V_{OH} = V_{DD} = 5V \rightarrow M_S$ is in the linear region,

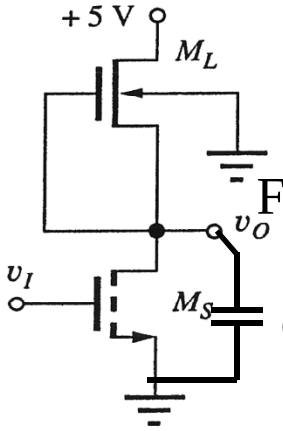
$$i_{DS} = 50\mu A = K_n'\left(\frac{W}{L}\right)\Big|_S \left(v_{GS-S} - V_{TN-S} - 0.5v_{DS-S}\right)v_{DS-S}$$

$$50e-6 = 25e-6\left(\frac{W}{L}\right)\Big|_S (5-1-.125)0.25$$

$$\left(\frac{W}{L}\right)\Big|_S = \frac{2.06}{1}$$

NOTE : This is the same as in the resistive load case!

Depletion Load



V_{IL}:

Inverter Transitional State:
Input is Low
Output is High

For v_i near V_{IL}, v_{DS-S} will be large and v_{DS-L} will be small. Thus, we assume: M_S is saturated and M_L is in the linear region,

$$i_{DS-S} = i_{DS-L}$$

$$K_{n-S}\left(v_{GS-S} - V_{TN-S}\right)^2 = K_{n-L}\left(v_{GS-L} - V_{TN-L} - 0.5v_{DS-L}\right)v_{DS-L}$$

$$K_{n-S}\left(v_i - V_{TN-S}\right)^2 = K_{n-L}\left(0 - V_{TN-L} - 0.5\left(V_{DD} - v_O\right)\right)\left(V_{DD} - v_O\right)$$

Solving for v_o,

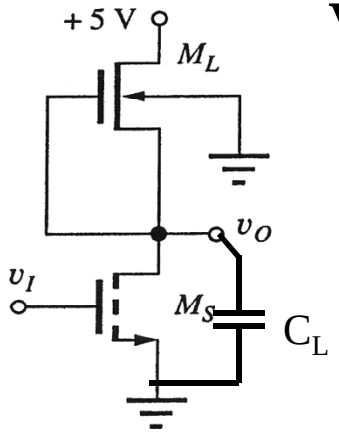
$$v_o = V_{DD} + V_{TN-L} + \sqrt{V_{TN-L}^2 - K_R\left(v_i - V_{TN-S}\right)^2}$$

$$\text{where } K_R = \frac{K_{n-S}}{K_{n-L}}$$

So, $\dfrac{dv_o}{dv_i} = \dfrac{dV_{TN-L}}{dv_i}$ (**Small**) $+ \dfrac{1}{2}\left[V_{TN-L}^2 - K_R\left(v_i - V_{TN-S}\right)^2\right]^{-\frac{1}{2}}\left[2V_{TN-L}\dfrac{dV_{TN-L}}{dv_i}\text{ (Small)} - 2K_R\left(v_i - V_{TN-S}\right)\right]$

$$\frac{dv_o}{dv_i} = \frac{-K_R\left(v_i - V_{TN-S}\right)}{\sqrt{V_{TN-L}^2 - K_R\left(v_i - V_{TN-S}\right)^2}}$$

Depletion Load



V_{IL}:

Setting this derivative equal to -1 and solving for $v_i = V_{IL}$,

$$\frac{dv_o}{dv_i} = \frac{-K_R\left(v_i - V_{TN-S}\right)}{\sqrt{V_{TN-L}^2 - K_R\left(v_i - V_{TN-S}\right)^2}} = -1$$

$$v_i = V_{IL} = V_{TN-S} - \frac{V_{TN-L}}{\sqrt{K_R^2 + K_R}}$$

Note : that V_{TN-L} is a function of V_{SB} (V_{TN-S} is not!)

Assume a value of v_O ($\sim V_{DD}$)

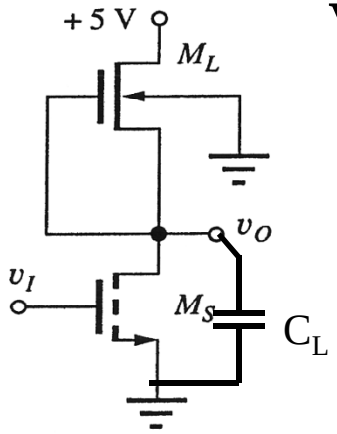
$$V_{TN-L} = V_{TNO} + \gamma\left(\sqrt{v_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right) \text{ using } v_{SB} = v_O$$

$$v_i = V_{IL} = V_{TN-S} - \frac{V_{TN-L}}{\sqrt{K_R^2 + K_R}}$$

$$v_o = V_{DD} + V_{TN-L} + \sqrt{V_{TN-L}^2 - K_R\left(v_i - V_{TN-S}\right)^2}$$

Iterate until convergence!

Depletion Load



V_{IL}:

For our numerical example:

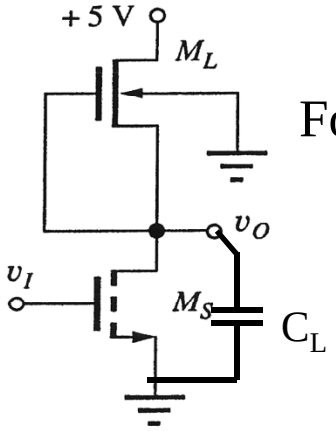
V_{TN-L}=-2.23 V (>-3V)

V_{IL}=1.50 V

v_O=4.74 V

Also, our assumptions regarding transistor operation conditions are correct.

Depletion Load



V_{IH}:

For v_i near V_{IH}, v_{DS-S} will be small and v_{DS-L} will be large. Thus, we assume: M_L is saturated and M_S is in the linear region,

$$i_{DS-L} = i_{DS-S}$$

$$K_{n-L}\left(v_{GS-L} - V_{TN-L}\right)^2 = K_{n-S}\left(v_{GS-S} - V_{TN-S} - 0.5v_{DS-S}\right)v_{DS-S}$$

$$K_{n-L}\left(0 - V_{TN-L}\right)^2 = K_{n-S}\left(v_i - V_{TN-S} - 0.5(v_O)\right)(v_O)$$

Solving for v_i, $$v_i = V_{TN-S} + \frac{v_O}{2} + \frac{K_L}{2K_S}\frac{V_{TN-L}^2}{v_O}$$

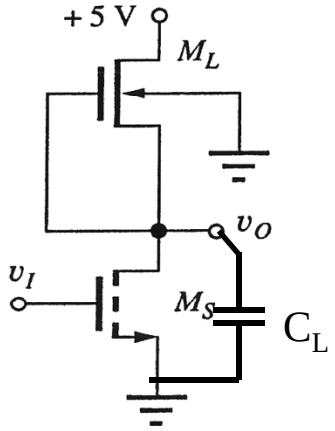
Assuming, $$\frac{dv_O}{dv_i} = \left[\frac{dv_i}{dv_O}\right]^{-1}$$

Small

$$\frac{dv_i}{dv_O} = \frac{1}{2} - \frac{K_L}{2K_S}\frac{V_{TN-L}^2}{(v_O)^2} + \frac{2K_L}{2K_S}\frac{V_{TN-L}}{v_O}\left(\frac{dV_{TN-L}}{dv_O}\right)$$

$$\frac{dv_i}{dv_O} = \frac{1}{2} - \frac{1}{2K_R}\frac{V_{TN-L}^2}{(v_O)^2}, \quad \text{where } K_R = \frac{K_{n-S}}{K_{n-L}}$$

Depletion Load



V_{IH}: Setting the derivative equal to -1 and solving for v_O,

$$\frac{dv_i}{dv_O} = \frac{1}{2} - \frac{1}{2K_R}\frac{V_{TN-L}^2}{(v_O)^2} = -1$$

$$v_O = -\frac{V_{TN-L}}{\sqrt{3K_R}}$$

Thus,

Inverter Transitional State:
Input is High
Output is Low

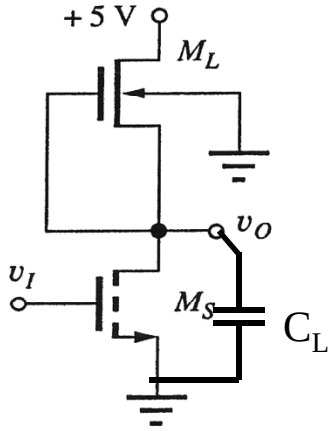
$$v_i = V_{TN-S} + \frac{v_O}{2} + \frac{K_L}{2K_S}\frac{V_{TN-L}^2}{v_O}$$

$$v_i = V_{TN-S} + \frac{\left(-\frac{V_{TN-L}}{\sqrt{3K_R}}\right)}{2} + \frac{K_L}{2K_S}\frac{V_{TN-L}^2}{\left(-\frac{V_{TN-L}}{\sqrt{3K_R}}\right)}$$

$$v_i = V_{TN-S} - \left(\frac{V_{TN-L}}{2\sqrt{3K_R}}\right) - \frac{1}{2K_R}\frac{V_{TN-L}^2\sqrt{3K_R}}{V_{TN-L}}$$

Cont'd...

Depletion Load



V_{IH}: Cont'd...

$$v_i = V_{TN-S} - \left(\frac{V_{TN-L}}{2\sqrt{3K_R}}\right) - \frac{1}{2K_R}\frac{V_{TN-L}^2\sqrt{3K_R}}{V_{TN-L}}$$

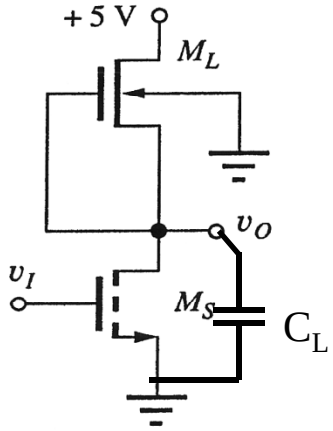
$$v_i = V_{TN-S} - \frac{V_{TN-L}}{2\sqrt{3K_R}}\left(\frac{K_R}{K_R}\right) - \frac{V_{TN-L}\sqrt{3K_R}}{2K_R}\left(\frac{\sqrt{3K_R}}{\sqrt{3K_R}}\right)$$

$$v_i = V_{TN-S} - \frac{V_{TN-L}K_R + V_{TN-L}3K_R}{2K_R\sqrt{3K_R}}$$

$$v_i = V_{TN-S} - \frac{2V_{TN-L}}{\sqrt{3K_R}}$$

$$v_i = V_{IH} = V_{TN-S} + 2v_O$$

Depletion Load



V_{IH}: Cont'd...

Assume a value of $V_{TN\text{-}L}$ ($\sim V_{TNO\text{-}L}$)

$$v_O = -\frac{V_{TN-L}}{\sqrt{3K_R}}$$

$$V_{IH} = V_{TN-S} + 2v_O$$

Iterate until convergence!

$$V_{TN\text{-}L} = V_{TNO} + \gamma\left(\sqrt{v_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right) \text{using } v_{SB} = v_O$$

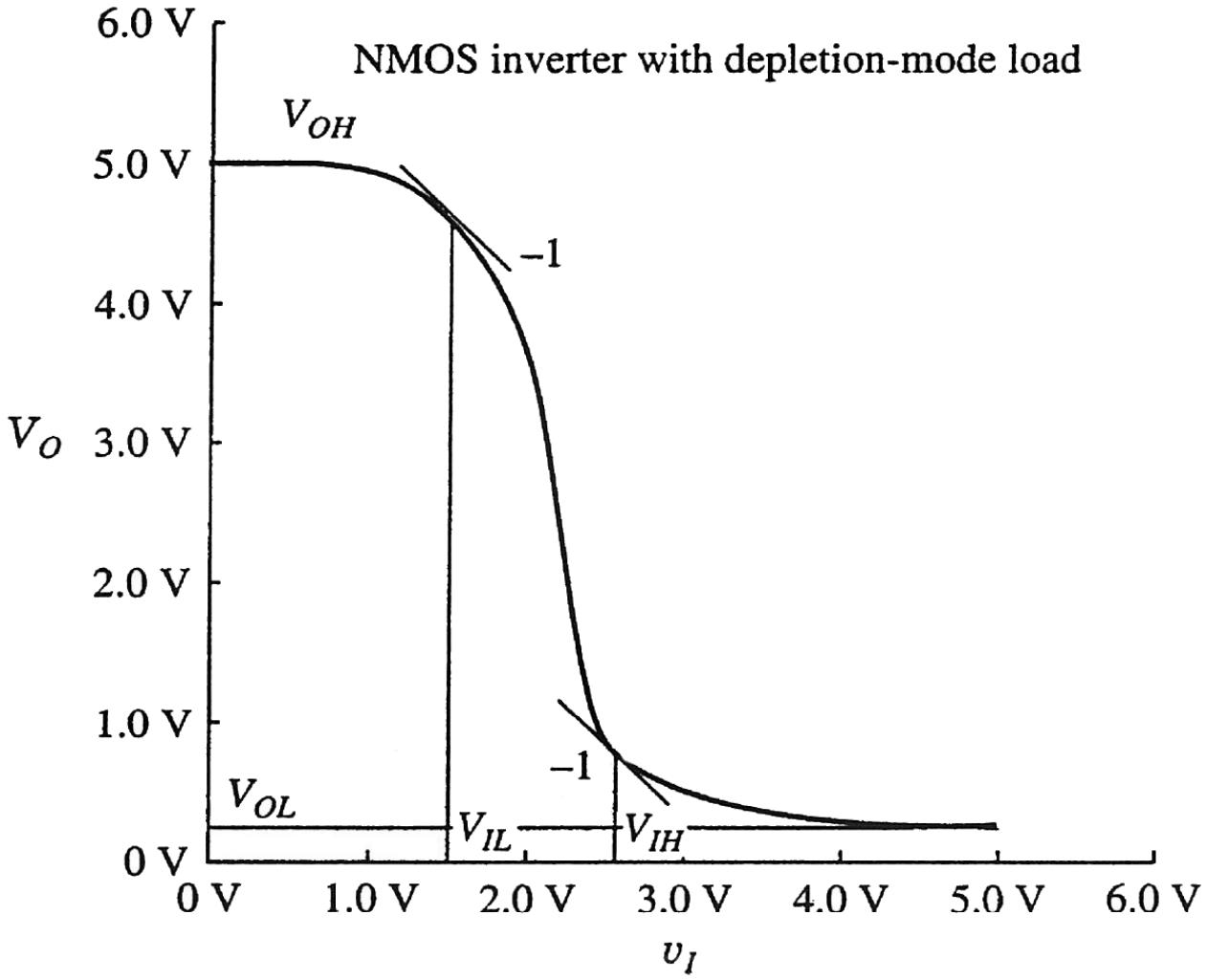
For our numerical example:

$V_{TN\text{-}L}$=-2.80 V, V_{IH}=2.53 V, v_O=0.77 V

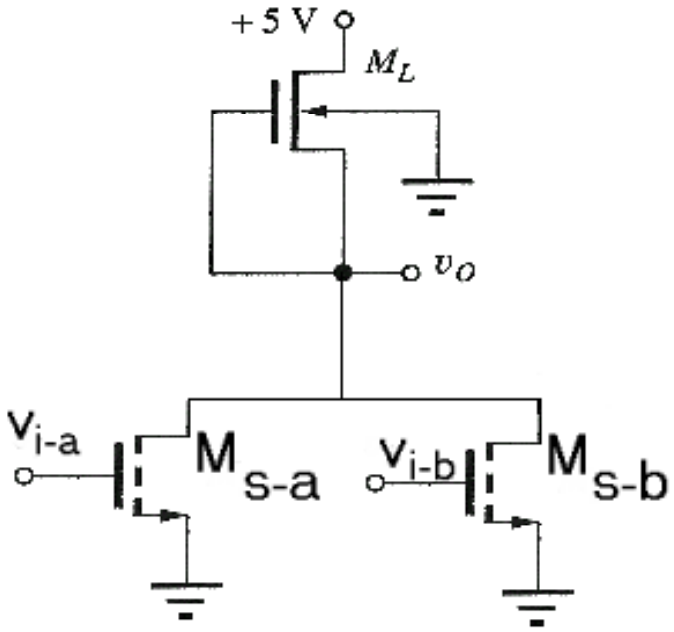
Also, our assumptions regarding transistor operation conditions are correct.

Depletion Load

VTC

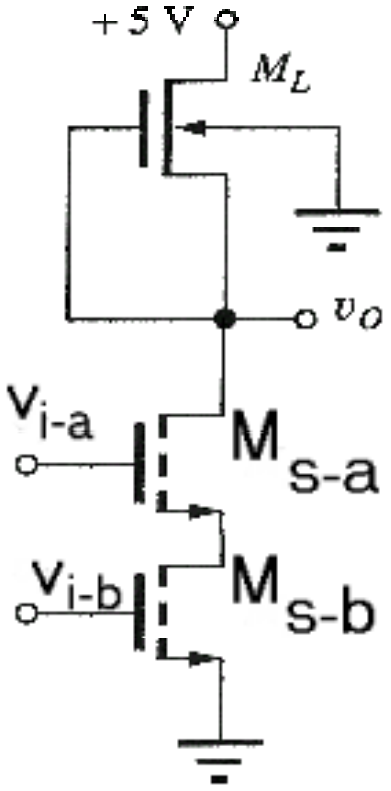


NMOS NOR Gate



If either input, v_{i-a} or v_{i-b} goes high ($v_i=V_{OH}$), v_o goes low ($v_o=V_{OL}$)

NMOS NAND Gate



If both inputs, v_{i-a} or v_{i-b} goes high ($v_i=V_{OH}$), v_o goes low ($v_o=V_{OL}$)

Depletion Load

The Depletion Load NMOS gate…

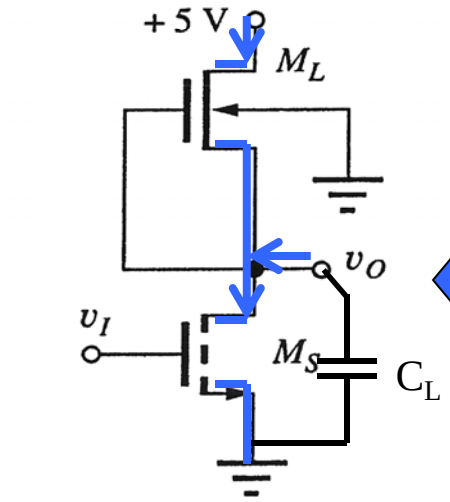
… takes up much less area, leading to higher density (more complex and faster) circuitry.

… has a $V_{OH}=V_{DD}$

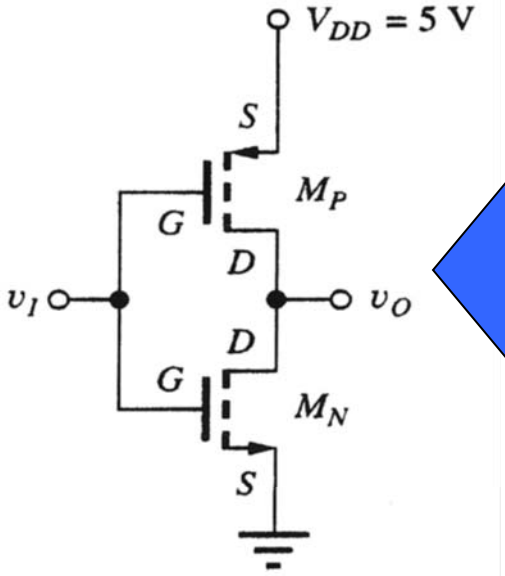
…switches faster leading to higher frequency operation.

… dominated microprocessor design until "CMOS" or Combination-MOS replaced it.

CMOS Logic Gates

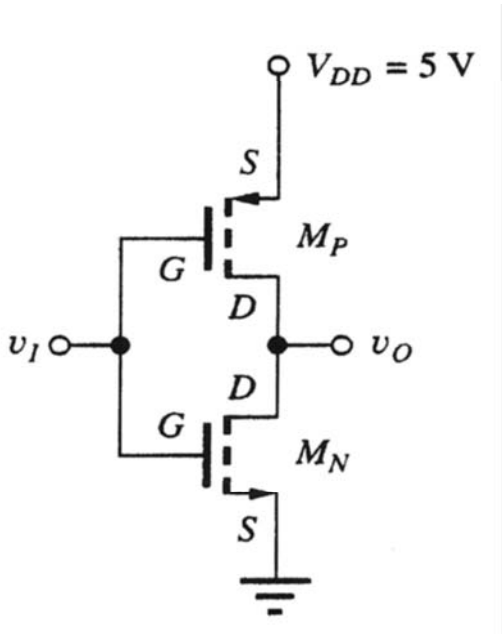


NMOS Logic Gates "waste" power by having a current flow from V_{DD} to ground during the "0" output state. All we really need during this state is a current path to discharge C_L. Analogous to a Class A out put stage.



CMOS Logic Gates eliminate this DC or "Static" power dissipation. CMOS logic gates only dissipate power during a switching event. Once in a state, no power is used. Analogous to a class B output stage (push pull).

CMOS Logic Gates

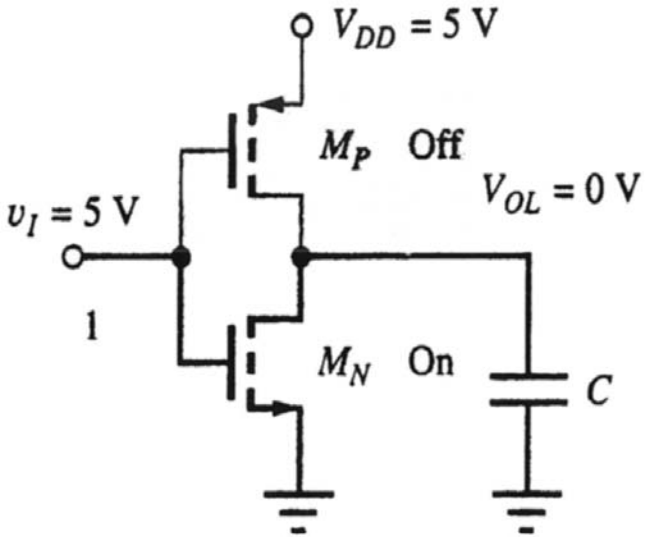


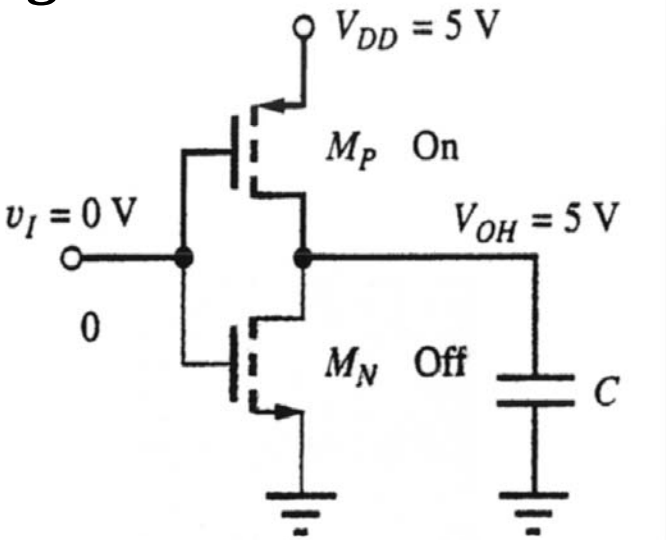
•CMOS Inverter uses one NMOS and 1 PMOS transistor.

•Each Transistor is design to have V_{TN}=-V_{TP} (recall for PMOS, V_{TP}<0)

•Since the Body can be connected to source for the NMOS and VDD for the PMOS, there is no problem with the body effect *FOR THE CMOS INVERTER (ONLY)*

CMOS Logic Gates





- For $v_i > V_{TN}$ and $v_i > V_{DD}+V_{TP}$ (example: if v_i=5V, V_{TN}=1V and V_{TP}=-1V this is satisfied)
- $v_{GS-P} > V_{TP}$ ($v_{SG-P} < -V_{TP}$), $v_{GS-N} > V_{TN}$
- M_P is OFF, M_N is ON
- Load Capacitor discharges all the way down to ground

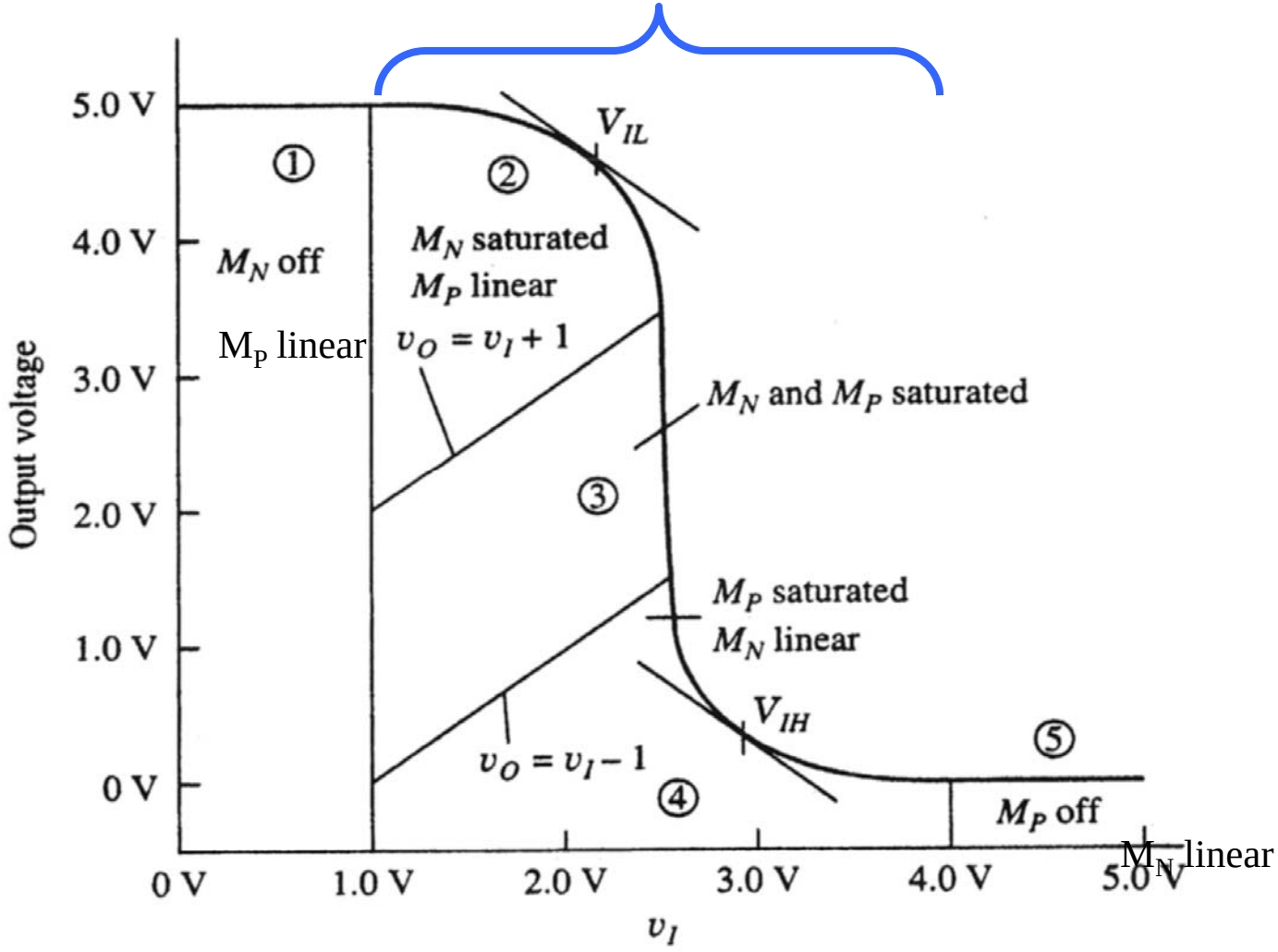
- For $v_i < V_{TN}$ and $v_i < V_{DD}+V_{TP}$ (example: if v_i=0V, V_{TN}=1V and V_{TP}=-1V this is satisfied)
- $v_{GS-P} < V_{TP}$ ($v_{SG-P} > -V_{TP}$), $v_{GS-N} < V_{TN}$
- M_P is ON, M_N is OFF
- Load Capacitor charges all the way up to V_{DD}.

Thus, V_{OL}=0V and V_{OH}=V_{DD}

and there is *NO STEADY_STATE DC CURRENT FLOW*

CMOS Logic Gates

Only during switching are both transistors turned on simultaneously



CMOS Logic Gates

V_{IH}:

For $v_i \sim V_{IH}$, v_{DS-P} is large and v_{DS-N} is small implying M_P is saturated and M_N is linear

Inverter Transitional State:
Input is High
Output is Low

$$i_{DS-N} = i_{DS-P}$$

$$K_n\left(v_{GS-N} - V_{TN} - 0.5V_{DS-N}\right)V_{DS-N} = \frac{Kp}{2}\left(v_{SG-P} + V_{TP}\right)^2$$

$$K_n\left(v_i - V_{TN} - 0.5v_O\right)v_O = \frac{Kp}{2}\left(\left(V_{DD} - v_i\right) + V_{TP}\right)^2$$

Solving for v_O,

$$v_O = v_i - V_{TN} \pm \sqrt{\left(v_i - V_{TN}\right)^2 - \frac{\left(V_{DD} - v_i + V_{TP}\right)^2}{K_R}} \quad where\ K_R = \frac{K_n}{K_p}$$

As before, taking he derivative, $\frac{dv_O}{dv_i}$ and setting this equal to -1 and solving for v_i,

$$V_{IH} = v_i\Big|_{\frac{dv_O}{dv_i}=-1} = \frac{2K_R\left(V_{DD} - V_{TN} + V_{TP}\right)}{\left(K_R - 1\right)\sqrt{1+3K_R}} - \frac{\left(V_{DD} - K_R V_{TN} + V_{TP}\right)}{\left(K_R - 1\right)}$$

CMOS Logic Gates

V_{IH} (cont'd):

For a very useful case where $K_n=K_p$ ($K_R=1$)

Do not use this equation without mathmatical manipulation to eliminate $(K_R - 1)$ terms in denominator

$$V_{IH} = v_i\Big|_{\frac{dv_O}{dv_i}=-1} = \frac{2K_R(V_{DD} - V_{TN} + V_{TP})}{(K_R-1)\sqrt{1+3K_R}} - \frac{(V_{DD} - K_R V_{TN} + V_{TP})}{(K_R-1)}$$

Instead, go back to,

$$v_O = v_i - V_{TN} \pm \sqrt{(v_i - V_{TN})^2 - \frac{(V_{DD} - v_i + V_{TP})^2}{K_R}} \quad where\ K_R = \frac{K_n}{K_p} = 1$$

As before, taking he derivative, $\frac{dv_O}{dv_i}$ and setting this equal to -1 and solving for v_i,

$$V_{IH} = v_i\Big|_{\frac{dv_O}{dv_i}=-1} = \frac{(5V_{DD} + 3V_{TN} + 5V_{TP})}{8} \quad For\ K_R = \frac{K_n}{K_p} = 1$$

CMOS Logic Gates

V_{IL}:

For $v_i \sim V_{IL}$, v_O is large. Thus, v_{DS-P} is small and v_{DS-N} is large implying M_P is linear and M_N is saturated

Inverter Transitional State:
Input is Low
Output is High

$$i_{DS-P} = i_{DS-N}$$

$$K_p\left(v_{SG-P} + V_{TP} - 0.5V_{SD-P}\right)V_{SD-P} = \frac{K_n}{2}\left(v_{GS-N} - V_{TN}\right)^2$$

$$K_p\left(\left(V_{DD} - v_i\right) + V_{TP} - 0.5\left(V_{DD} - v_O\right)\right)\left(V_{DD} - v_O\right) = \frac{K_n}{2}\left(v_i - V_{TN}\right)^2$$

Again, solving for v_O, taking he derivative, $\frac{dv_O}{dv_i}$ and setting this equal to -1 and solving for v_i,

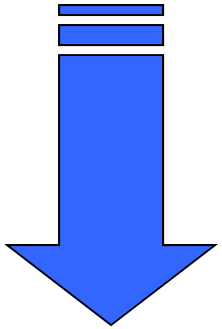
$$V_{IL} = v_i\Big|_{\frac{dv_O}{dv_i}=-1} = \frac{2\sqrt{K_R}\left(V_{DD} - V_{TN} + V_{TP}\right)}{\left(K_R - 1\right)\sqrt{K_R + 3}} - \frac{\left(V_{DD} - K_R V_{TN} + V_{TP}\right)}{\left(K_R - 1\right)}$$

CMOS Logic Gates

V_{IL} (cont'd):

For a very useful case where $K_n=K_p$ ($K_R=1$)

$$V_{IL} = v_i\Big|_{\frac{dv_O}{dv_i}=-1} = \frac{2\sqrt{K_R}\left(V_{DD} - V_{TN} + V_{TP}\right)}{\left(K_R - 1\right)\sqrt{K_R + 3}} - \frac{\left(V_{DD} - K_R V_{TN} + V_{TP}\right)}{\left(K_R - 1\right)}$$



$$V_{IL} = v_i\Big|_{\frac{dv_O}{dv_i}=-1} = \frac{\left(3V_{DD} + 5V_{TN} + 3V_{TP}\right)}{8} \quad \textit{for } K_R = \frac{K_n}{K_P} = 1$$

As always, we can calculate the appropriate noise margins.

CMOS Logic Gates

Example: Calculate the noise margins for a logic family with V_{DD}=3.3V, V_{TN}=1V, V_{TP}= -0.75V and K_R=1:

$$V_{OH} = 3.3V$$

$$V_{OL} = 0V$$

$$V_{IH} = \frac{\left(5V_{DD} + 3V_{TN} + 5V_{TP}\right)}{8} = \frac{\left(5(3.3) + 3(0.75) + 5(-0.75)\right)}{8} = 1.86V$$

$$V_{IL} = \frac{\left(3V_{DD} + 5V_{TN} + 3V_{TP}\right)}{8} = \frac{\left(3(3.3) + 5(0.75) + 3(-0.75)\right)}{8} = 1.43V$$

$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_{IH} = 1.43V$$

$$NM_L = V_{IL} - V_{OL} = V_{IL} = 1.43V$$

CMOS Logic Gates

Dynamic Response of a CMOS Inverter:

For the case when $V_{TN}=-V_{TP}$ and $K_R=1$, the transistors are said to be "electrically equivalent" meaning they have identically "opposite" current-voltage characteristics ("on resistance" in the linear state is the same, the voltage turn on points are symmetric etc...).

In this case, the turn on transient and the turn off transient are identical (charging of C_L is through a resistor, $R_{on\text{-}PMOS}$ and discharging of C_L is through a resistor, $R_{on\text{-}NMOS}$ where $R_{on\text{-}PMOS}= R_{on\text{-}NMOS}$)

$$R_{on\text{-}NMOS} = \frac{1}{K_n\left(V_{DD} - V_{TN}\right)} \qquad \textit{and} \qquad R_{on\text{-}PMOS} = \frac{1}{K_p\left(V_{DD} + V_{TP}\right)}$$

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The charging time is related to the "RC time constant" of this resistance and the load capacitor. Detailed analysis indicates a slight elongation of the time constant (due to the resistance of the channel changing during the switching cycle) leading to,

$$\tau_{PHL} = 1.29 R_{on\text{-}NMOS} C_L \qquad \textit{and} \qquad \tau_{PLH} = 1.29 R_{on\text{-}PMOS} C_L$$

It can also be found that,

$$t_f = 2\tau_{PHL} \qquad \textit{and} \qquad t_r = 2\tau_{PLH}$$

For K_R=1, these are equal greatly simplifying timing designs in complex circuits.

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2} = \tau_{PLH} = \tau_{PHL}$$

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Power Considerations:

Since power is only dissipated during a switching event, it can be shown that for a CMOS inverter the power dissipated is,

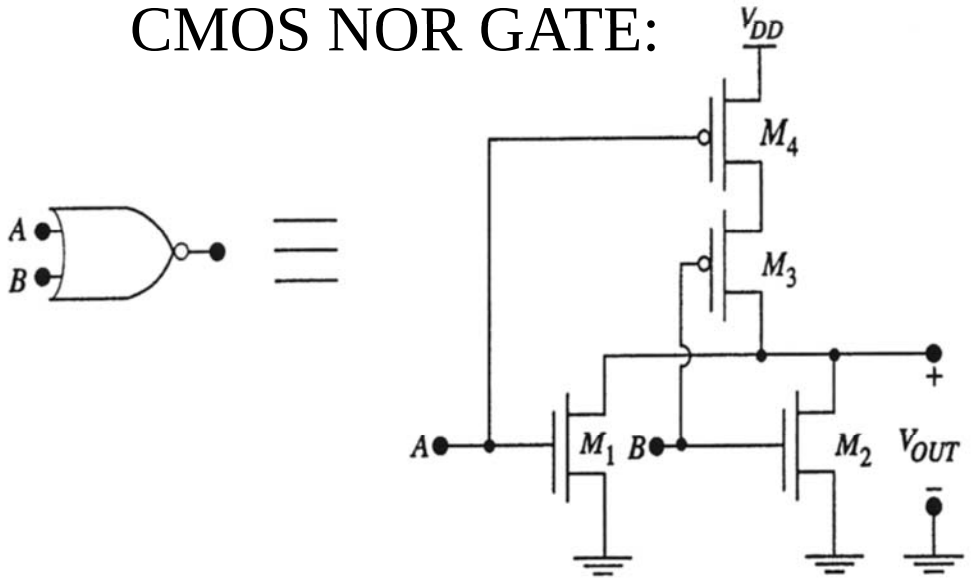
$$P_D = C_L V_{DD}^2 f$$

Where f is the switching frequency (assuming a 50%duty cycle).

Note that for DC, f=0, P_D=0 as expected

CMOS Logic Gates

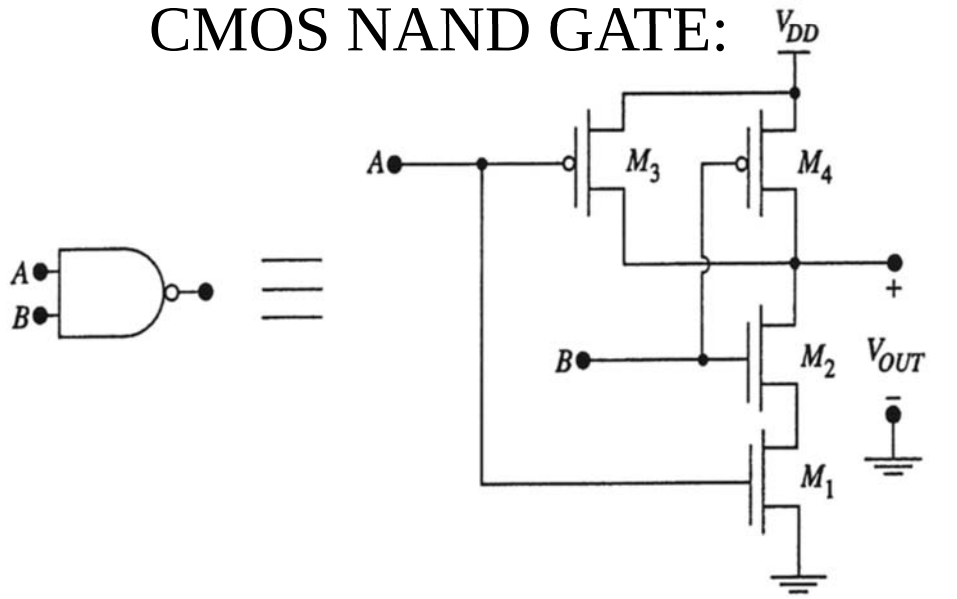
CMOS NOR GATE:



- If both A and B are low, M_1 and M_2 are off, and M_3 and M_4 are on allowing V_{out} to be pulled high
- If either A, B or both are high, M_1 or M_2 or both are on and M_3, or M_4 or both are off allowing V_{out} to be pulled low
- Note that the body effect would modify our design (W/L) of M_3

CMOS Logic Gates

CMOS NAND GATE:



- If both A and B are high, M_1 and M_2 are on, and M_3 and M_4 are off allowing V_{out} to be pulled low
- If either A, B or both are low, M_1 or M_2 or both are off and M_3, or M_4 or both are on allowing V_{out} to be pulled low
- Note that the body effect would modify our design (W/L) of M_2