Lecture 1

Introduction to Microelectronic Technologies:

The importance of multidisciplinary understanding.

Reading:

Chapters 1 and parts of 2

Goal of this Course

The goal of this course is to teach the fundamentals of Microelectronic Technology

- Emphasis will be placed on multidisciplinary understanding using concepts from Electrical Engineering, materials science/engineering, chemistry, physics, and mechanical engineering.

Desired Outcome:

- Provide the student with enough basic information so he/she can understand literature related to his/her desired topic and allow him/her to begin developing new technologies.

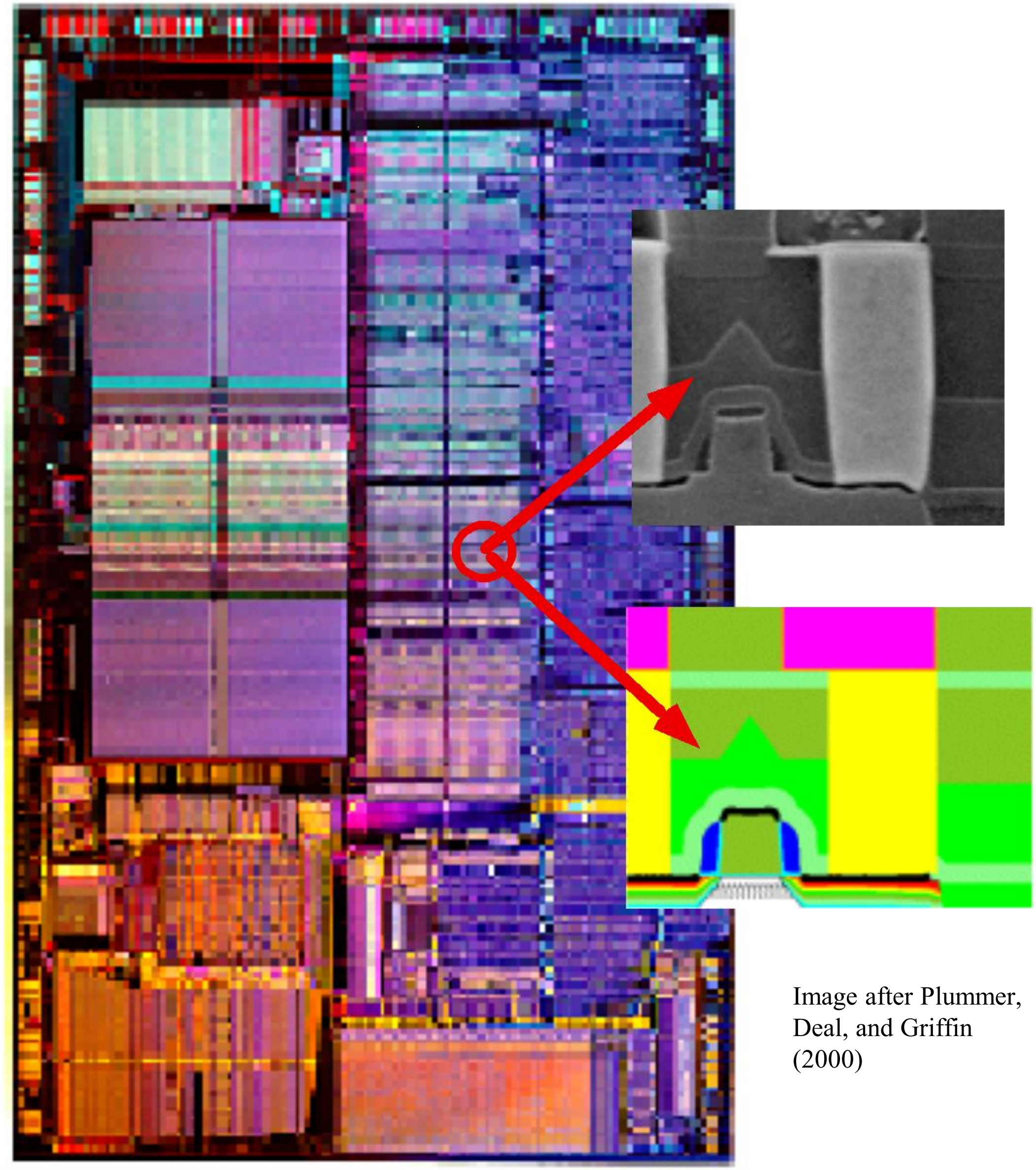

Image after Plummer, Deal, and Griffin (2000)

Disciplines

ECE

- Electrical Design
- Electrostatic Field Control
- Electrical behavior and limits of materials and material systems
- Using defects for our electrical advantage
- Effects of strain and stress on device reliability
- Designing a better device, circuit, system

Material Science

- Structural Classification of Materials: Crystal Structure
- Formation and control of defects, impurity diffusion
- Strain and Stresses materials
- Materials interactions (alloys, annealing)
- Phase transformations

Chemistry

- Bonding Classification of Materials
- Etching and deposition chemistry
- Chemical cleaning

Physics

- Quantum transport
- Solid state descriptions of carrier motion

Mechanical Engineering

- Heat transfer
- Micro-machines-Micro Electro-Mechanical Machines (MEMS)
- Fatigue/fracture, (especially for packaging) etc...
- Mechanical stresses during processing (polishing, thermal cycles, etc…)

Disciplines

ECE

•Electrical Design

•Electrostatic Field Control

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stress on device reliability

•Designing a better device, circuit, system

Interested in the uses of these processes

Material Science

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•...

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...arrier ...

Interested in the fundamental process

Mechanical Engineering

•Heat ...

•Micr... ...ro-Mecha... ...)

•Fatig... ...for packa...

•Mech... ...rocessing (polishing, thermal cycles, etc…)

Interested in the uses of these processes

Modern electronics consist of extremely small devices

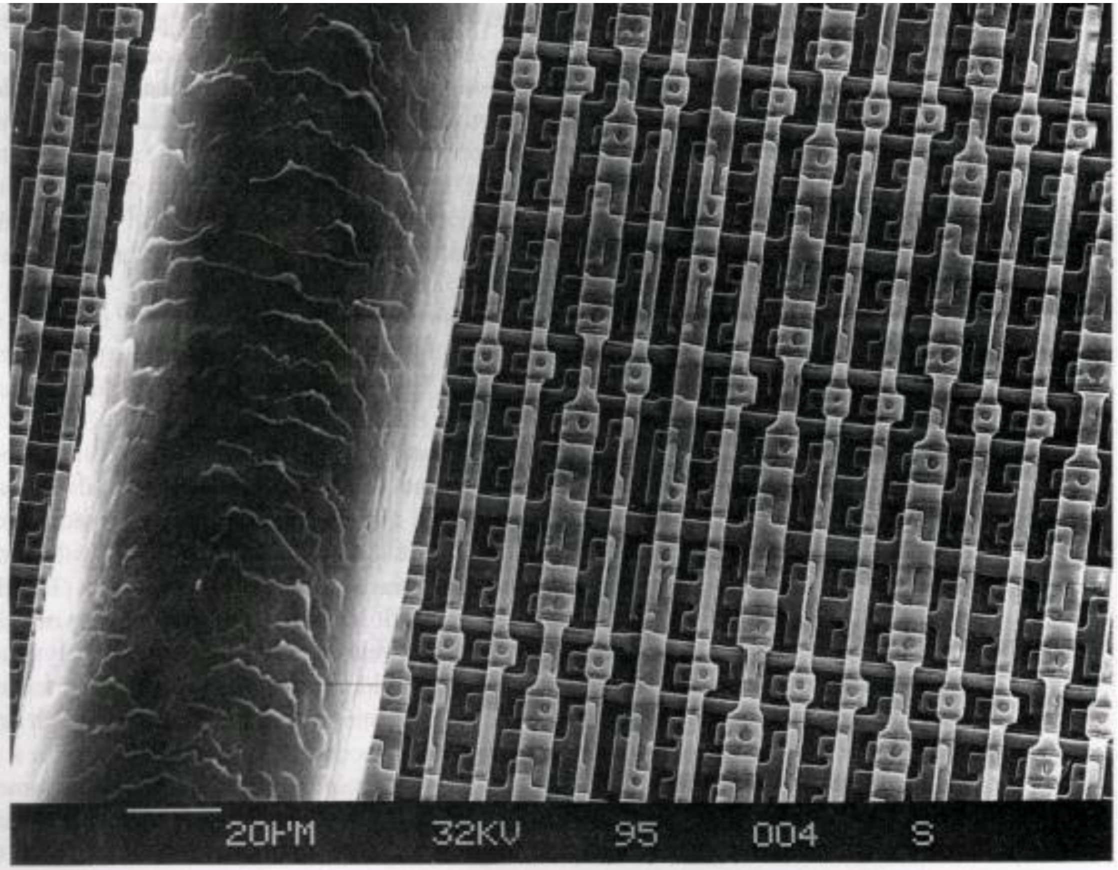


Figure 1-2 Scanning electron micrograph (SEM) of an IC circa mid 1980s. The visible lines correspond to metal wires connecting the transistors.

Transistors in the above image are only a few microns (μm or 1e-6 meters) on a side.

Modern devices have lateral dimensions that are only fractions of a micron (~0.012 μm) and vertical dimensions that may be only a few atoms tall.

Control of Conductivity is the Key to Modern Electronic Devices

- Conductivity, σ, is the ease with which a given material conducts electricity.

- Ohms Law: V=IR or $J=\sigma E$ where J is current density and E is electric field.

  - Metals: High conductivity

  - Insulators: Low Conductivity

  - Semiconductors: Conductivity can be varied by several orders of magnitude.

- It is the ability to control conductivity that make semiconductors useful as "current/voltage control elements". "Current/Voltage control" is the key to switches (digital logic including microprocessors etc…), amplifiers, LEDs, LASERs, photodetectors, etc...

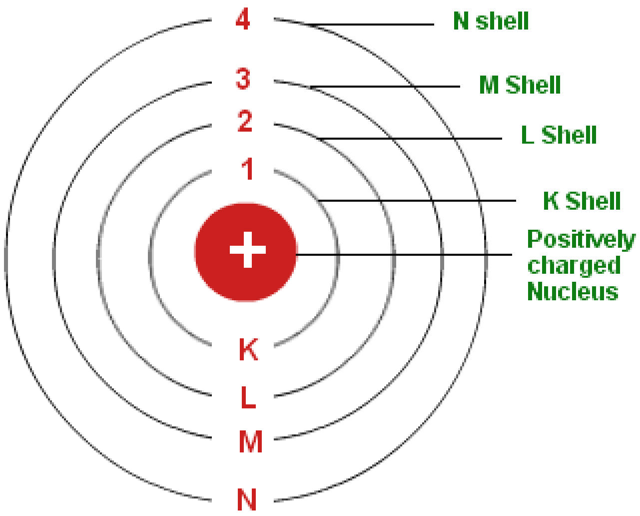
Classifications of Electronic Materials

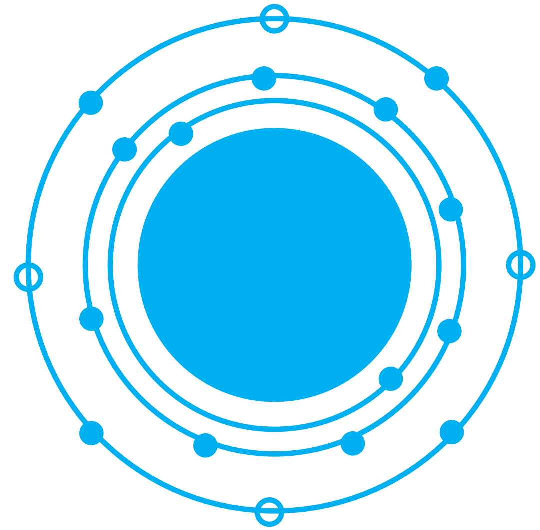
Electrical/Computer engineers like to classify materials based on electrical behavior (insulating, semi-insulating, and metals).

Chemists or Materials Engineers/Scientists classify materials based on bond type (covalent, ionic, metallic, or van der Waals), or structure (crystalline, polycrystalline, amorphous, etc...).

In 20-50 years, EE's may not be using semiconductors at all!! Polymers or bio-electronics may replace them! However the materials science will be the same!

Classifications of Electronic Materials





Example: Silicon n=1 (2 s), n=2 (2 s and 6 p) and n=3 (2 s and 2 p with 4 unoccupied p states)

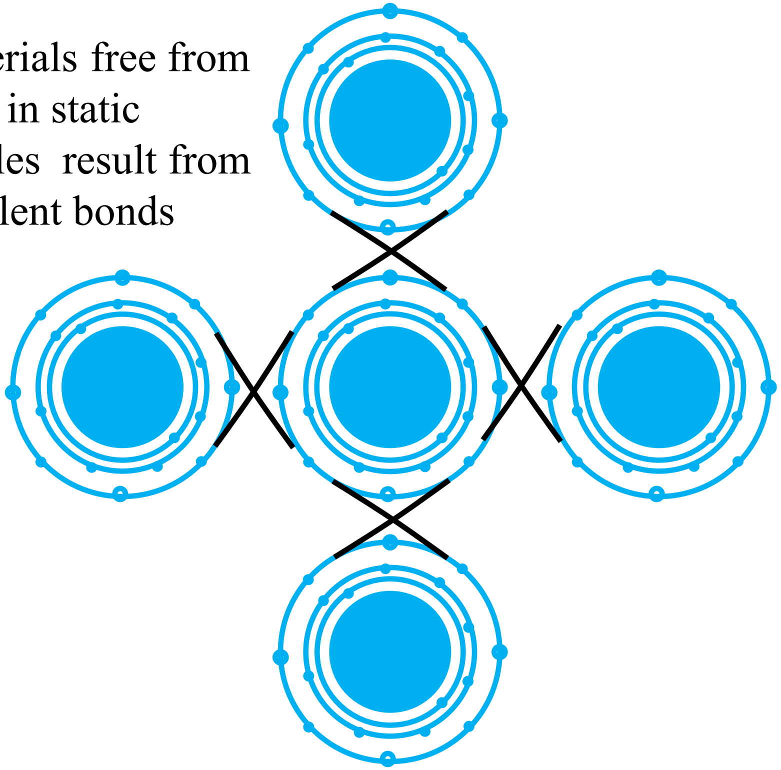
•Atoms contain various “orbitals”, “levels” or “shells” of electrons labeled as n=1, 2, 3, 4, etc… or K, L, M, or N etc… The individual allowed electrons “states” are simply allowed positions (energy and space) within each orbital/level/shell for which an electron can occupy.

•Electrons fill up the levels (fill in the individual states in the levels) from the smallest n shell to the largest occupying “states” (available orbitals) until that orbital is completely filled then going on to the next higher orbital.

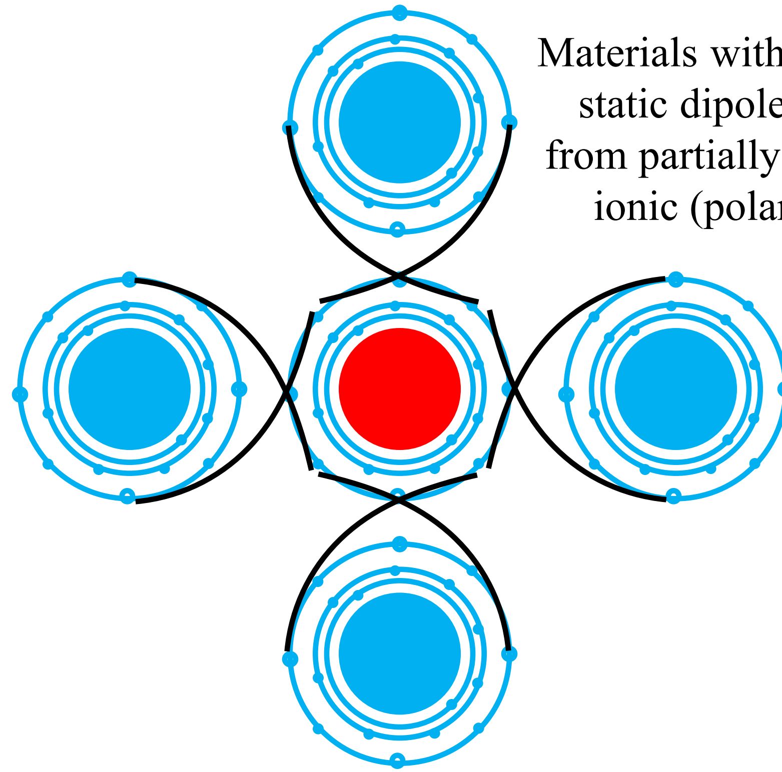
•The outer most orbital/level/shell is called the “Valence orbital”. This valence orbital si the only one that participated in the bonding of atoms together to form solids.

Classifications of Electronic Materials

Materials free from built in static dipoles result from covalent bonds

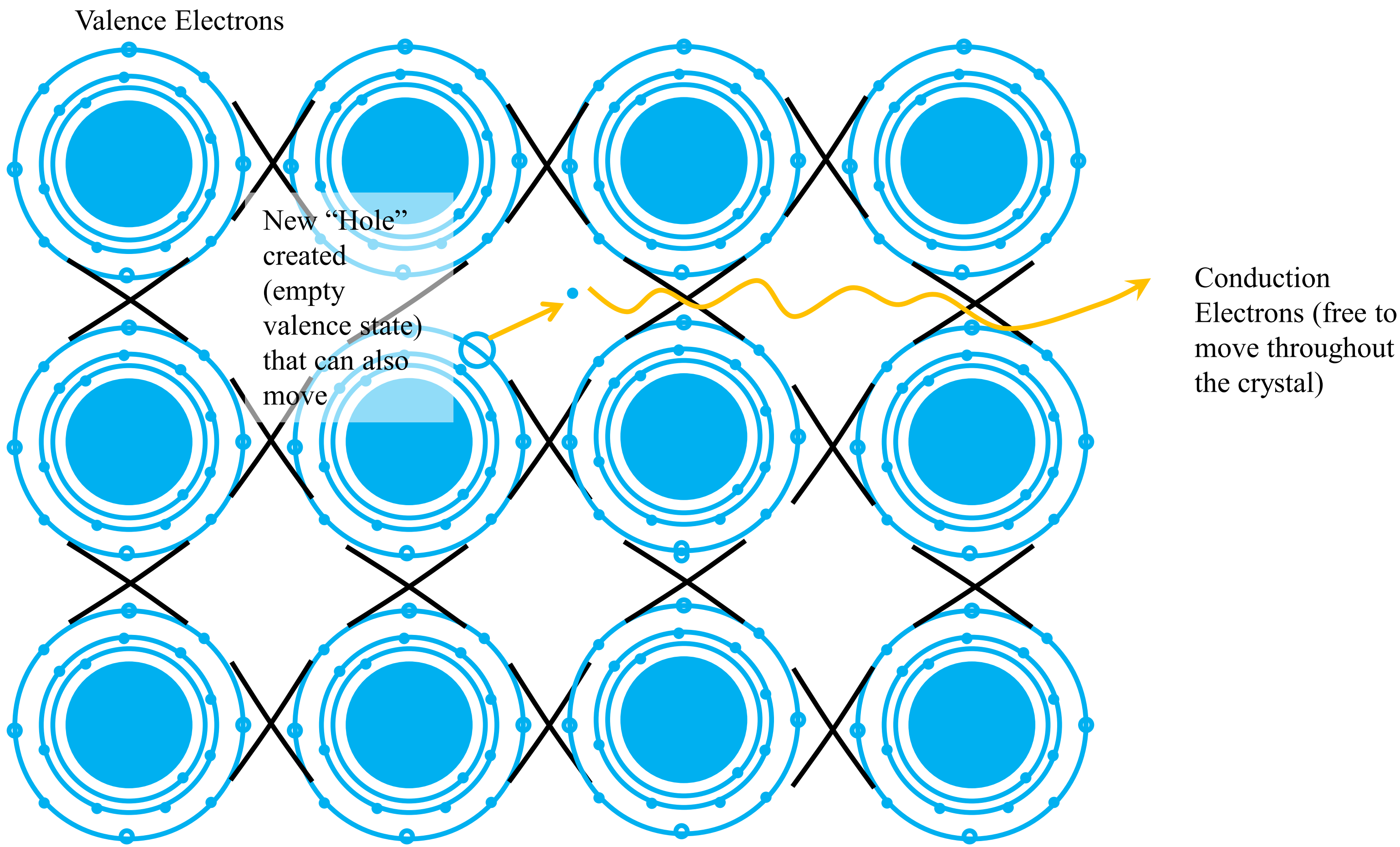


Materials with built in static dipoles result from partially or fully ionic (polar) bonds



- Solids are formed by several methods, including (but not limited to) sharing electrons (covalent bonds) or by columbic attraction of ions (fully ionic) or partial ionic attraction / partial sharing of electrons (partially ionic)
- The method for which the semiconductor forms, particularly whether or not a fixed static di-pole is constructed inside the crystal, effects the way the semiconductor interacts with light.
- Later we will see that covalent bonds tend toward “indirect bandgap” (defined later) materials whereas polar bonds (ionic and partially ionic) tend toward “direct bandgap” materials.

Classifications of Electronic Materials

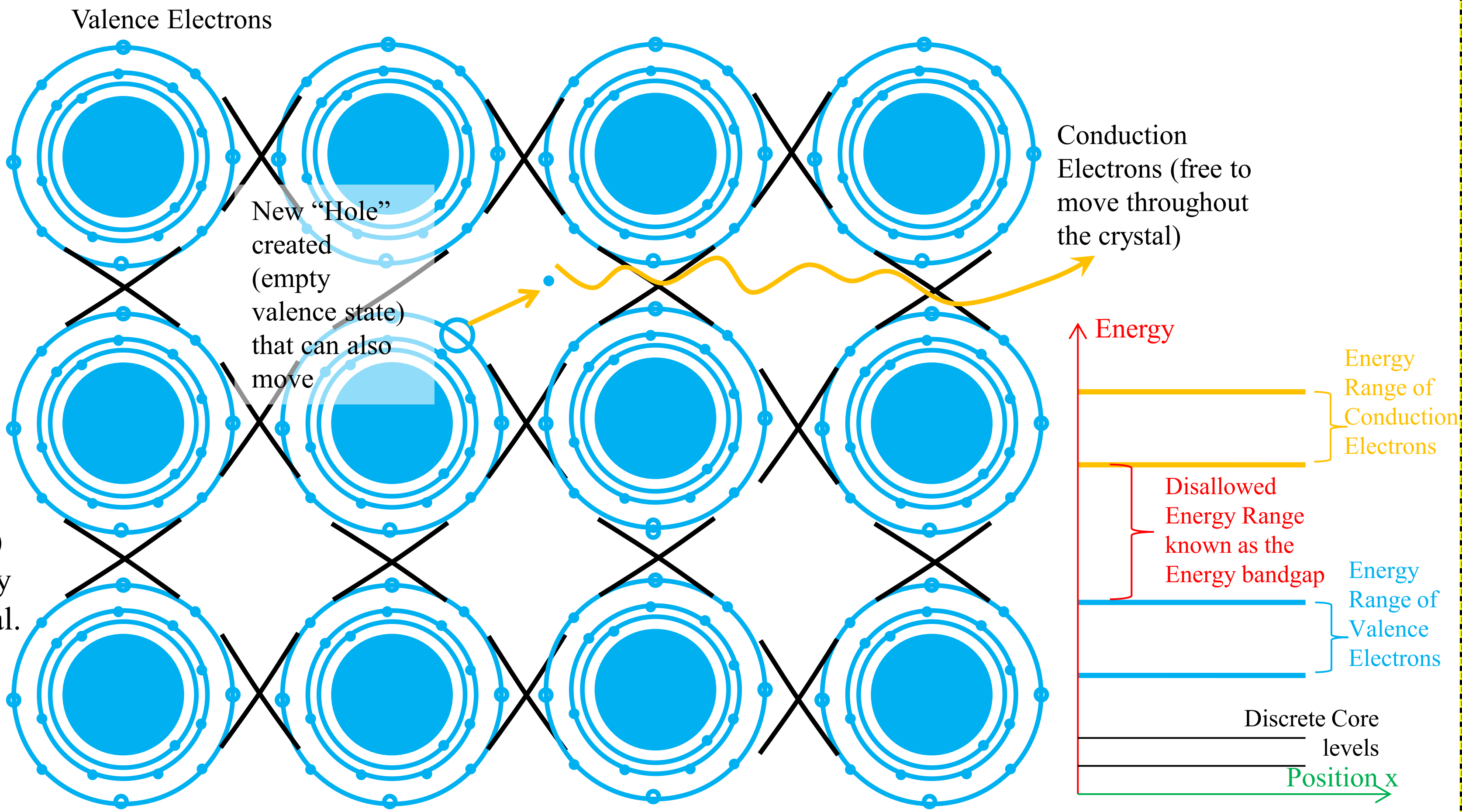


Valence electrons can gain energy (thermal, electrical, magnetic or optical energy) and break away from the crystal.

- Only the outermost core levels participate in bonding. We call these "Valance orbits" or "Valence Shells".
- For metals, the electrons can jump from the valence orbits (outermost core energy levels of the atom) to any position within the crystal (free to move throughout the crystal) with no "extra energy needed to be supplied". Thus, "free conducting electrons are prevalent at room temperature.
- For insulators, it is VERY DIFFICULT for the electrons to jump from the valence orbits and requires a huge amount of energy to "free the electron" from the atomic core. Thus, few conducting electrons exist.
- For semiconductors, the electrons can jump from the valence orbits but does require a small amount of energy to "free the electron" from the atomic core, thus making it a "***SEMI***-conductor".

Classifications of Electronic Materials

Valence electrons can gain energy (thermal, electrical, magnetic or optical energy) and break away from the crystal.



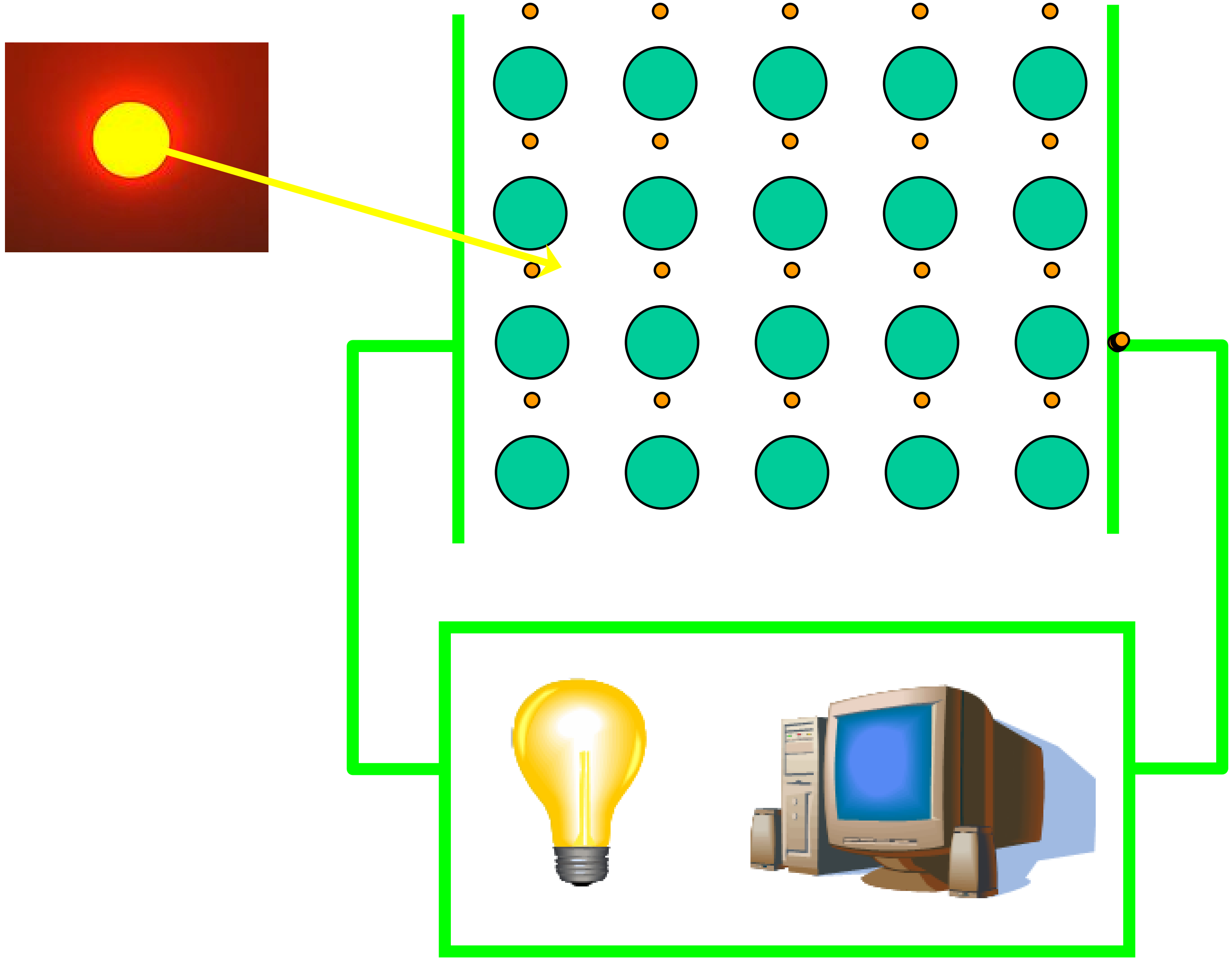
•Since the electrons in the valance orbitals of a solid can have a range of energies and since the free conducting electrons can have a range of energies, semiconductor materials are a sub-class of materials distinguished by the existence of a range of disallowed energies between the energies of the valence electrons (outermost core electrons) and the energies of electrons free to move throughout the material.

•The energy difference (**energy gap or bandgap**) between the states in which the electron is bound to the atom and when it is free to conduct throughout the crystal is related to the bonding strength of the material, it's density, the degree of ionicity of the bond, and the chemistry related to the valence of bonding.

•High bond strength materials (diamond, SiC, AlN, GaN etc...) tend to have large energy bandgaps.

•Lower bond strength materials (Si, Ge, InSb, etc...) tend to have smaller energy bandgaps.

Example: Solar Cells

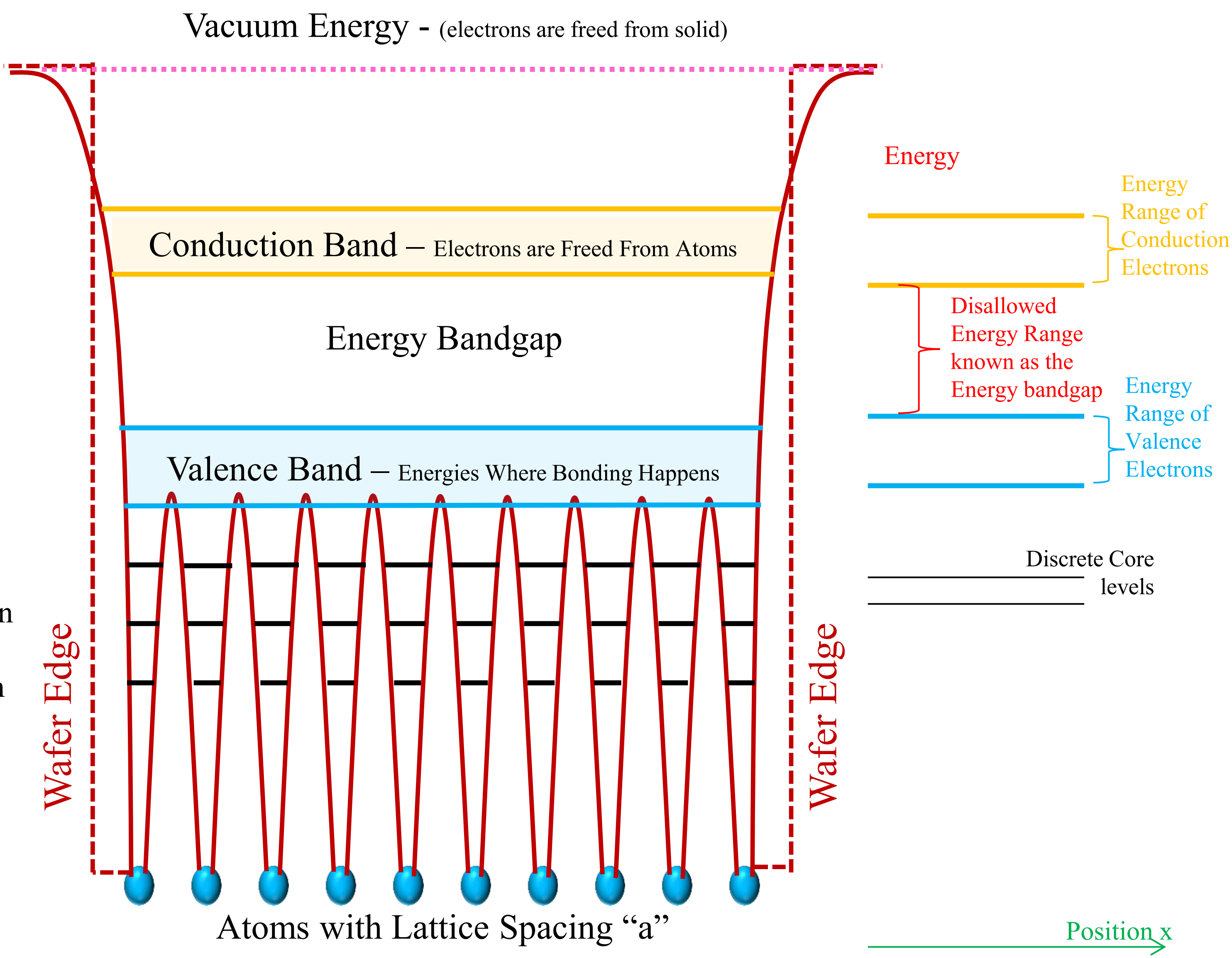


Why do the electrons flow when light is present but not flow when light is not present?

Answer, Energy Bandgap (very important concept).

Origin of Energy Bands in Semiconductors, Insulators and Metals

- A large molecular solid means all atoms are interconnected with bonds. There are many intermixed "states" inside the "quantum well" formed by the wafer edges.
- These form ranges of energies that:
  - Hold the atoms together (share bonds forming a valence band) and…
  - where electrons can gain energy (energy bandgap) and
  - be free to move within the solid. If the electrons gain enough energy (>Vacuum energy) they can be liberated form the solid itself.



Classifications of Electronic Materials

•More formally, the energy gap is derived from the Pauli exclusion principle (Physics), where no two electrons occupying the same space, can have the same energy. Thus, as atoms are brought closer towards one another and begin to bond together, their energy levels must split into bands of discrete levels so closely spaced in energy, they can be considered a continuum of allowed energy.

•Strongly bonded materials tend to have small interatomic distances between atoms (I.e very dense materials). Thus, the strongly bonded materials can have larger energy bandgaps than do weakly bonded materials.

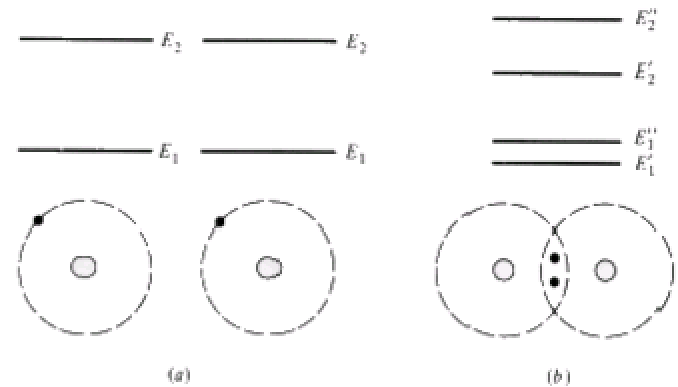
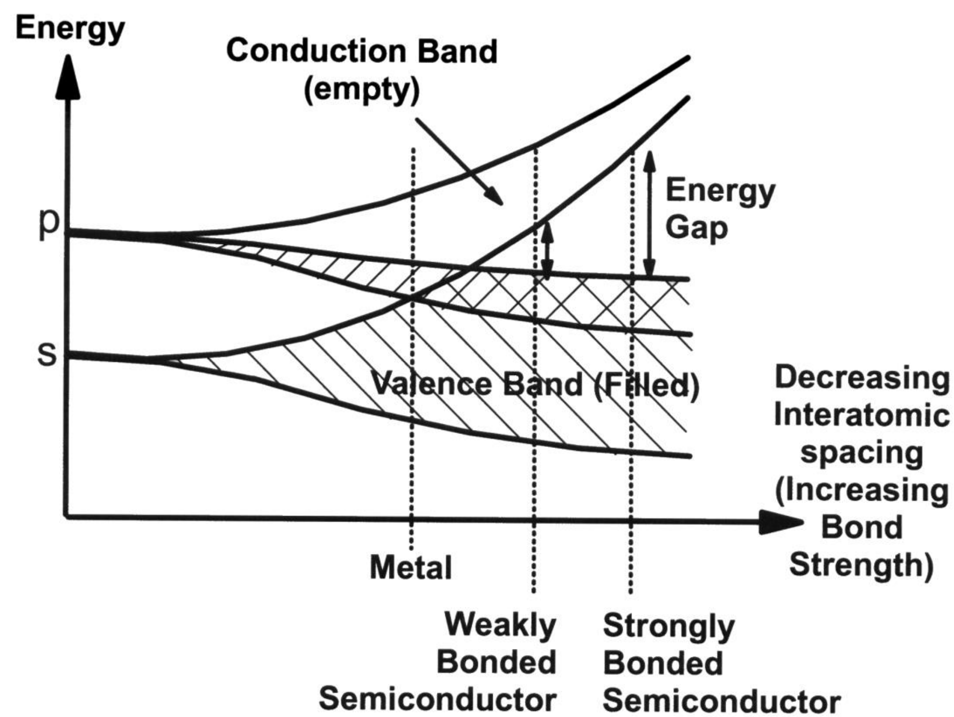
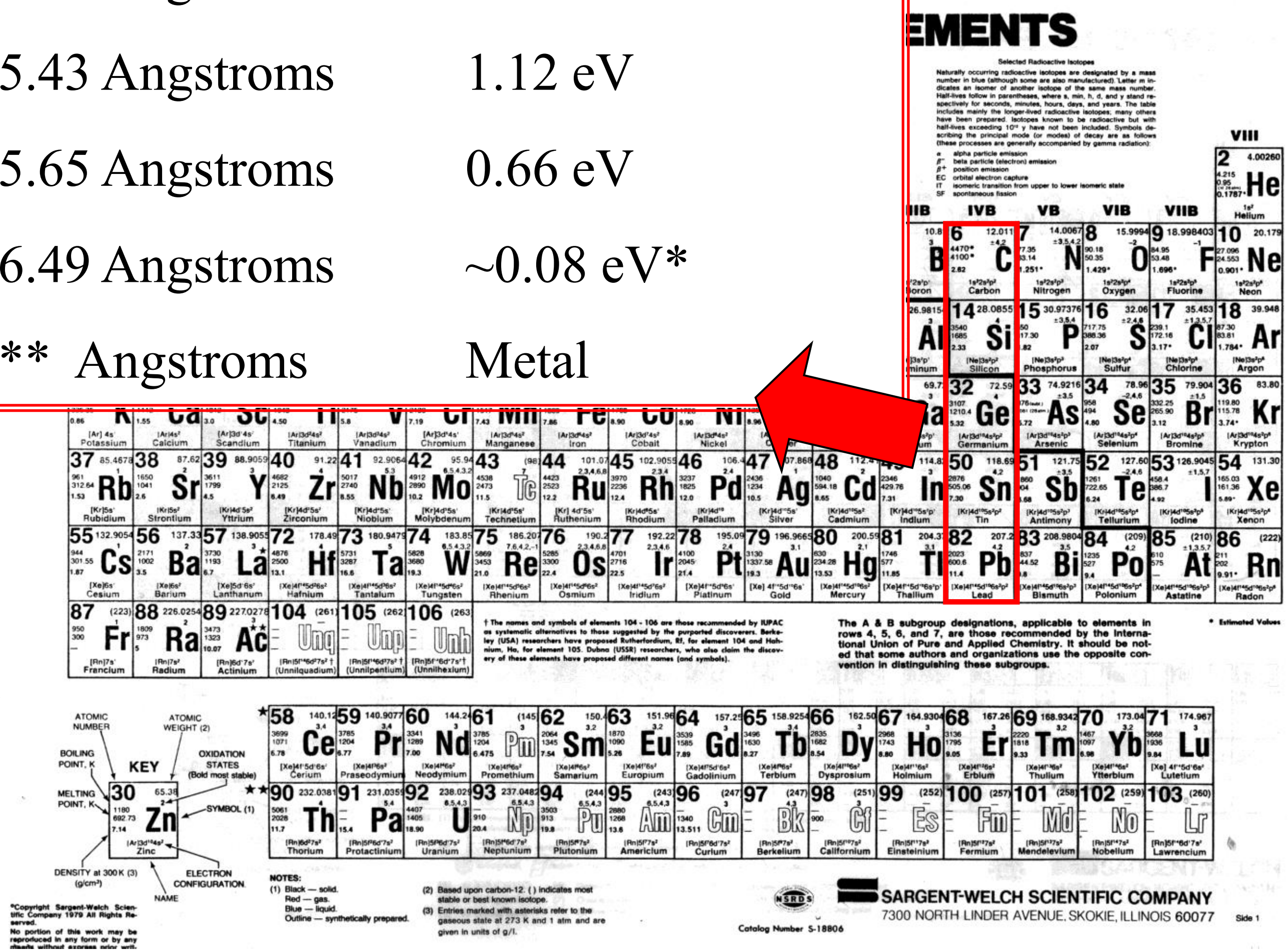


FIGURE 1-9
Two hydrogen atoms: (a) noninteracting and (b) interacting. Splitting of energy levels is illustrated for (b).



Consider the case of the group 4 elements, all** covalently bonded

Element	Atomic Radius/Lattice Constant (How closely spaced are the atoms?)	Bandgap
C	0.91/3.56 Angstroms	5.47 eV
Si	1.46/5.43 Angstroms	1.12 eV
Ge	1.52/5.65 Angstroms	0.66 eV
α-Sn	1.72/6.49 Angstroms	~0.08 eV*
Pb	1.81/** Angstroms	Metal

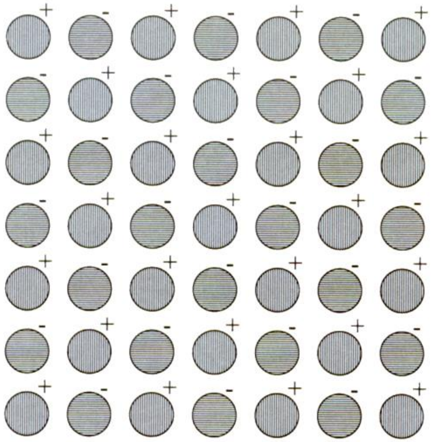


*Only has a measurable bandgap near 0K

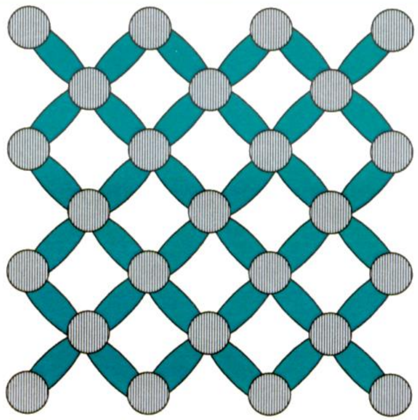
**Different bonding/Crystal Structure due to unfilled higher orbital states

Material Classifications based on Bonding Method

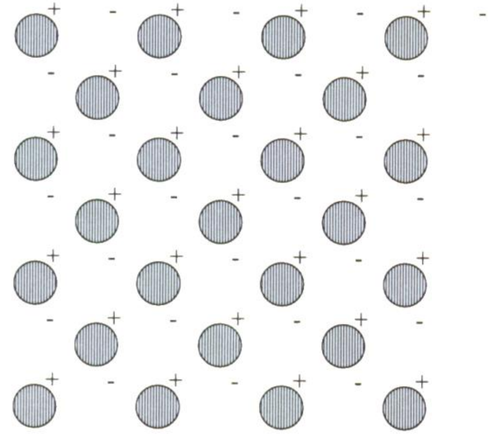
Bonds can be classified as metallic, Ionic, Covalent, and van der Waals.



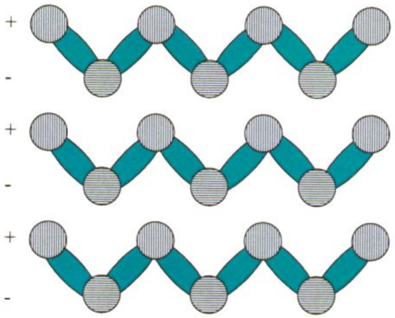
Ionic Bonding: One atom acquires and holds the electron(s) of an adjacent atom. Bonding is coulombic and strong.



Covalent Bonding: Atoms share electrons with the surrounding atoms. Bonding is moderately weak.



Metallic Bonding: Atoms give up electrons to the surrounding regions, forming an "electron cloud". Bonding is coulombic but weak due to screening of charge.



Van der Waals Bonding: Neutrally charged molecules form dipoles which are attracted to other dipoles. Bonding is extremely weak, but long chains can form.

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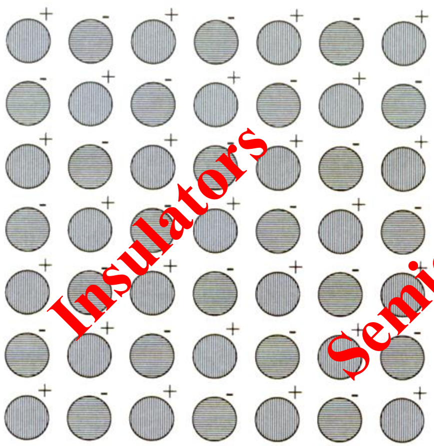

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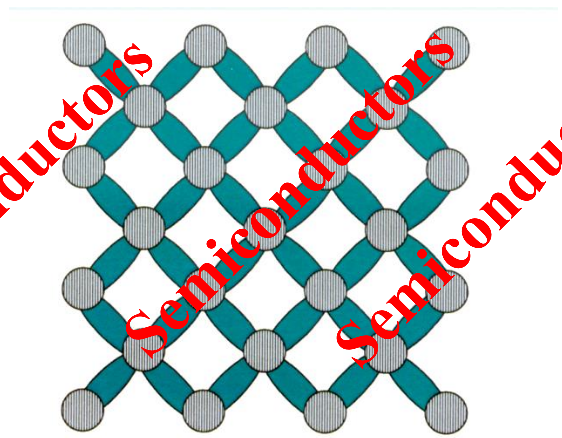

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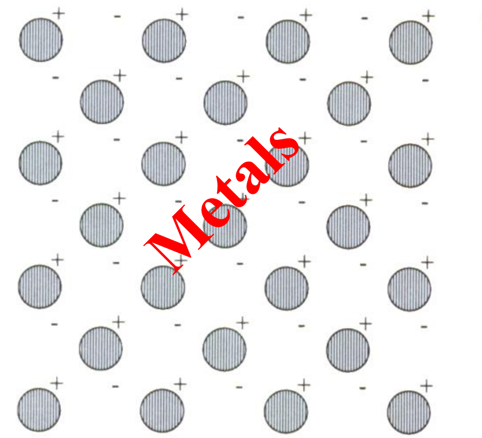

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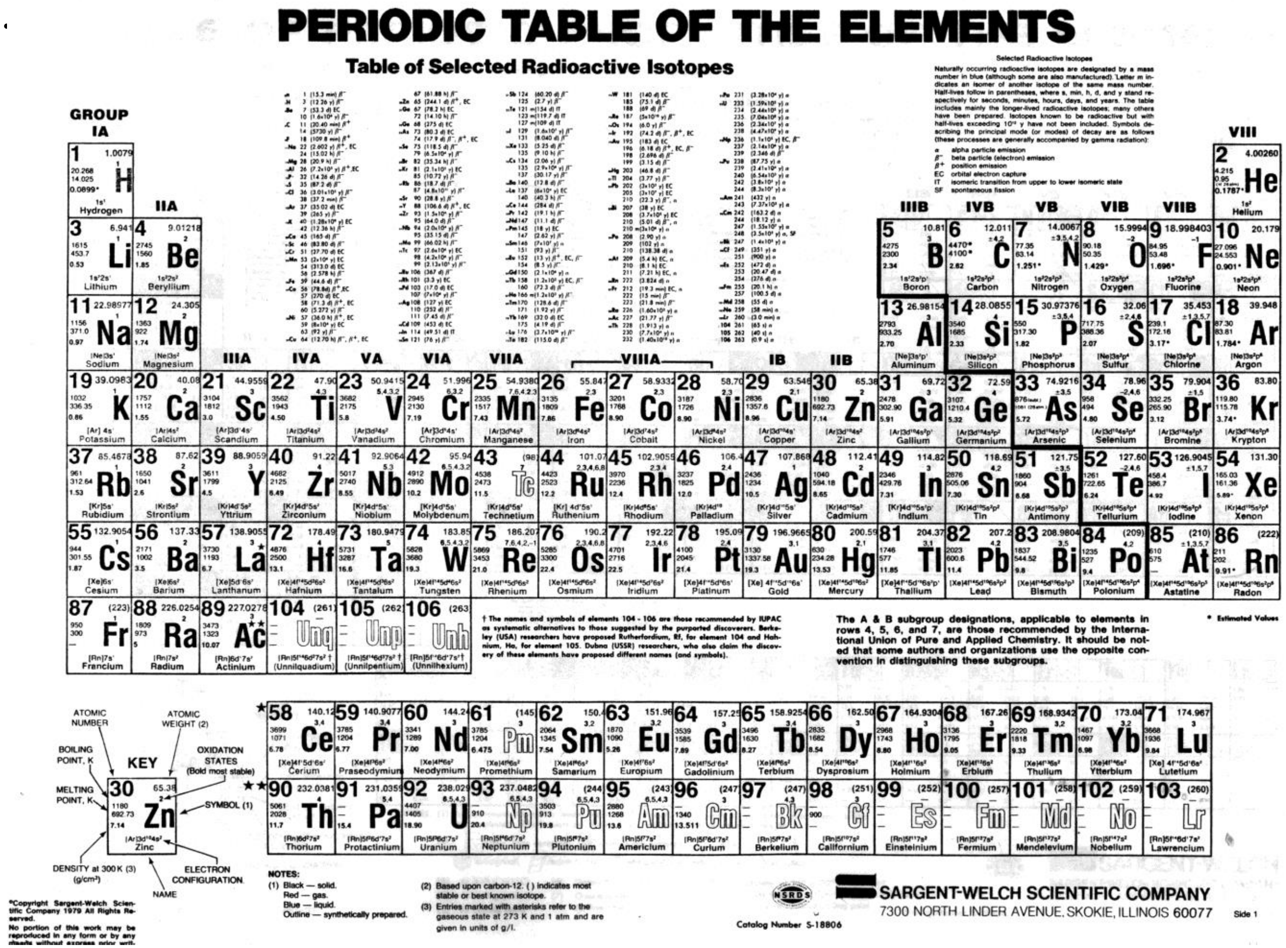
Classifications of Electronic Materials

Types of Semiconductors:

•Elemental: Silicon or Germanium (Si or Ge)

•Compound: Gallium Arsenide (GaAs), Indium Phosphide (InP), Silicon Carbide (SiC), CdS and many others

- •Note that the sum of the valence adds to 8, a complete outer shell. I.E. 4+4, 3+5, 2+6, etc...



Classifications of Electronic Materials

Compound Semiconductors: Offer high performance (optical characteristics, higher frequency, higher power) than elemental semiconductors and greater device design flexibility due to mixing of materials.

Binary: GaAs, SiC, etc...

Ternary: $Al_xGa_{1-x}As$, $In_xGa_{1-x}N$ where $0<=x<=1$

Quaternary: $In_xGa_{1-x}As_yP_{1-y}$ where $0<=x<=1$ and $0<=y<=1$

Half the total number of atoms must come from group III (Column III) and the other half the atoms must come from group V (Column V) (or more precisely, IV/IV , III/V, or II/VI combinations) leading to the above "reduced semiconductor notation.

Example: Assume a compound semiconductor has 25% "atomic" concentrations of Ga, 25% "atomic" In and 50% "atomic" of N. The chemical formula would be:

$$Ga_{0.25}In_{0.25}N_{0.5}$$

But the correct reduced semiconductor formula would be:

$$\boxed{Ga_{0.5}In_{0.5}N}$$

Classifications of Electronic Materials

General classification of solids based on the degree of atomic order: (a) amorphous, (b) polycrystalline, and (c) crystalline.

Material Classifications based on Crystal Structure

Amorphous Materials

No discernible long range atomic order (no detectable crystal structure). Examples are silicon dioxide (SiO_2), amorphous-Si, silicon nitride (Si_3N_4), and others. Though usually thought of as less perfect than crystalline materials, this class of materials is extremely useful.

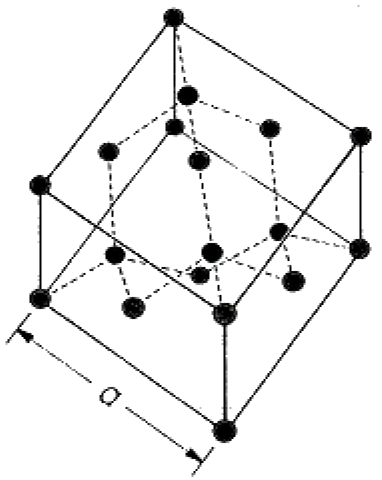
Polycrystalline Materials

Material consisting of several "domains" of crystalline material. Each domain can be oriented differently than other domains. However, within a single domain, the material is crystalline. The size of the domains may range from cubic nanometers to several cubic centimeters. Many semiconductors are polycrystalline as are most metals.

Crystalline Materials

Crystalline materials are characterized by an atomic symmetry that repeats spatially. The shape of the unit cell depends on the bonding of the material. The most common unit cell structures are diamond, zincblende (a derivative of the diamond structure), hexagonal, and rock salt (simple cubic).

Classifications of Crystalline Electronic Materials



The Diamond Crystal Structure

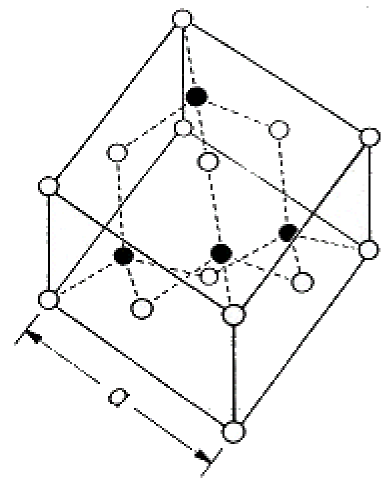
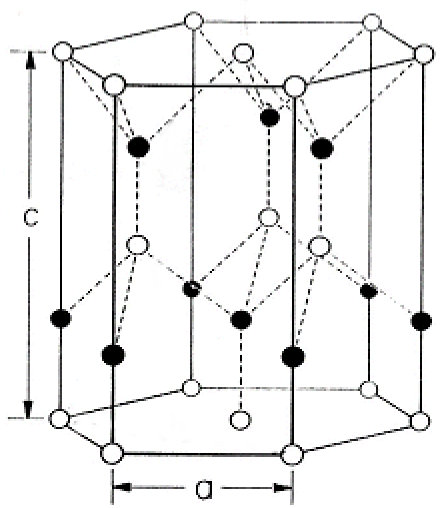


FIGURE 2 The zinc blende crystal structure.



Hexagonal (example: Wurzite)

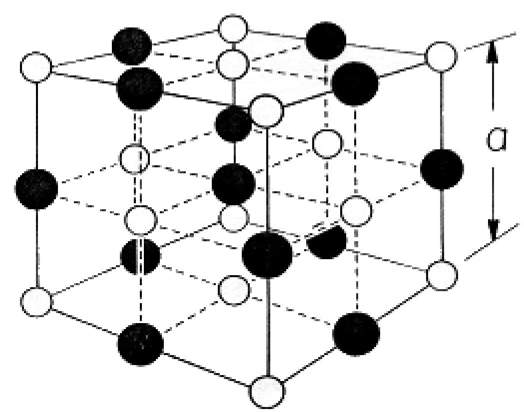
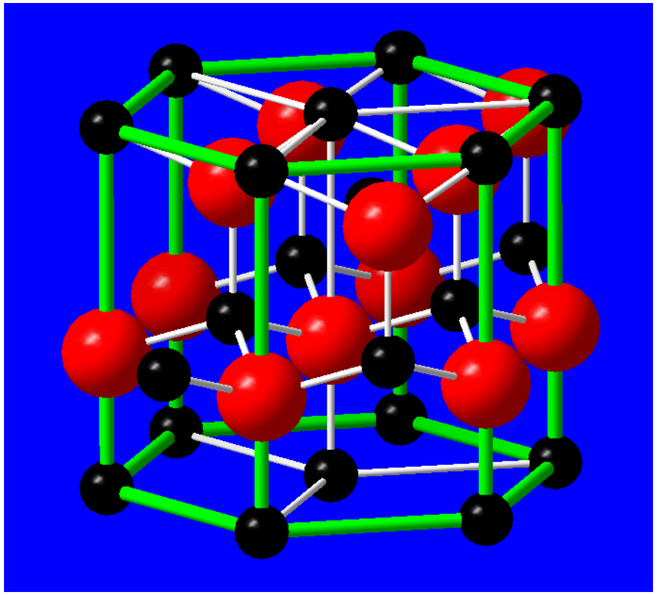


FIGURE 3 The rocksalt crystal structure.

Refer to my web page for 3D animations of crystal structures

Crystalline Order

Water Molecules, H_2O, forming "Snowflakes"



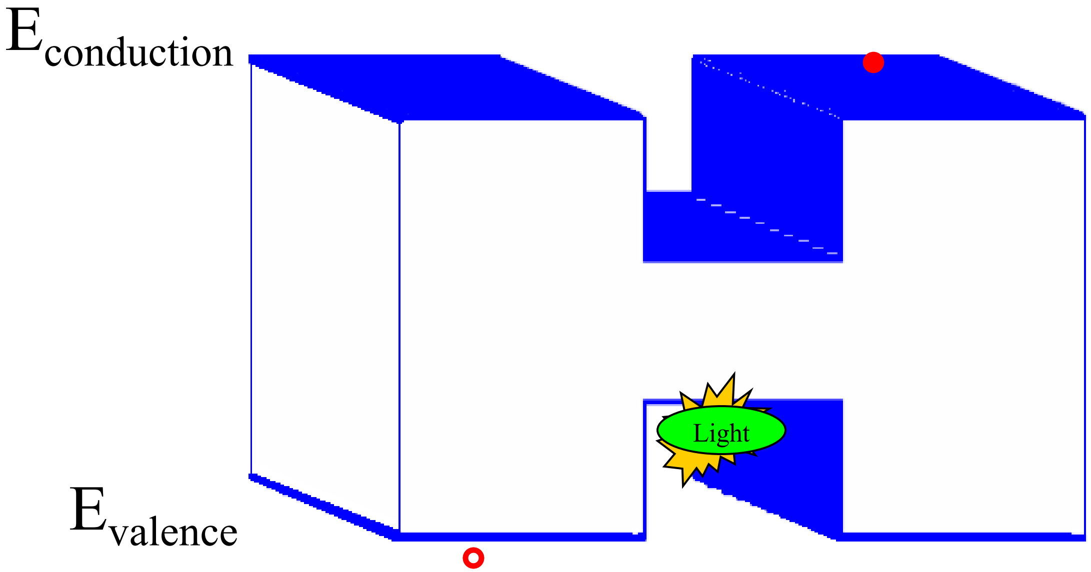
Atoms forming a "Semiconductor"

Need two volunteers… **(demo on how a crystal forms naturally due to repulsive electronic bonds)**

Classifications of Electronic Materials

Compound Semiconductors allow us to perform "Bandgap Engineering" by changing the energy bandgap as a function of position. This allows the electrons to see "engineered potentials" that "guide" electrons/holes in specific directions or even "trap" them in specific regions of devices designed by the electrical engineer.

Example: Consider the simplified band diagram of a GaN/ $Ga_{0.75}In_{0.25}N$/ GaN LED structure. Electrons and holes can be "localized" (trapped) in a very small region – enhancing the chance they will interact (recombine). This is great for light emitters!



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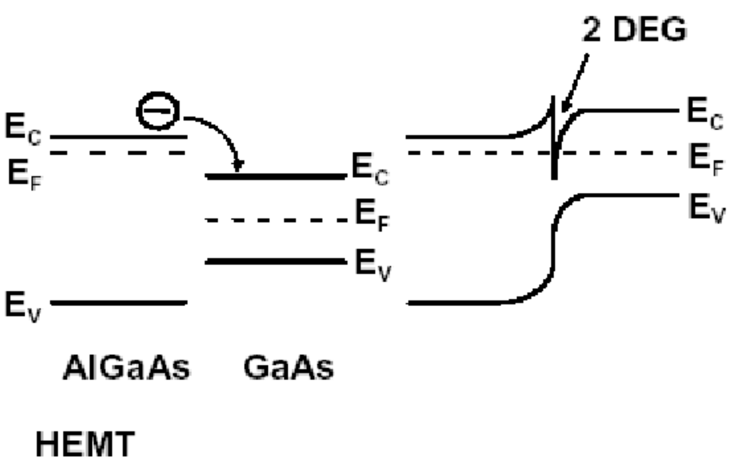
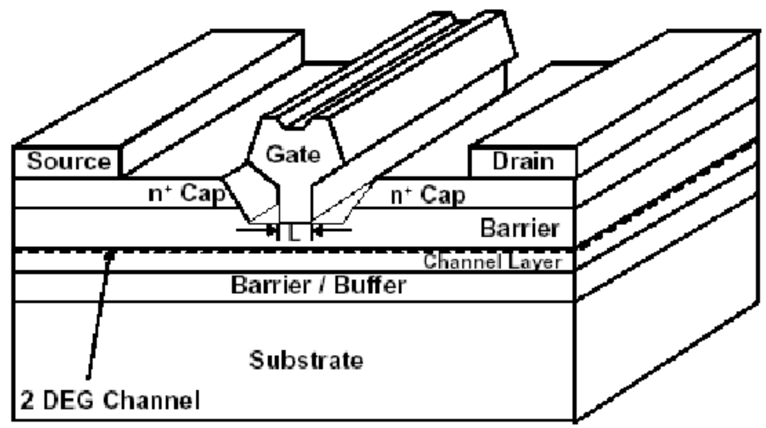
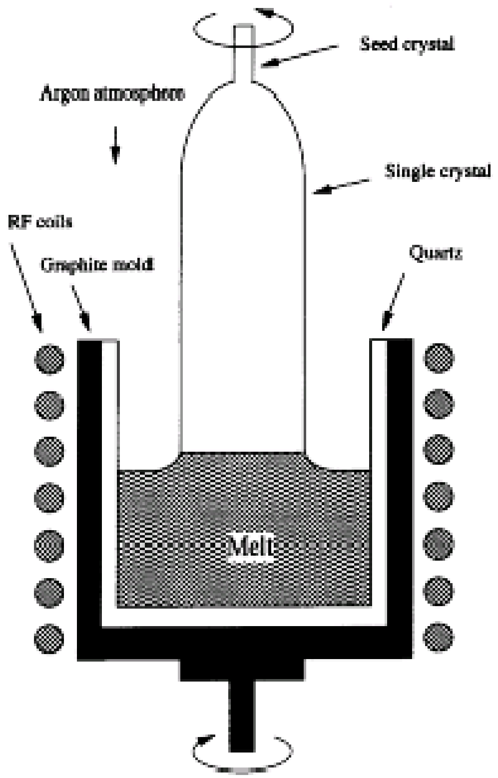
Example: Consider the band Diagram of a GaAs MODFET. Electrons in the "transistor channel" can be confined in a very thin (50-100 Angstroms) sheet known as a 2 dimensional electron gas (2DEG). This thin layer is very quickly (easily) depleted (emptied of electrons) by application of a gate voltage (repelling electrons) making such transistors very fast. This technology enables high speed communications, modern RADAR and similar applications.



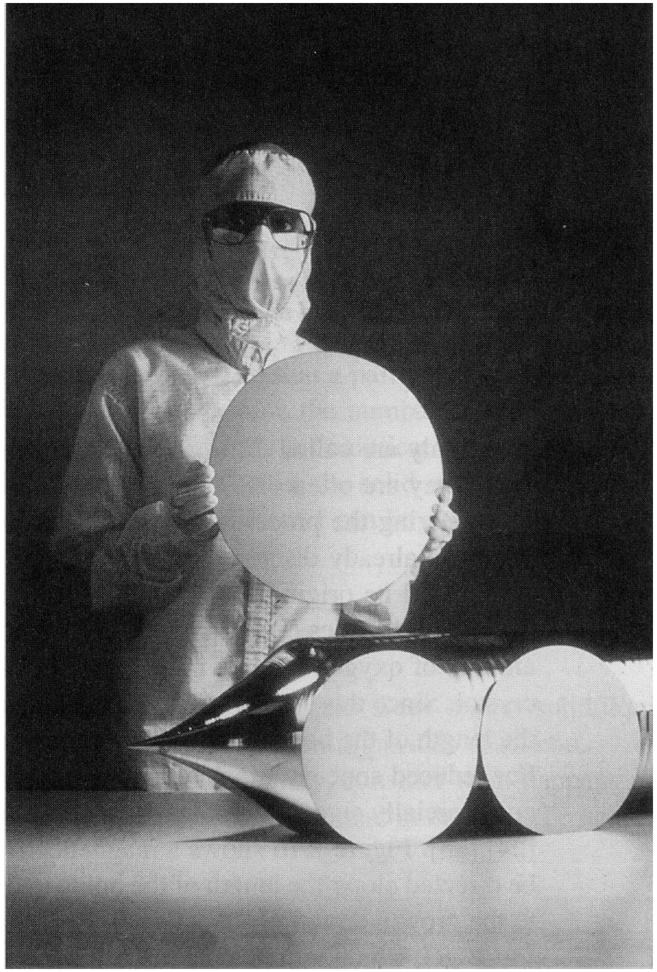


Crystal Growth: How do we get "Single Crystalline Material"?

The vast majority of crystalline silicon produced is grown by the Czochralski growth method. In this method, a single crystal seed wafer is brought into contact with a liquid Silicon charge held in a crucible (typically SiO_2 but may have a lining of silicon-nitride or other material). The seed is pulled out of the melt, allowing Si to solidify. The solidified material bonds to the seed crystal in the same atomic pattern as the seed crystal.



Schematic representation of the Czochralski (a) and float-zone (b) single-crystal growth techniques.



Crystal Growth: Adding Impurities

Impurities can be added to the melt to dope the semiconductor as p-type or n-type. Generally, impurities "prefer to stay in the liquid" as opposed to being incorporated into the solid. This process is known as segregation. The degree of segregation is characterized by the segregation coefficient, k, for the impurity,

$$k = \frac{[\text{Impurity in the Solid}]}{[\text{Impurity in the Liquid}]}$$

Impurities like Al, k_{Al}=0.002 prefers the liquid whereas B, k_B=0.8 have very little preference.

Refer to Table 2.1 in your book for more k's

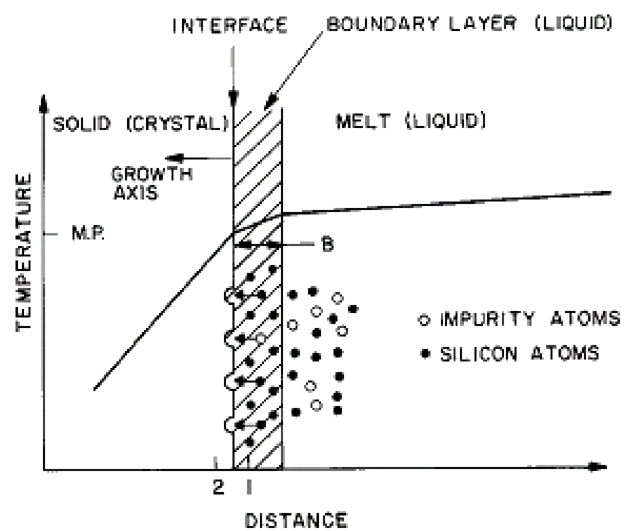


FIGURE 8
Temperature gradients, solidification, and transport phenomena involved in Czochralski growth. Positions 1 and 2 represent the location of isotherms associated with Eq. 7 and the crystal solidification at the interface. Impurity atoms are transported across the boundary layer (B) and incorporated into the growing crystal interface. M.P. is the melting point.

Crystal Growth: Float Zone Refining

Since impurities can be introduced from the melt contacting the crucible, a method of purification without contacting a crucible has been developed based on liquid-solid segregation of impurities. These crystals are more expensive and have very low oxygen and carbon and thus, are not suitable for the majority of silicon IC technology. However, for devices where a denuded zone can not be used these wafers are preferred.

Impurities are "kept out" of the single crystal by the liquid-solid segregation process.

Good for Solar cells, power electronic devices that use the entire volume of the wafer not just a thin surface layer, etc…

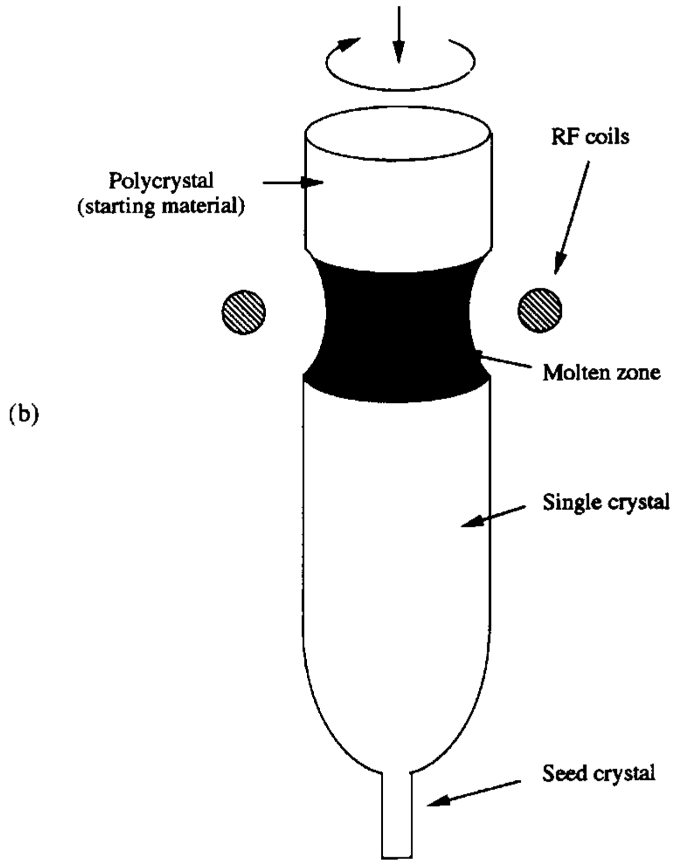


Figure 6.2 Continued.

Crystal Growth: GaAs

GaAs Liquid Encapsulated CZ (LEC)

GaAs is more difficult. At 1238 C, the vapor pressure of As is ~10 atmospheres while Ga is only ~0.001 atmospheres. Thus, at these temperatures, As is rapidly lost to evaporation resulting in a non-stoichiometric melt. (Recall from the phase diagram that 50% Ga and 50% As is required to get pure GaAs). Thus, a cap is used to encapsulate the melt. This cap is typically Boric oxide (B_2O_3) and melts at ~400 C, allowing the seed crystal to be lowered through the cap and pulled out of the cap.

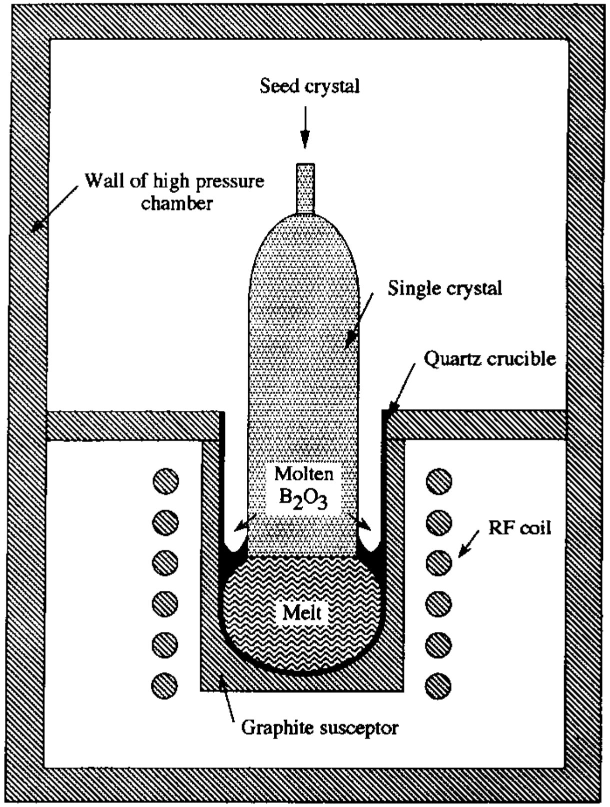


Figure 7.4 Schematic representation of the LEC technique for the growth of GaAs single crystals.

Crystal Growth: GaAs

Horizontal Bridgman GaAs Growth

Historically, limitations on defect densities possible with LEC limit the use of LEC wafers to electronic applications. Most GaAs for optoelectronics (requiring low defect densities) is produced by the bridgman method. In this method and it's many variants, the GaAs charge is held in a sealed ampoule with excess arsenic. Thus, higher pressures can be reached that limit As evaporation. The charge is heated, partially melted with the melt then brought into contact with a seed crystal. The molten region is then moved through the charge allowing the trailing edge of the molten region to solidify into a low defect single crystal while the leading edge of the molten region melts more of the charge.

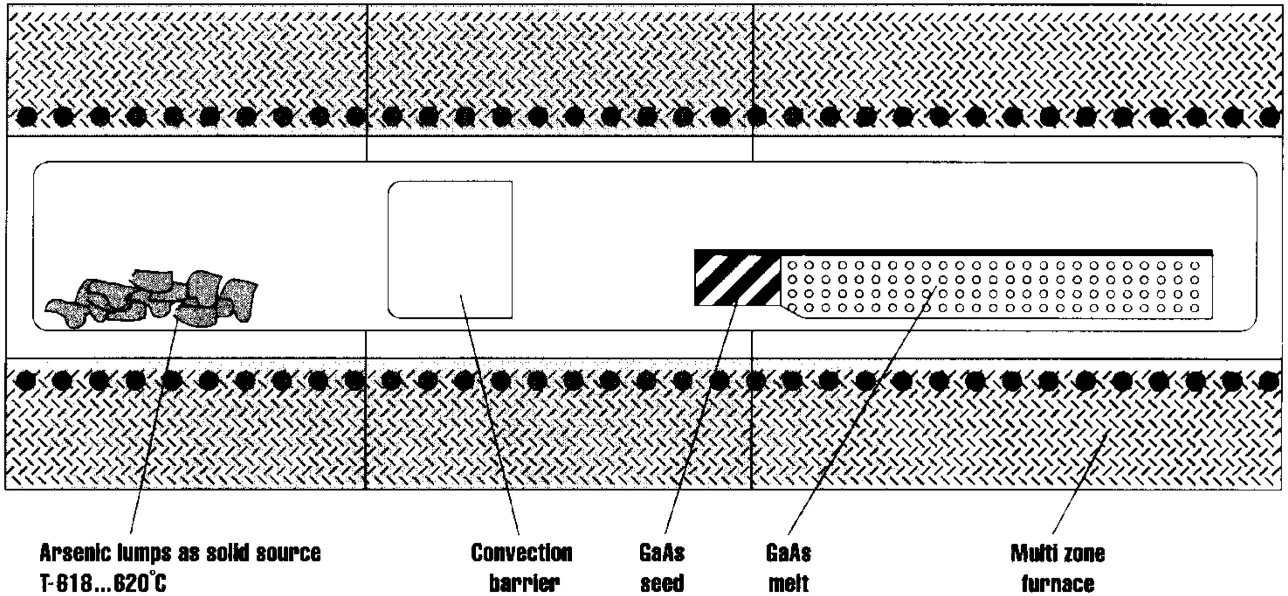


Figure 2-19 Schematic of a horizontal Bridgman growth system *(after Sell)*.

Classifications of the many processes used in Microelectronics Technology…an Example

Unit I: Hot (or energetic) Processes

- Diffusion (chapter 3)
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- Ion Implantation (chapter 5)
- Rapid Thermal Processing (chapter 6)

Unit II: Pattern Transfer

- Optical Lithography (chapter 7)
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- Non-Optical Lithographic Techniques (chapter 9)
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- Etching (chapter 11)

Unit III: Thin Films

- Physical Deposition: Evaporation and Sputtering (chapter 12)
- Chemical Vapor Deposition (chapter 13)
- Epitaxial Growth (chapter 14)

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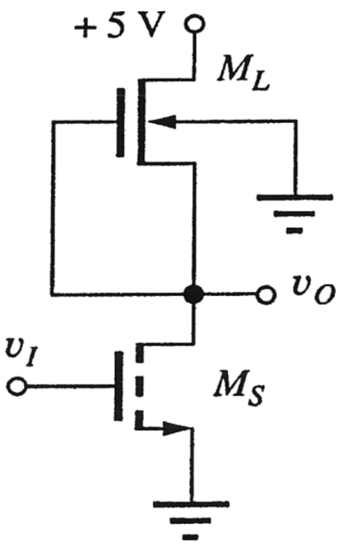
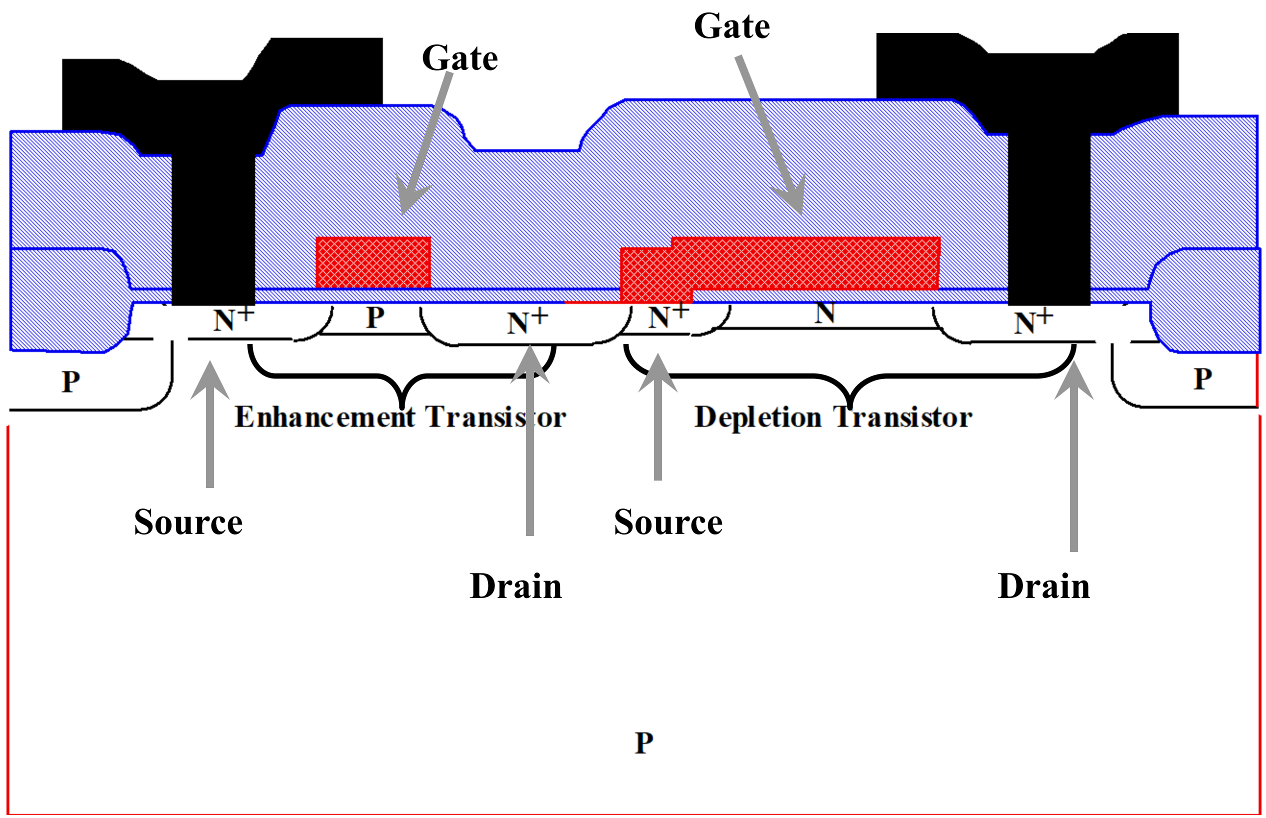
- Selected topics from Silicon (chapters 16 & 18), GaAs (chapter 17) and yield Analysis (chapter 19)

The Need for Multidisciplinary Understanding:

Consider the simple inverter in NMOS technology using Depletion Load Transistors

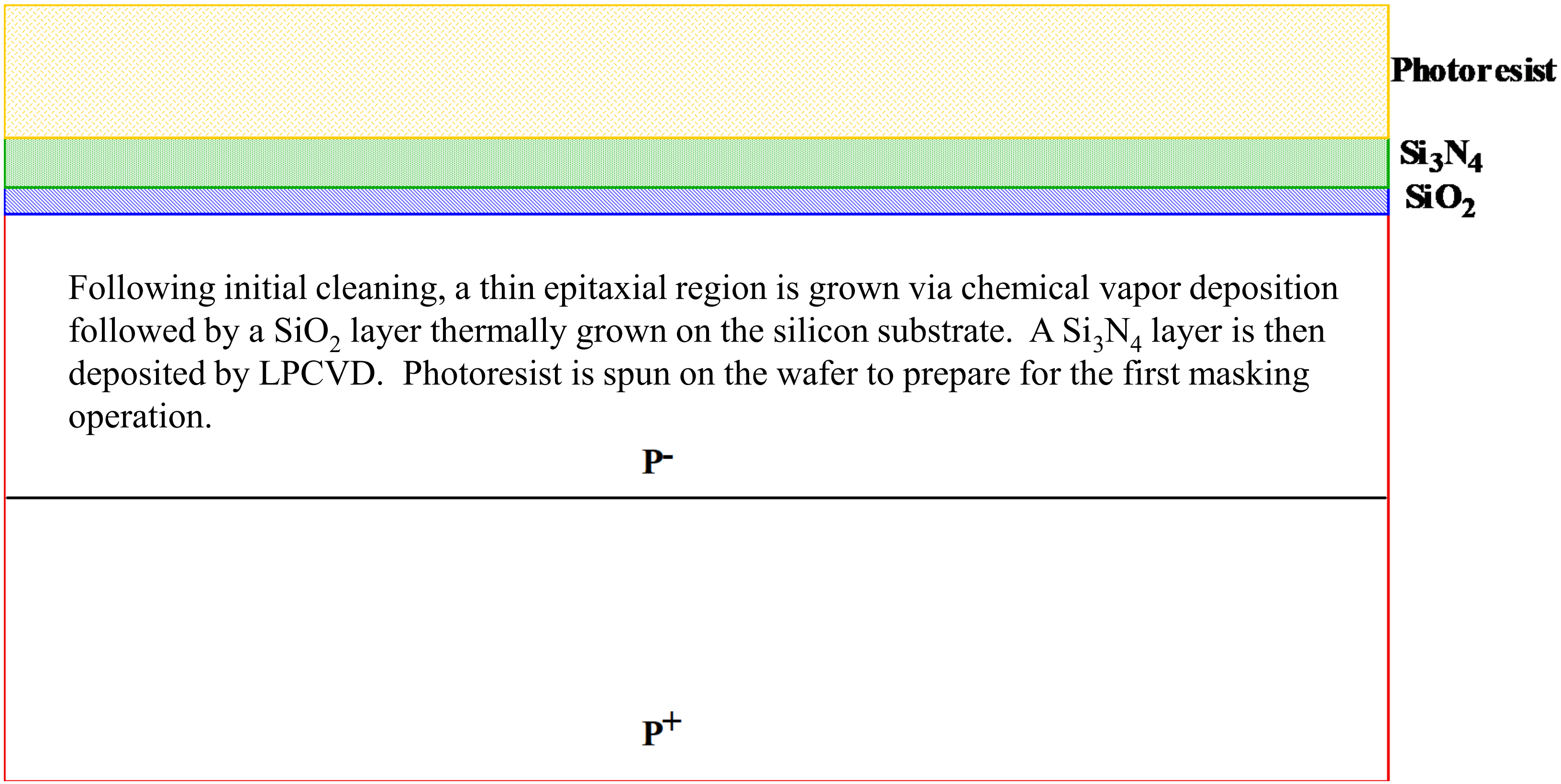




Both MOSFETS are NMOS (n-channel)

Enhancement Mode: Normally Off (have to do something to get it to conduct electricity)

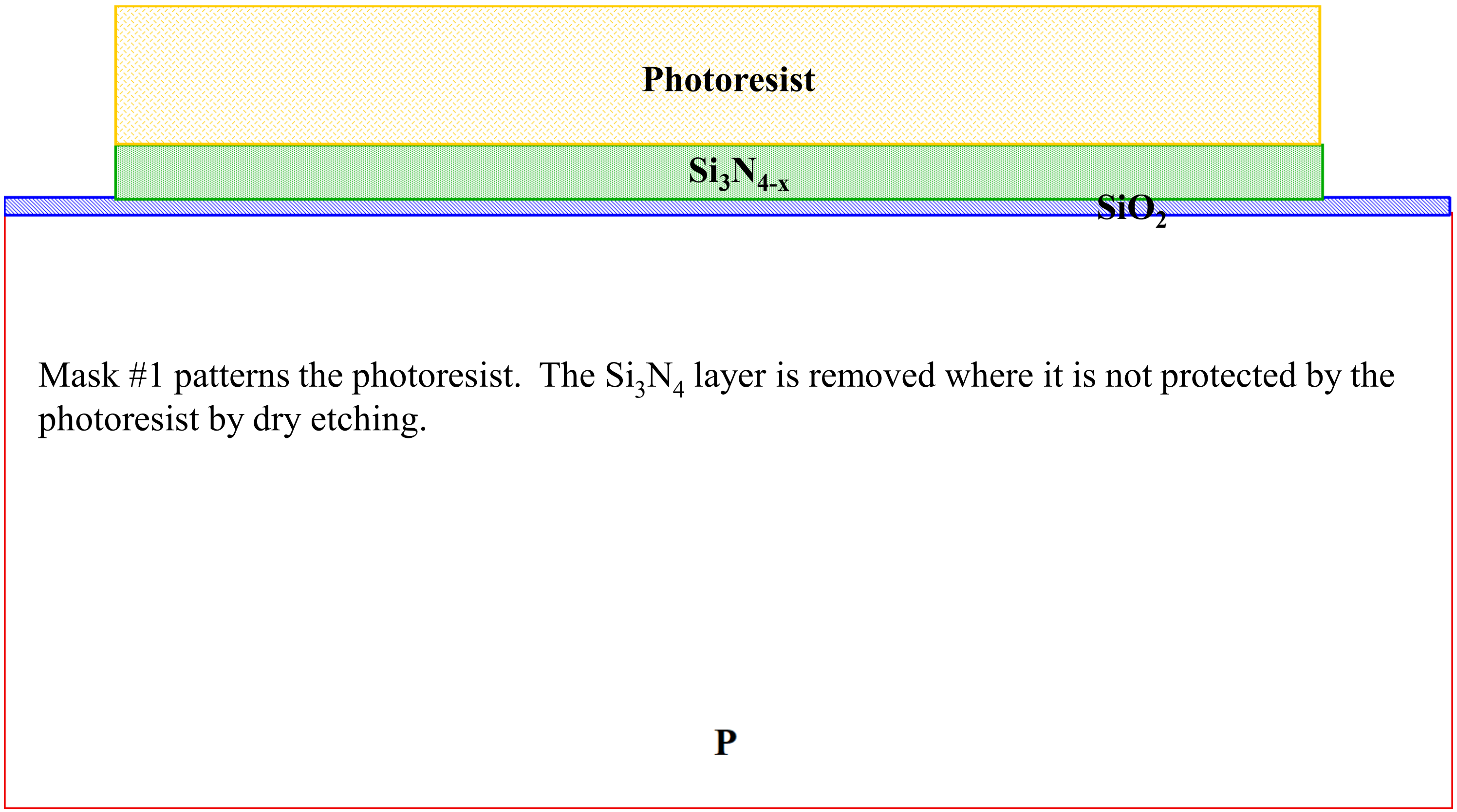
Depletion Mode: Normally On (have to do something to get it to stop conducting electricity)



Following initial cleaning, a thin epitaxial region is grown via chemical vapor deposition followed by a SiO_2 layer thermally grown on the silicon substrate. A Si_3N_4 layer is then deposited by LPCVD. Photoresist is spun on the wafer to prepare for the first masking operation.

Disciplines Used: ECE (choice of p-type layers and doping concentrations), Chemistry (CVD), MSE (solid solutions of dopants), Physics (small devices)

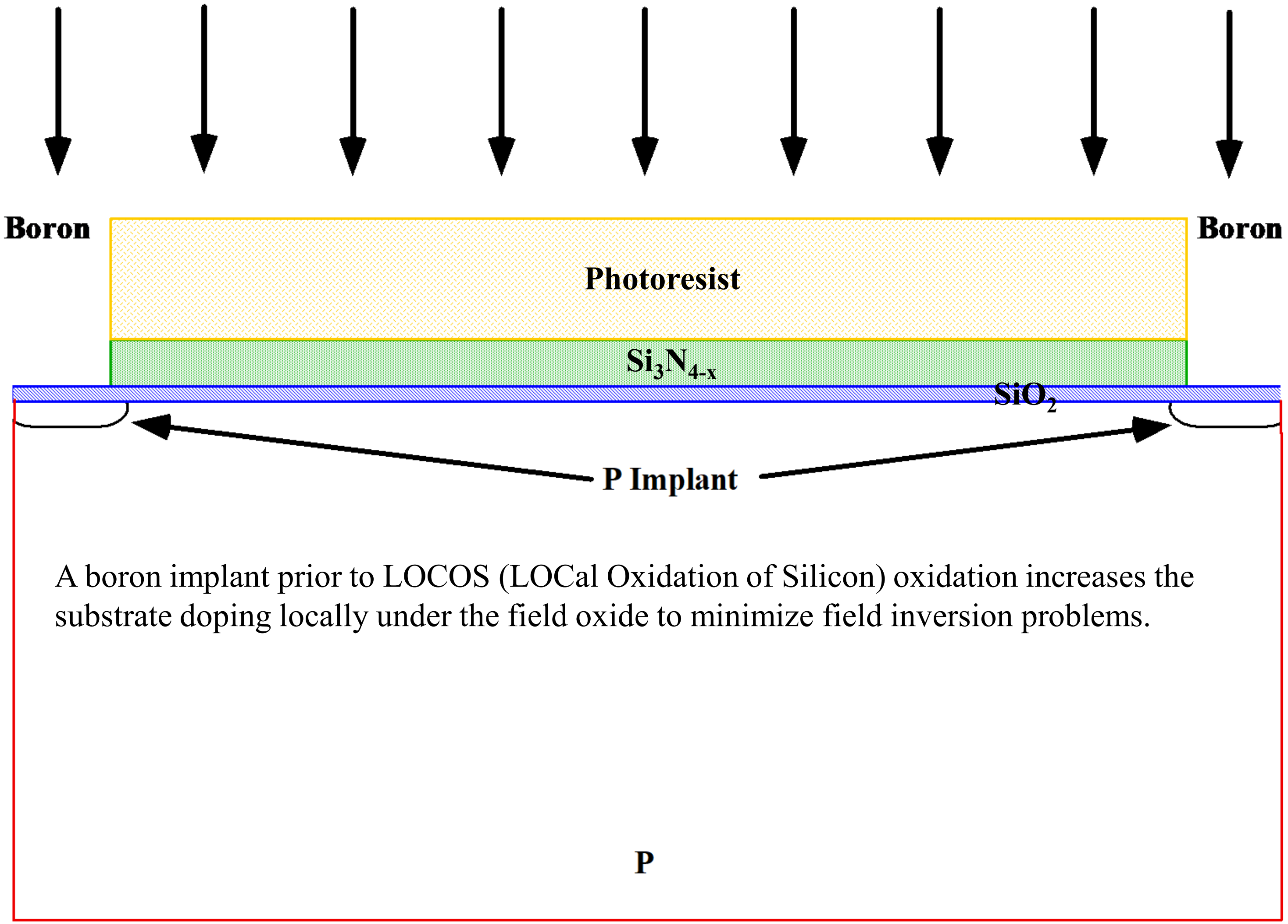
Materials Used: Crystalline Semiconductors, amorphous dielectrics, polymers



Mask #1 patterns the photoresist. The Si_3N_4 layer is removed where it is not protected by the photoresist by dry etching.

Disciplines Used: Chemistry (etching), Physics (optics/diffraction, plasma physics)

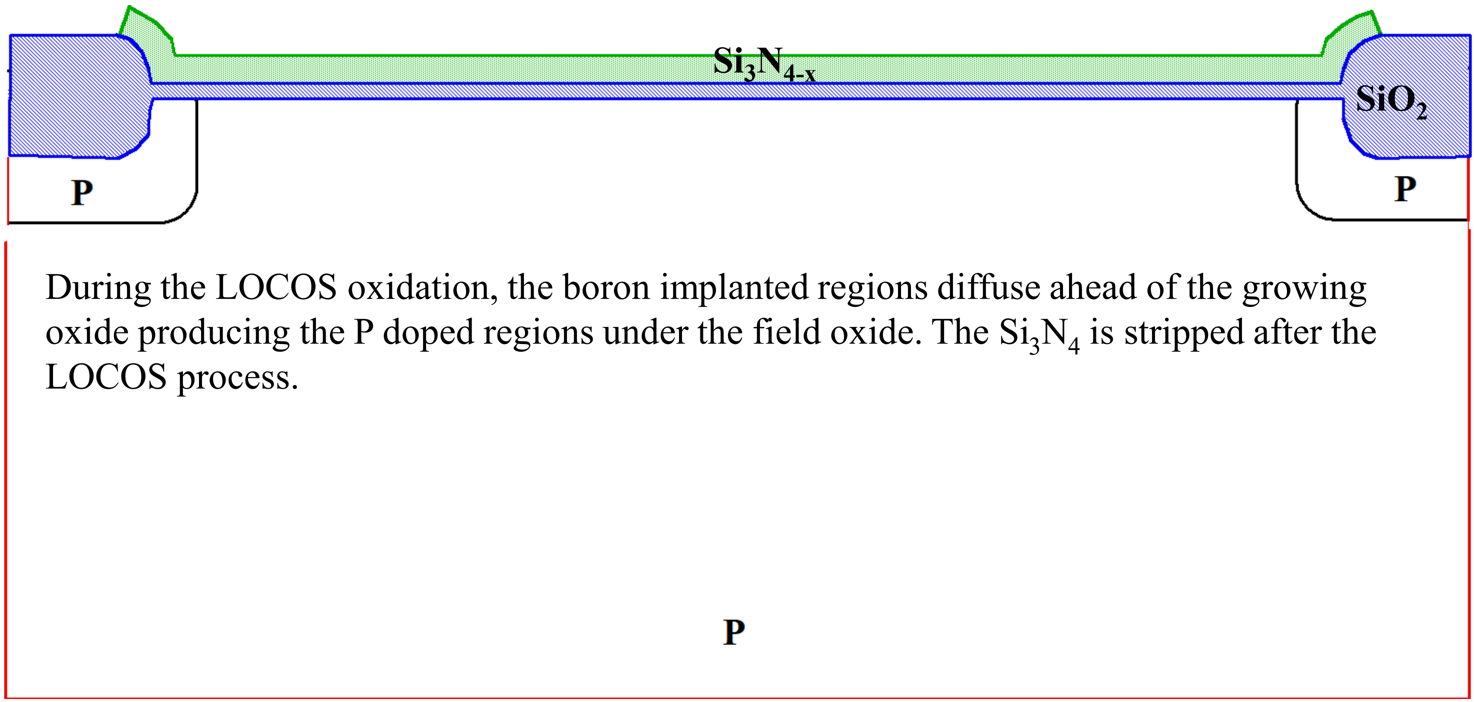
Materials Used: Acids, bases, dry plasmas, Crystalline Semiconductors, amorphous dielectrics, polymers



A boron implant prior to LOCOS (LOCal Oxidation of Silicon) oxidation increases the substrate doping locally under the field oxide to minimize field inversion problems.

Disciplines Used: ECE (electrical design of edge termination layers), Chemistry (choice of dopants), MSE (solid solutions of dopants), Physics (Ion bombardment)

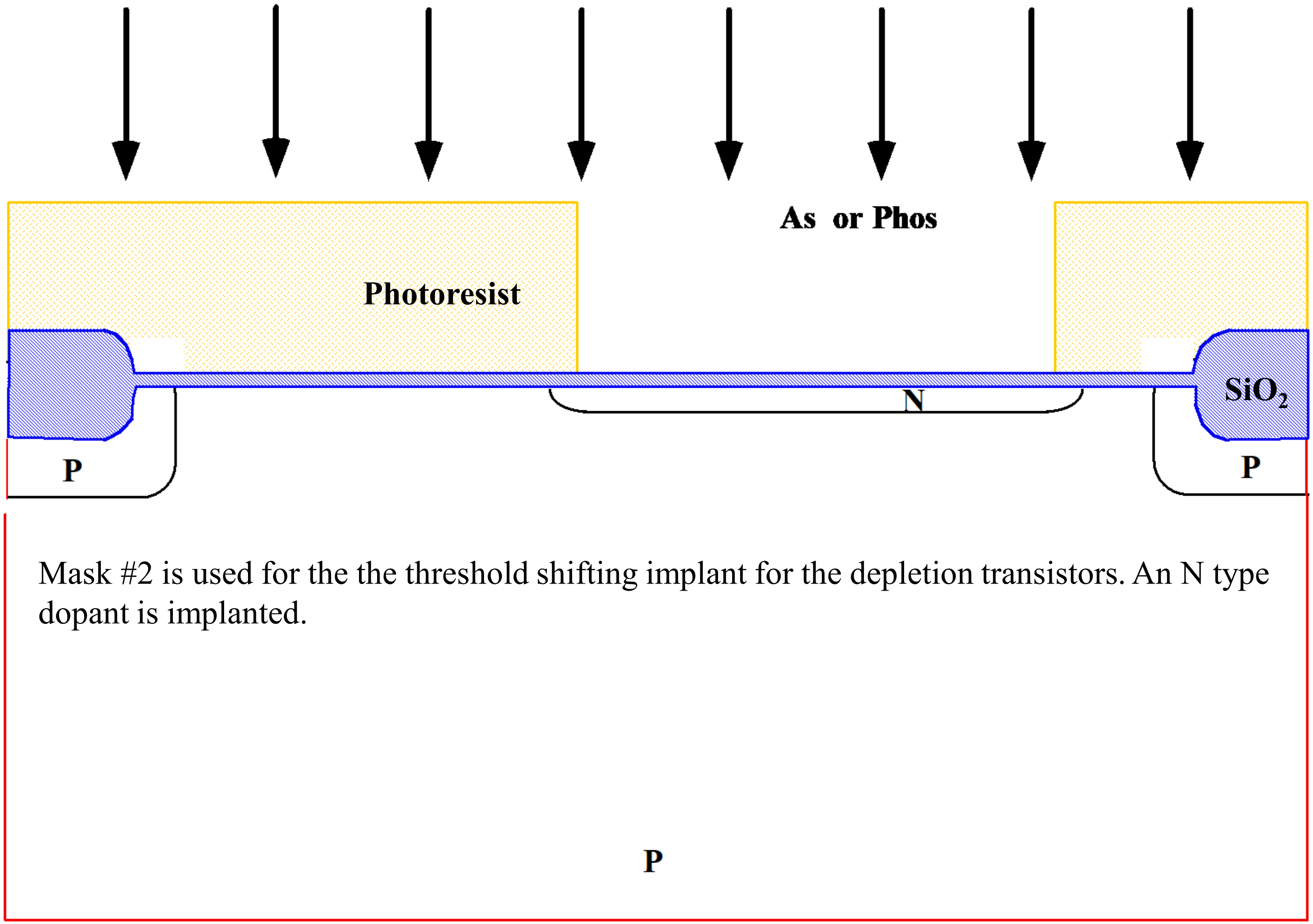
Materials Used: Crystalline Semiconductors, amorphous dielectrics, polymers



During the LOCOS oxidation, the boron implanted regions diffuse ahead of the growing oxide producing the P doped regions under the field oxide. The Si_3N_4 is stripped after the LOCOS process.

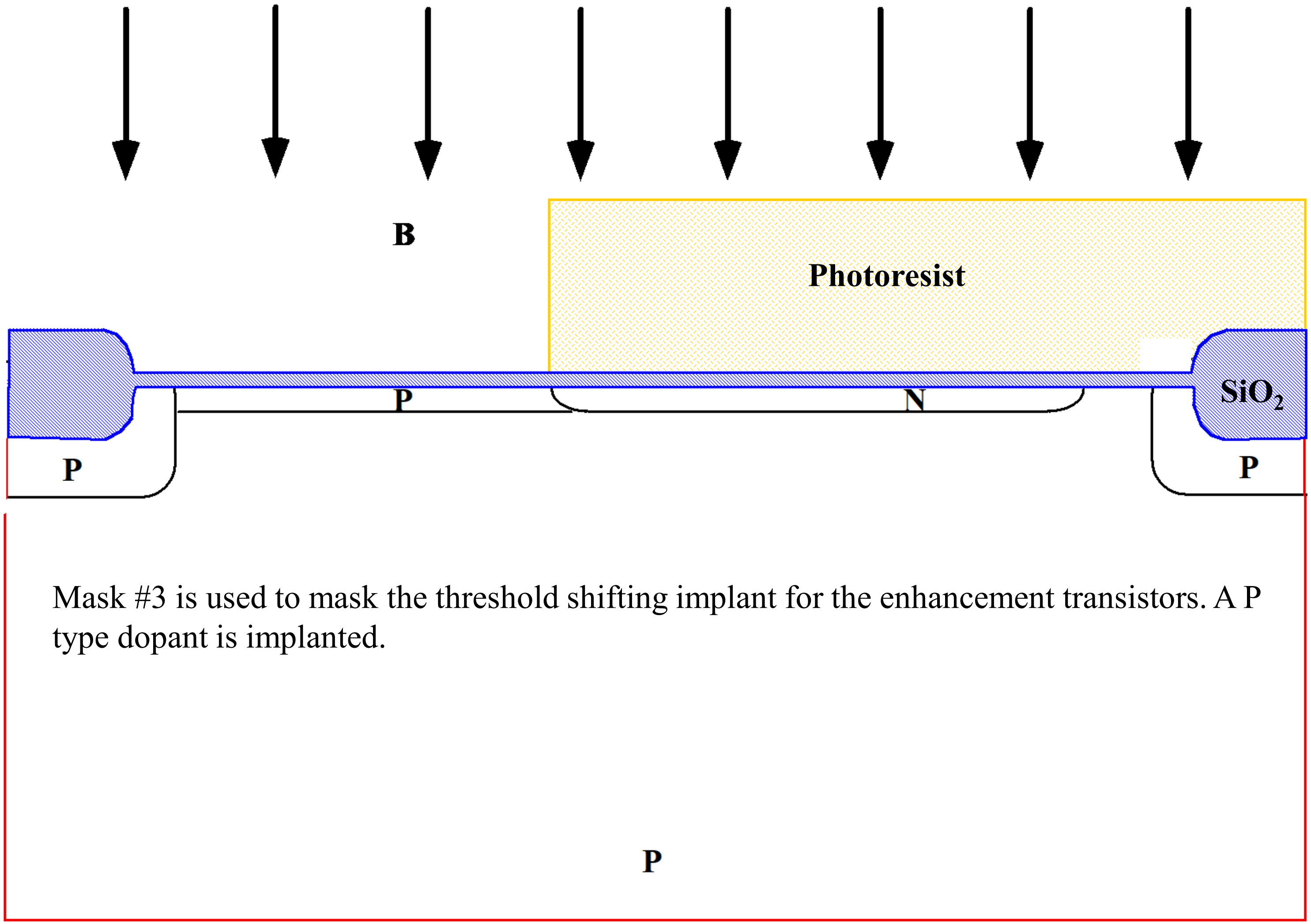
Disciplines Used: ECE (electrical design of isolation), Chemistry (oxidation reactions and barriers), MSE (solid solutions of dopants)

Materials Used: Amorphous dielectrics, toxic/corrosive gases



Disciplines Used: ECE (electrical design of channel), Chemistry (choice of dopants), MSE (solid solutions of dopants), Physics (Ion bombardment)

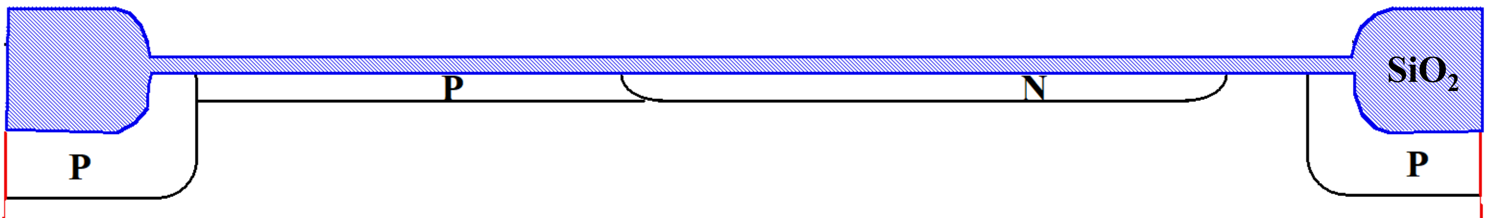
Materials Used: Crystalline Semiconductors, amorphous dielectrics, polymers, and ions



Mask #3 is used to mask the threshold shifting implant for the enhancement transistors. A P type dopant is implanted.

Disciplines Used: ECE (electrical design of channel), Chemistry (choice of dopants), MSE (solid solutions of dopants), Physics (Ion bombardment)

Materials Used: Crystalline Semiconductors, amorphous dielectrics, polymers, and ions

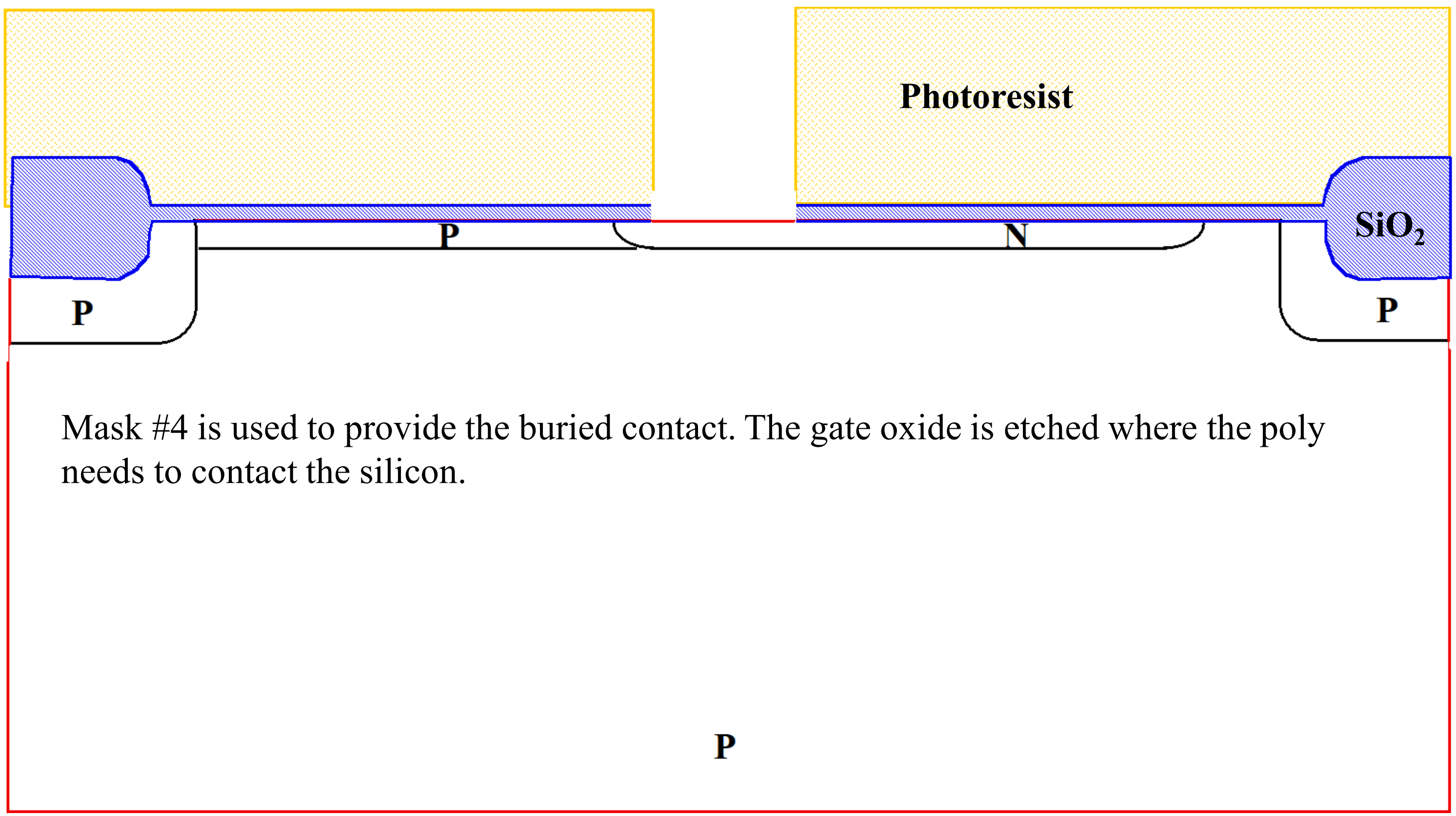


After etching back the thin oxide to bare silicon, the gate oxide is grown for the MOS transistors.

P

Disciplines Used: ECE (electrical design of isolation, electrical reliability), Chemistry (oxidation reactions), MSE (solid solutions of dopants)

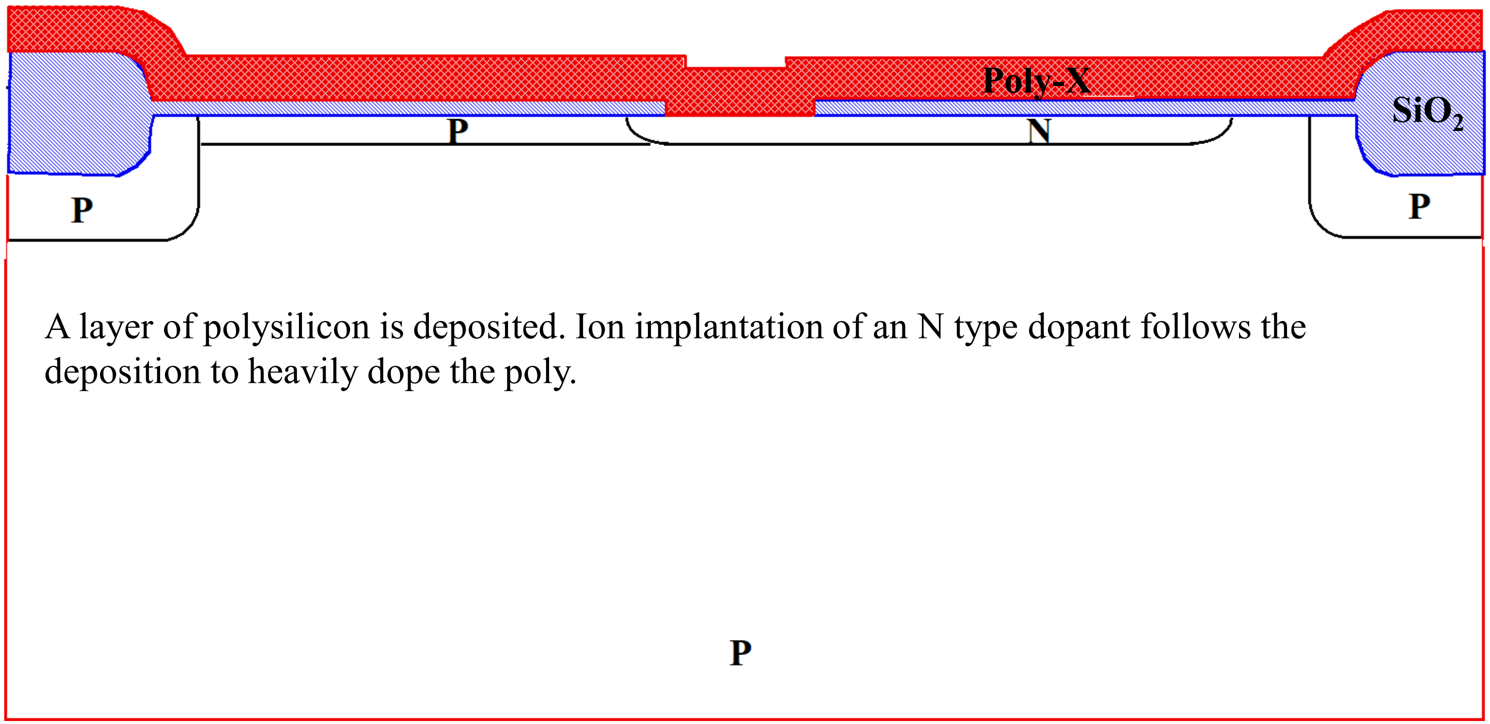
Materials Used: Amorphous dielectrics, gases



Mask #4 is used to provide the buried contact. The gate oxide is etched where the poly needs to contact the silicon.

Disciplines Used: ECE (electrical design of source), Chemistry (choice of dopants), MSE (solid solutions of dopants), Physics (optics/diffraction)

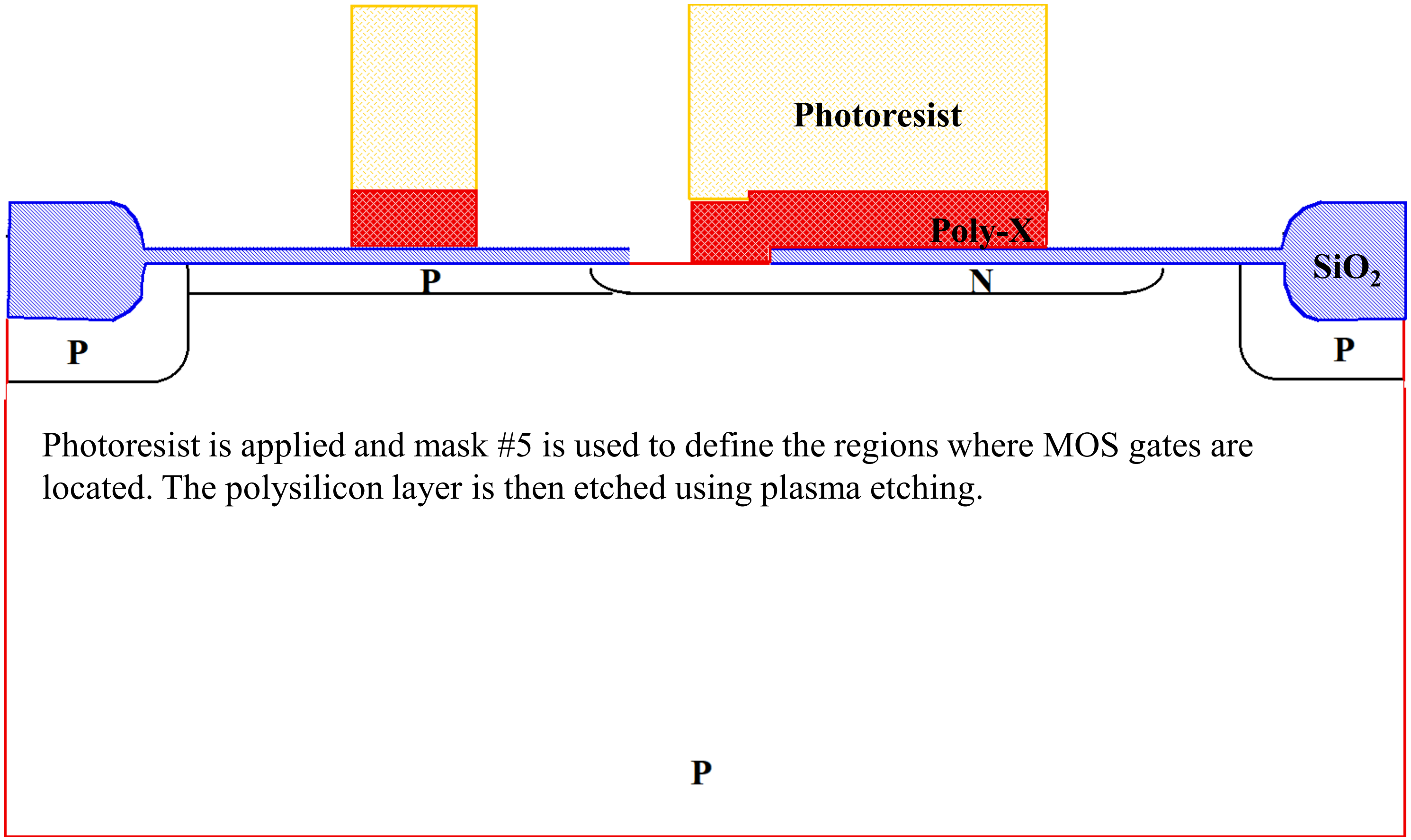
Materials Used: Crystalline Semiconductors, amorphous dielectrics, polymers, and ions



A layer of polysilicon is deposited. Ion implantation of an N type dopant follows the deposition to heavily dope the poly.

Disciplines Used: ECE (electrical design of source, reliability), Chemistry (CVD & choice of dopant for poly), MSE (alloy reactions)

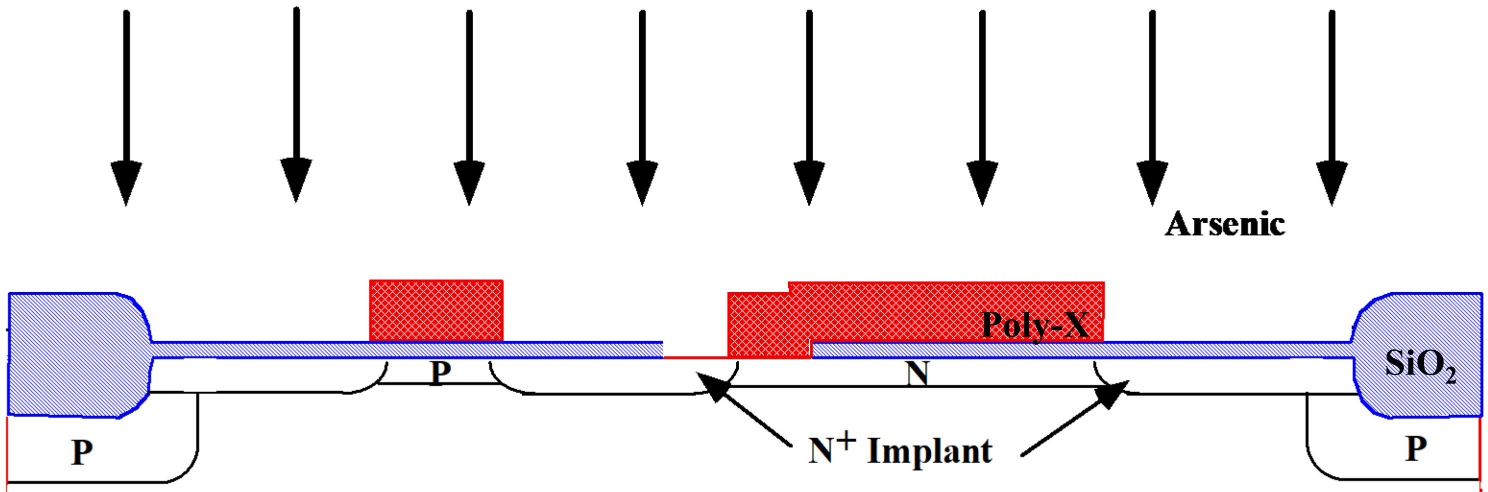
Materials Used: Crystalline and poly-crystalline Semiconductors, amorphous dielectrics, gases



Photoresist is applied and mask #5 is used to define the regions where MOS gates are located. The polysilicon layer is then etched using plasma etching.

Disciplines Used: …similar to previous…

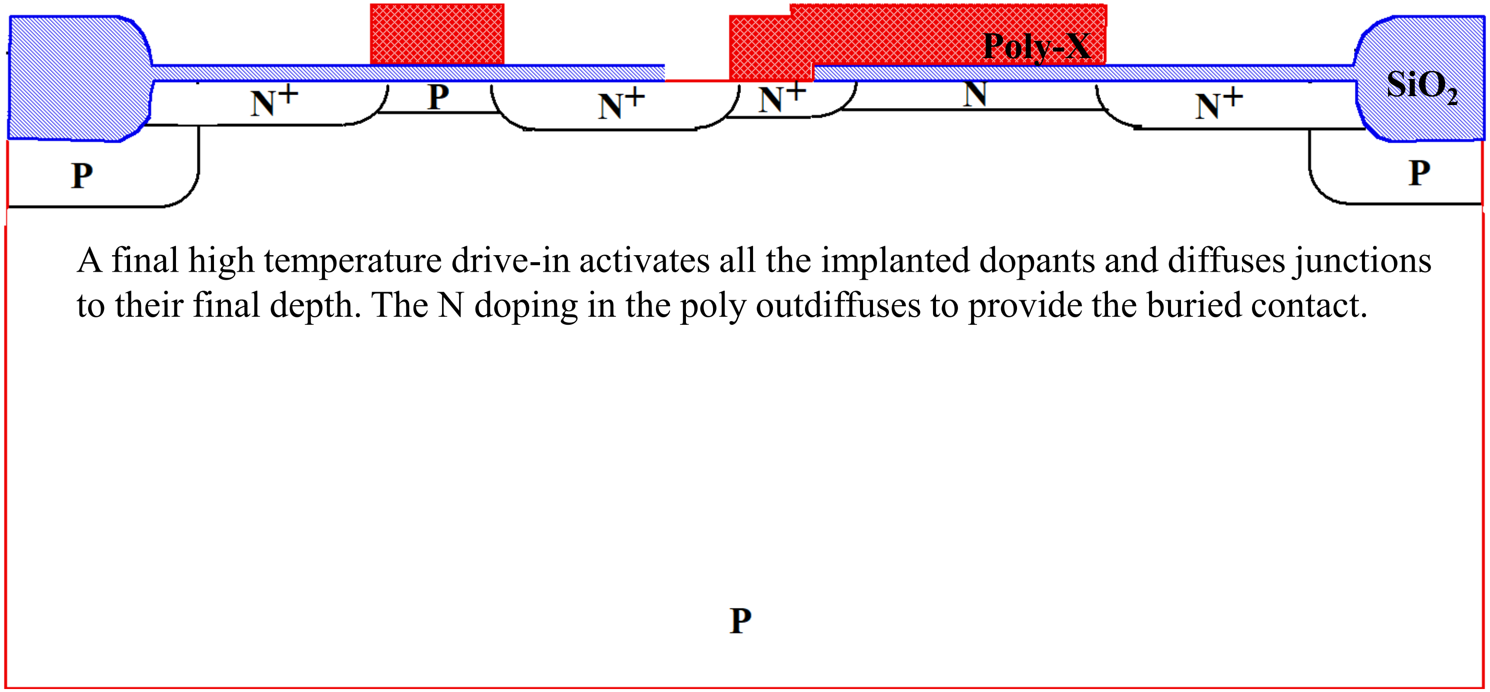
Materials Used: …similar to previous…



Arsenic is implanted to form the source and drain regions. Note that this can be unmasked because there are only NMOS transistors on the chip.

Disciplines Used: …similar to previous…

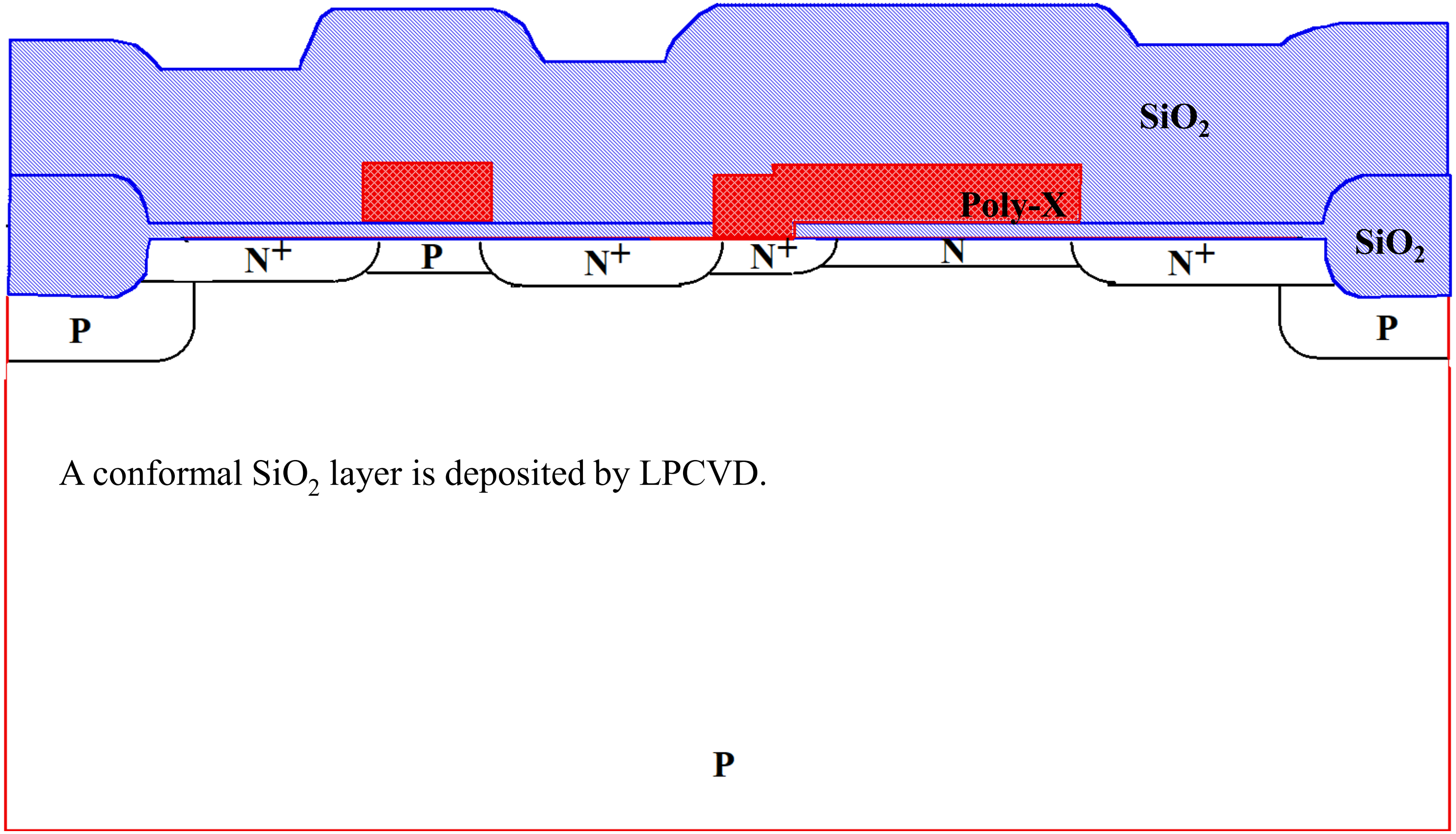
Materials Used: …similar to previous…



A final high temperature drive-in activates all the implanted dopants and diffuses junctions to their final depth. The N doping in the poly outdiffuses to provide the buried contact.

Disciplines Used: …similar to previous…

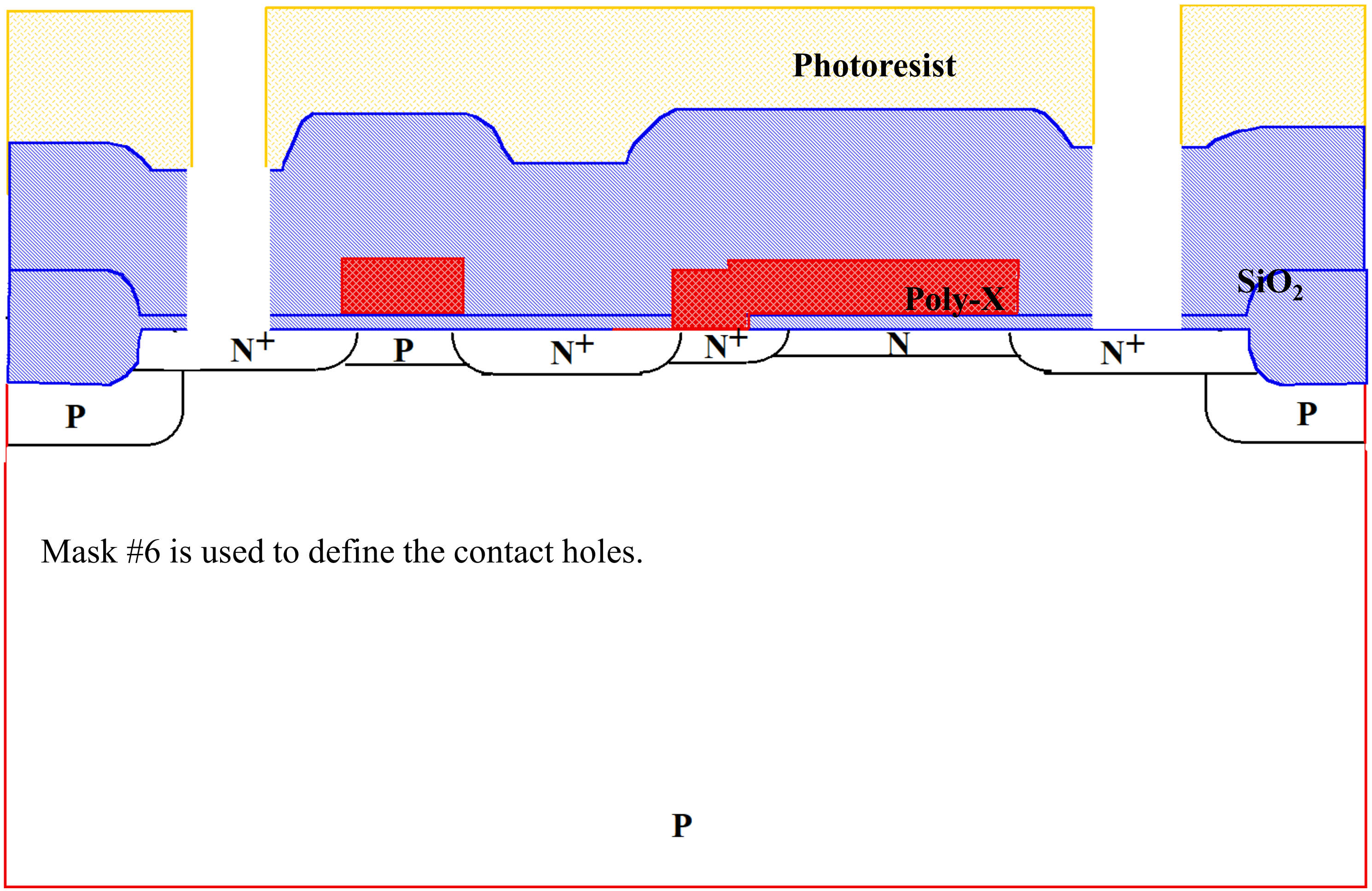
Materials Used: …similar to previous…



A conformal SiO_2 layer is deposited by LPCVD.

Disciplines Used: …similar to previous…

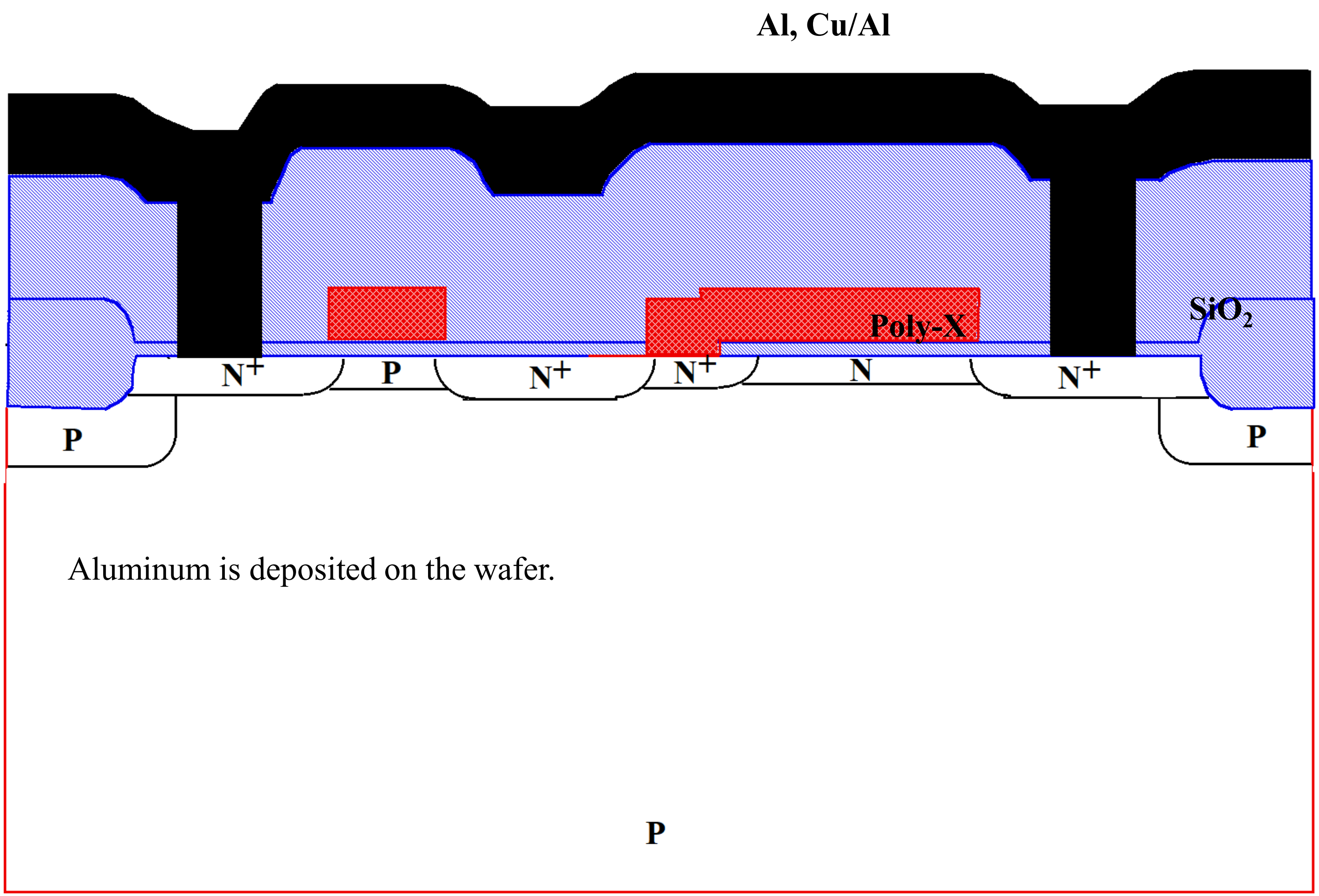
Materials Used: …similar to previous…



Mask #6 is used to define the contact holes.

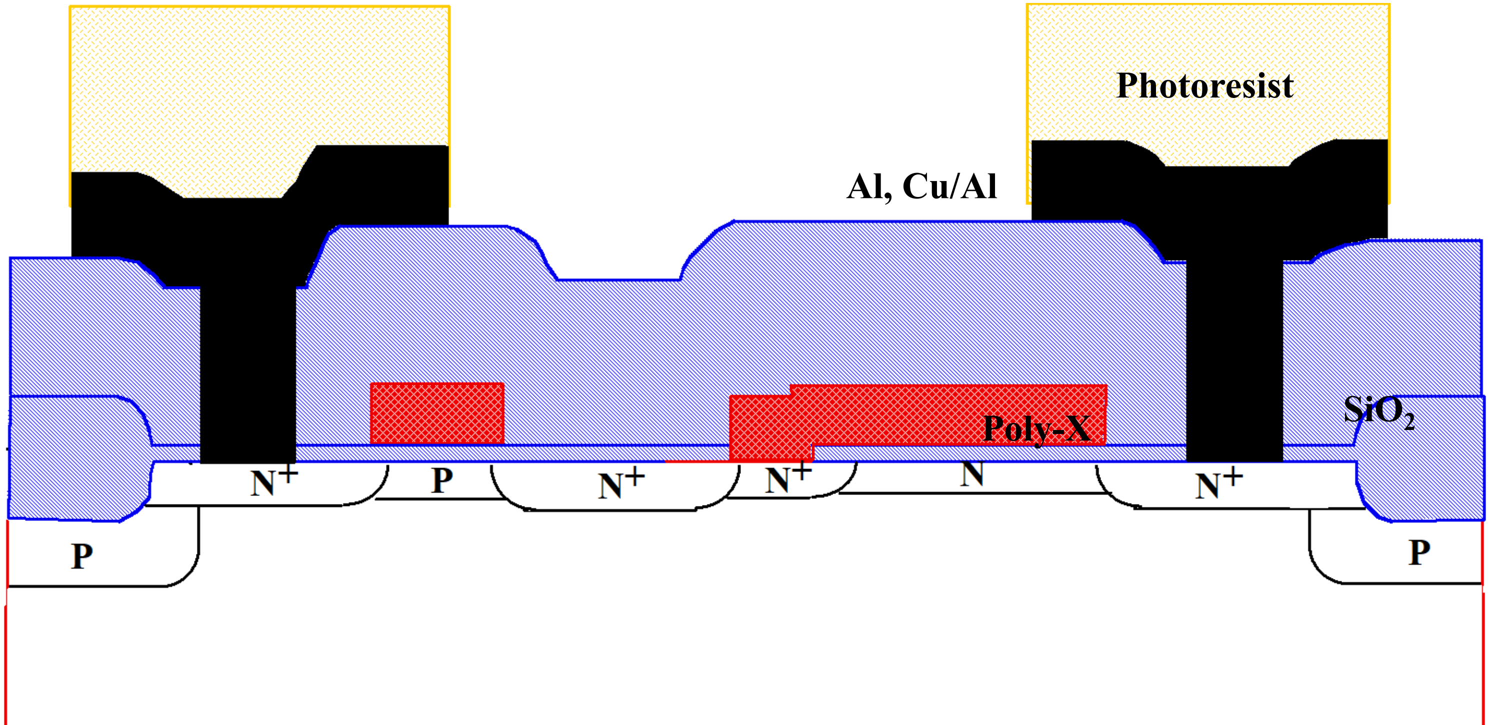
Disciplines Used: …similar to previous…

Materials Used: …similar to previous…



Disciplines Used: …similar to previous…

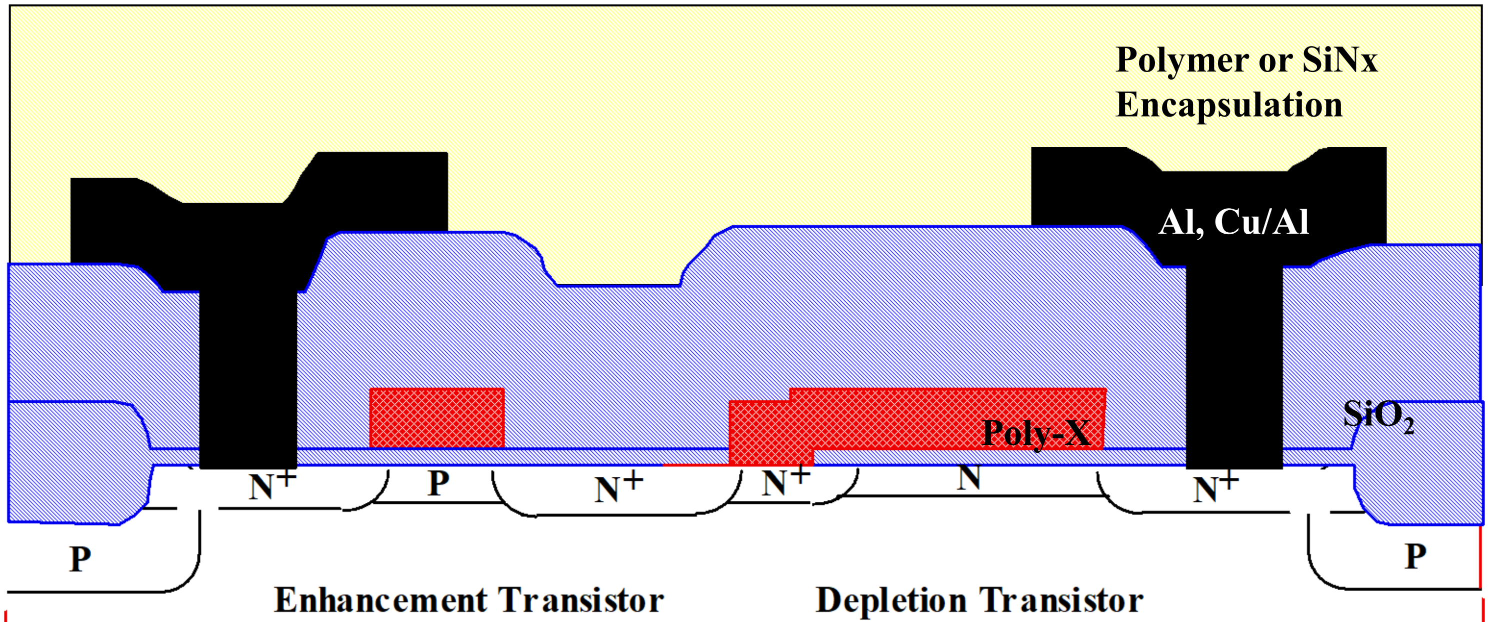
Materials Used: …similar to previous…



Mask #7 is used to pattern the aluminum. After stripping the resist, the structure is finished to the point shown in the cross-section we started with. In actual practice an additional deposition of a final passivation layer and an additional mask (#8) would be needed to open up the regions over the bonding pads.

Disciplines Used: …similar to previous…

Materials Used: …similar to previous…



Final environmental barrier deposited for encapsulating the device. Openings would be provided only at bond pads.

Disciplines Used: …similar to previous…

Materials Used: …similar to previous…

Classifications of the many processes used in Microelectronics Technology…now lets study each step

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