Lecture 4

Oxidation (applies to Si and SiC only)

Reading:

Chapter 4

Oxidation: Si (and SiC) Only

Introduction discussion:

The ability to grow a high-quality thermal oxide has propelled Si into the forefront of all semiconductor technology.

Ge allows faster transistors (due to its much higher mobility) , dissipates much less heat and was used first, before Silicon. However, Ge-oxides are much more unstable, much poorer quality and very difficult to form.

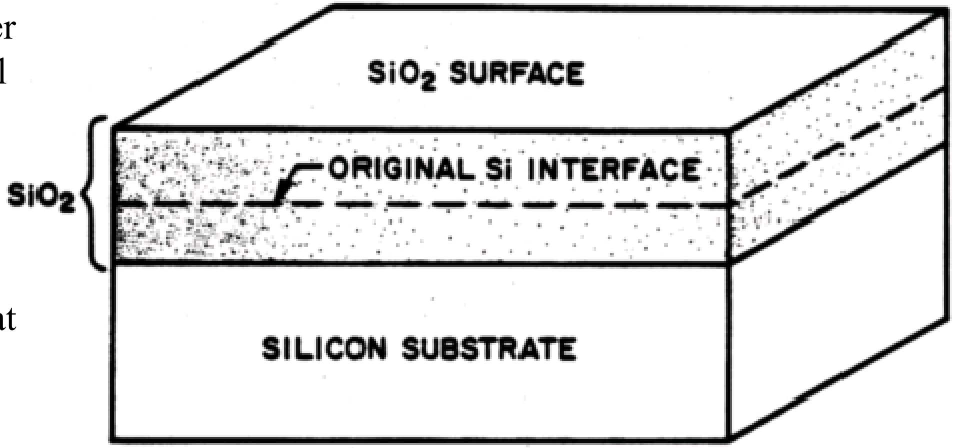
Some present-day efforts are being made to produce SiGe channel transistors to marry the benefits of Si (good oxides) with the speed of Ge.

High power devices are being developed in SiC. One key advantage of SiC over other material alternatives is the ability to grow high quality oxides on the Si face of SiC. (Note: SiO_2 is a low vapor pressure solid while CO_2 is a high vapor pressure gas).

During the oxidation of Si or Si-faced SiC, the Oxidizing Species defuses through the oxide to react with the Si at the Si/SiO_2 interface. In theory, some Si can diffuse back out of the oxide, but in practice, this does not occur (due to $Si_{Iinterstitial}$ injection into the bulk).

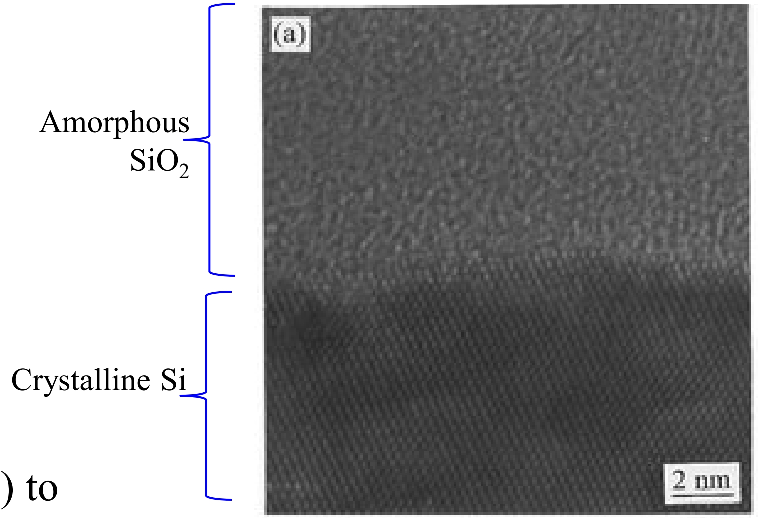
The $Si\text{-}SiO_2$ and $SiC\text{-}SiO_2$ interfaces are order disorder interfaces (crystalline to amorphous). As such most all oxidations are followed by a hydrogen anneal (oftn as forming gas) to tie up dangling bonds (broken chemical bonds).

SiC oxides often have a Nitrous oxide anneal prior to hydrogen anneals to remove the carbon accumulated at the interface.



Oxidation:

Chemistry



Park et al, Journal of Vacuum Science & Technology B, Microelectronics and Nanometer Structures Processing Measurement and Phenomena 14(4):2660 – 2666, August 1996
DOI: 10.1116/1.589001

For dry oxidations: $Si + O_2 = SiO_2$

While for wet oxidations: $Si + 2H_2 0 = SiO_2 + 2H_2$

- Typically, some hydrogen is introduced (even in a dry oxidation) to allow the monovalent hydrogen to passivate (chemically satisfy) broken interface bonds at the Si/SiO_2 interface.
- The stability of this passivation is an issue of increasing concern as E-fields increase due to decreasing device dimensions. Electrons tend to be accelerated into the Hydrogen, breaking the H-Si Bond. These same broken bonds can then trap electrons, preventing or slowing their conduction.
- Since the Si/SiO_2 interface never sees the ambient, it is extremely pure (impurities must be adsorbed onto the SiO_2 and diffuse to the interface to contaminate it).
- The oxidizing reaction occurs at the Si/SiO_2 interface which is continuously moving. Thus, Si material is consumed during Oxidation. From the densities and molecular weights of Si and SiO_2, we find that the thickness of the Si consumed is 0.44d, where d is the oxide thickness.
- Likewise, since the oxygen must diffuse through the oxide to react at the Si/SiO_2 interface, the oxidation rate depends on the thickness of the oxide and reduces as the oxidation progresses.

Oxidation:

Chemistry

3 flow regimes occurring during oxidation:

1.) Stagnant Gas Flow: occurs due to finite gas flow in the bulk gas, and zero flow at the wafer surface. The "boundary layer" between the wafer and the free flowing gas acts as a diffusion barrier for incoming gas molecules.

2.) Diffusion through the oxide: Molecular diffusion of O_2 or H_2O.

3.) Reaction limited flux at the Si/SiO_2 interface.

C_G=Concentration in Gas

C_S=Concentration in Gas side of the stagnant layer/oxide boundary

C_O= Concentration in the oxide at the stagnant layer/oxide boundary

C_i= Concentration in the oxide at the oxide/Si boundary

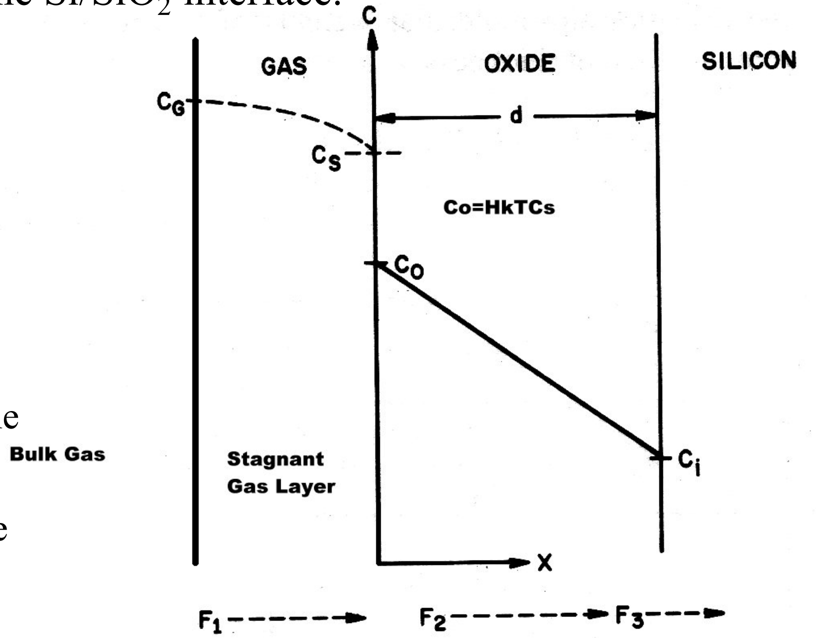


FIGURE 2
Basic model for thermal oxidation of silicon (*After Deal and Grove, Ref. 4.*)

Oxidation:

Chemistry

Given that the concentration of the oxygen at the Si/SiO$_2$ interface is,

$$C_i = \frac{HP_G}{\left(1 + \frac{k_s HkT}{h_G} + \frac{k_s t_{oxide}}{D}\right)}$$

and the concentration of the oxygen in the oxide at the stagnant gas/oxide boundary is,

$$C_0 = \frac{HP_G\left(1 + \frac{k_s t_{oxide}}{D}\right)}{\left(1 + \frac{k_s HkT}{h_G} + \frac{k_s t_{oxide}}{D}\right)}$$

If D--->0 (diffusion controlled) C_i--->0, C_O--->HP_G.

If D--->infinity (reaction controlled) $C_i=C_O=HP_G / (1 + k_S HkT/h_G)$

The rate of oxidation can be expressed as,

$$(*)\quad \text{Oxidation Rate} = \frac{dt_{oxide}}{dt} = \frac{Hk_s P_G}{N_1\left[1 + \frac{k_s HkT}{h_G} + \frac{k_s t_{oxide}}{D}\right]}$$

where H is Henry's gas constant, k_S is the chemical rate constant for the reaction at the Si/SiO$_2$ interface, k is Boltzman's constant, P_G is the partial pressure of the oxidizing species, T is absolute temperature, D is the diffusion coefficient for the oxidant, h_G is the mass transport coefficient in the stagnant layer, t_{oxide} is the oxide thickness, and N_1 is the number of molecules of oxidizing species per unit volume of SiO$_2$.

Oxidation:

Chemistry

What is N_1: Since SiO_2 has a molecular density of $2.2\text{x}10^{22}$ molecules/cm^3 and

$$Si + O_2 = SiO_2$$

$N_1 = 2.2\text{x}10^{22}$ molecules/cm^3 for dry oxidations.

While for wet oxidations,

$$Si + 2H_2O = SiO_2 + 2H_2$$

$N_1 = 4.4\text{x}10^{22}$ molecules/cm^3 for wet oxidations

N_1 is the number of molecules of oxidizing species per unit volume of SiO_2.

Oxidation:

Thickness -Time Relationship

The general solution of this equation (*), under the assumptions of at t=0, $t_{oxide} = t_o$,

$$(t_{oxide})^2 + At_{oxide} = B(t+\tau) \qquad A = 2D\left(\frac{1}{k_s} + \frac{1}{h_G}\right) \qquad B = \frac{2DHP_G}{N_1}$$

$$\tau = \frac{t_o^2 + At_o}{B},$$ Time shift due to initial oxide thickness, t_o

A and B or B/A are usually quoted, not the fundamental constants (D, k_s etc...).

A more useful form of this equation is,

$$t_{oxide}(t) = \frac{1}{2}A\left[-1 + \sqrt{1 + 4\left(\frac{B(t+\tau)}{A^2}\right)}\right]$$

Oxidation:

Thickness -Time Relationship

Consider two limiting cases,

Case I.) Thin oxides, ===> Neglect quadratic term,

$$t_{oxide} \approx \frac{B}{A}(t+\tau)$$

in which case B/A is termed the linear rate coefficient.

Case II: Thick oxides ===> Neglect the linear term,

$$t^2_{oxide} \approx B(t+\tau)$$

in which case B is called the parabolic rate coefficient.

Advantages/Disadvantages of Wet verses Dry Oxidations

	Advantages	Disadvantages
Dry (O_2)	Better Electrical Breakdown, Dense, Used for Gates	Slow Growth Rate
Wet (O_2+H_2O)	Fast Growth Rate, good for device isolation, contact isolation, etc...	Somewhat Porous (sponge analogy). Not used for gate oxides. Often replaced by CVD deposited oxides now

Practical considerations:

Metallic impurity gettering:

Halogen species (Cl, F, etc...) are often introduced to getter metallic impurities from the tube during an oxidation. This also tends to increase the oxidation rate for thin oxides (linear term). HCL is the safest to use (bubbled into the furnace as described in the diffusion discussion) but is highly corrosive to the gas tubing etc.... However, Trichloroethylene (TCE) and Trichloroethylane (TCA) are less corrosive but can be toxic (TCE is, while TCA can form phosgene at high temperatures).

Thick oxides:

Due to the growth rate dependence on thickness, thick oxides must be performed at high pressures. These furnaces look like submarine torpedo tubes and raise the partial pressure of oxygen that in turn raises the parabolic rate coefficient, B.

Thin Oxides:

Most thin (t_{oxide} <~ few hundred angstroms) dry oxides grow at a rate faster than Deal & Grove predicts. Corrections can be made to work down to ~ 300 angstroms, but modern MOS gate oxides are <100 angstroms.

Orientation Dependence:

Oxidation rate depends on orientation. MOS uses <100> oriented wafers because it has the fewest atoms per cm^2 ===> results in lower interface states.

Oxidation Induced Stacking Faults:

The oxidation process injects $Si_{interstitials}$ into the bulk silicon. These interstitials can add up to result in stacking faults or OSF (oxidation induced stacking faults). High temperature or high pressure oxidations can reduce OSF as can the use of HCl in the oxidizing ambient.

Dopant Effects:

Doping of the semiconductor tends to increase the oxidation rate. The dopants can redistribute due to segregation at the Si/SiO_2 interface.

Oxide Charges

Charges in oxides:

Real oxides have several types of charged defects each that effect devices in different ways:

1.) Mobile Ionic Charge: BAD!!!! Leads to fluctuations in turn on voltages with time.

2.) Oxide Trapped Charge: Defects in the SiO_2 can result from ionizing radiation (E-beam evaporation, high photon energy lithography, etc...), or high currents in the oxide. It generally can be annealed out at low temperatures.

3.) Interface Trapped Charge: Results from broken bonds at the Si/SiO_2 interface. Hydrogen anneal effectively reduces these defects to less than 10^{10} cm^{-2}.

4.) Fixed Oxide Charge: Usually positive charge is located within ~30 angstroms from the interface. It is thought to be related to excess Si in the oxide and can be greatly reduced by a post oxidation anneal in an inert gas such as nitrogen or argon and rapid cooling from high temperatures. Effects the device turn on voltages.

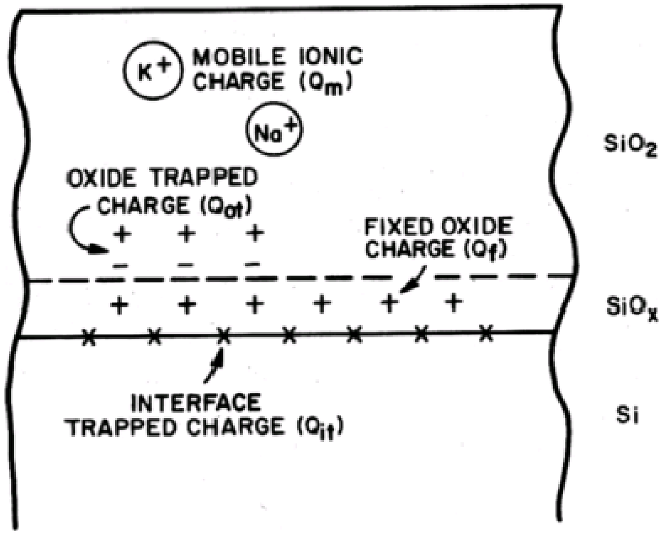
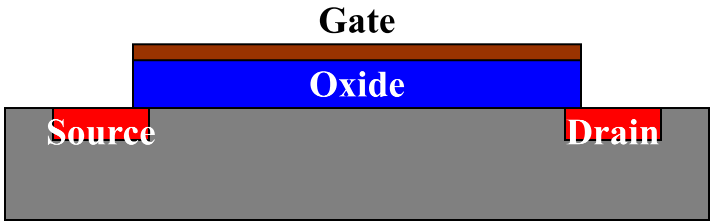


FIGURE 16
Charges in thermally oxidized silicon. (*After Deal, Ref. 48.*)

Alternative Gate Dielectrics

$$Q = CV$$

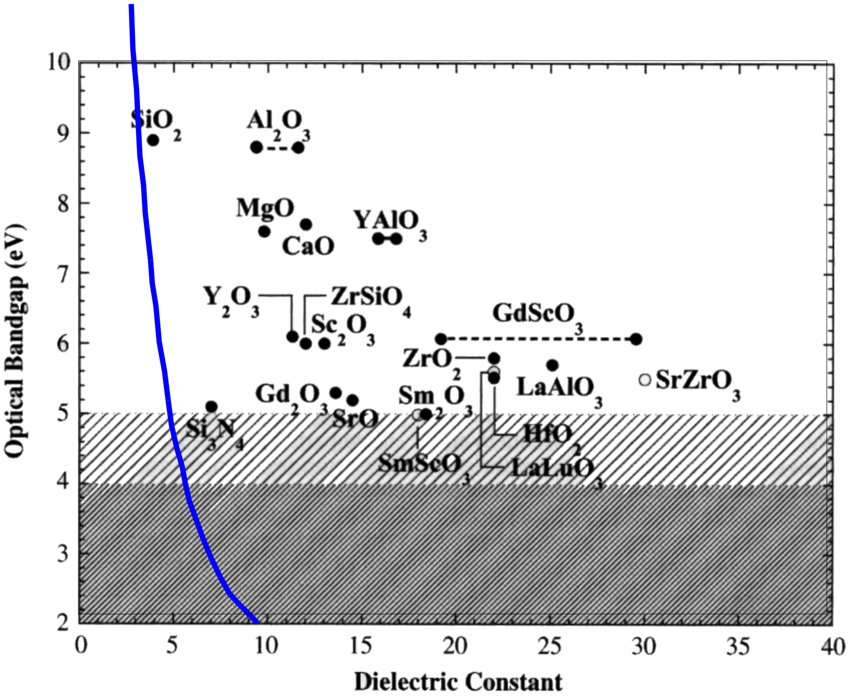
$$Q = \left(\frac{\varepsilon_o \overset{k_R}{\varepsilon_R} \left(Area \right)}{Dielectric\ Thickness} \right) V$$



- As device areas and drive voltages reduce, dielectric thicknesses must be reduced to insure enough charge exists in the channel to allow current flow (specifically enough to invert the semiconductor surface)
- Oxides less than ~1-2 nm are excessively leaky so as to *POSSIBLY* prevent practical use.
- Alternatively, another material with a higher relative dielectric constant can be used while making the dielectric thicker.

Alternative Gate Dielectrics

Trade offs in insulating properties verses dielectric constant



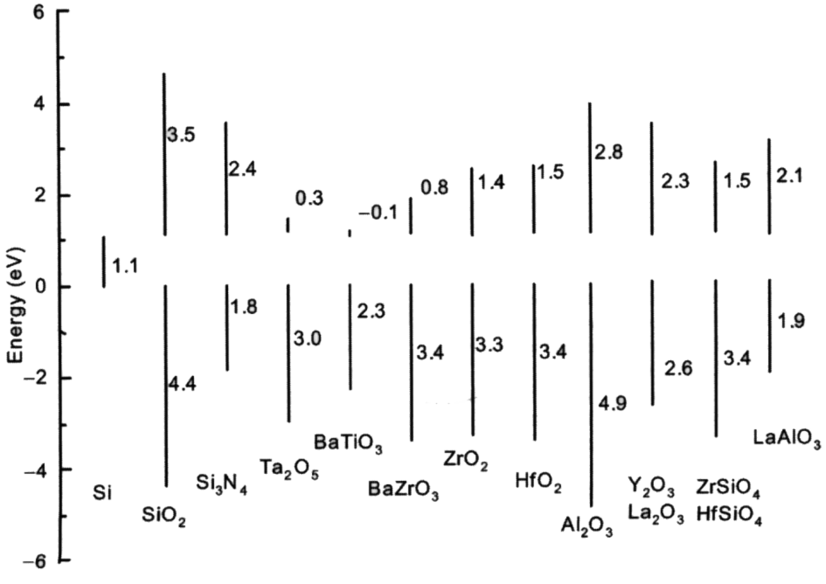


Figure 5. Calculated band offsets of oxides on Si.

The energy bandgap tends to reduce with increasing dielectric constant

Dielectric constant measures the ease for which charge within a material can be separated. Thus, since wide bandgap materials "hold their electrons tightly" they have lower dielectric constants and as we previously have shown higher bandgaps.

Not only is the energy bandgap important, but the offset in the valence and conduction bands is important since the insulator must block both electrons and holes.

Example: Ta_2O_5 is a poor insulator for electrons but is fine for holes

Note: Eq. (old text 4.24 – 4.26 new text), shown in blue above, is plainly incorrect!

Alternative Gate Dielectrics

Hafnium (Hf), Zirconium (Zr) and other exotic oxides.

(See in Class discussion.)

Oxynitrides: Important for older FLASH memory and thin oxides to prevent Boron Penetration. Newer FLASH tends to use floating gate structures that replace (partially) the role of oxynitrides.

Can be deposited by:

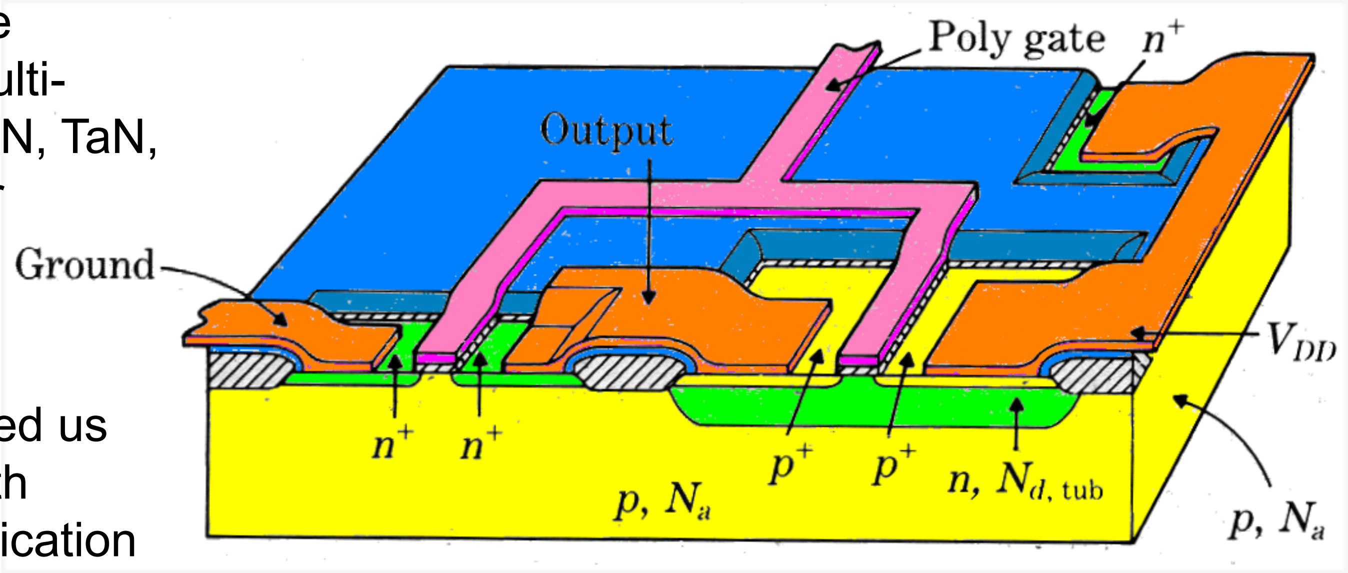
- Chemical Vapor Deposition (Later)
- Introduction of ammonia (NH_3) during oxidation (requires a re-oxidation to lower trap density)
- Introduction of Nitrous oxide (N_2O) or Nitric Oxide (NO) during oxidation

Why do we need to know about Nano-electronic "materials" details? – A Case study of the evolution of the Transistor

Semi-Modern MOSFET (late 1990's vintage): SiO_2 Gate Oxide, Polysilicon gate metals, metal source/drain contacts and Aluminum metal interconnects

Problem: As interconnect sizes shrank, Aluminum lines became too resistive leading to slow RC time constants

Solution: Replace Aluminum with multi-metal contacts (TiN, TaN, etc…) and copper interconnects.



This change carried us for ~ 1 decade with challenges in fabrication (lithography) being the primary barriers that were overcome …until…

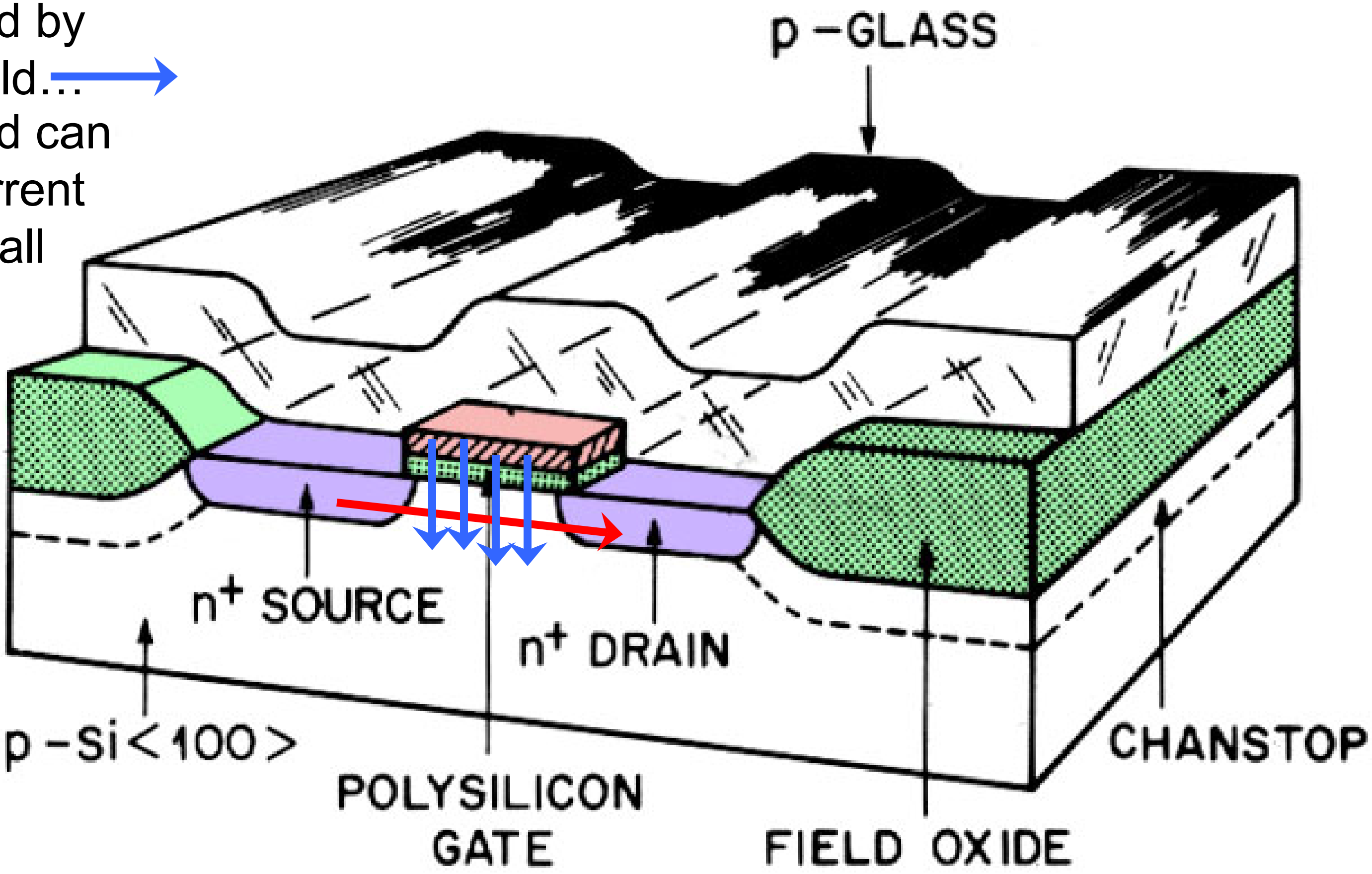
The Basic Device in CMOS Technology is the MOSFET

Direction of Desired Current flow… →

…is controlled by an electric field… →

…but this field can also drive current through a small gate.

Modern transistors have more power loss in the gate circuit than the source - drain! New approaches are needed.



Why do we need to know about Nano-electronic "materials" details? – A Case study of the evolution of the Transistor

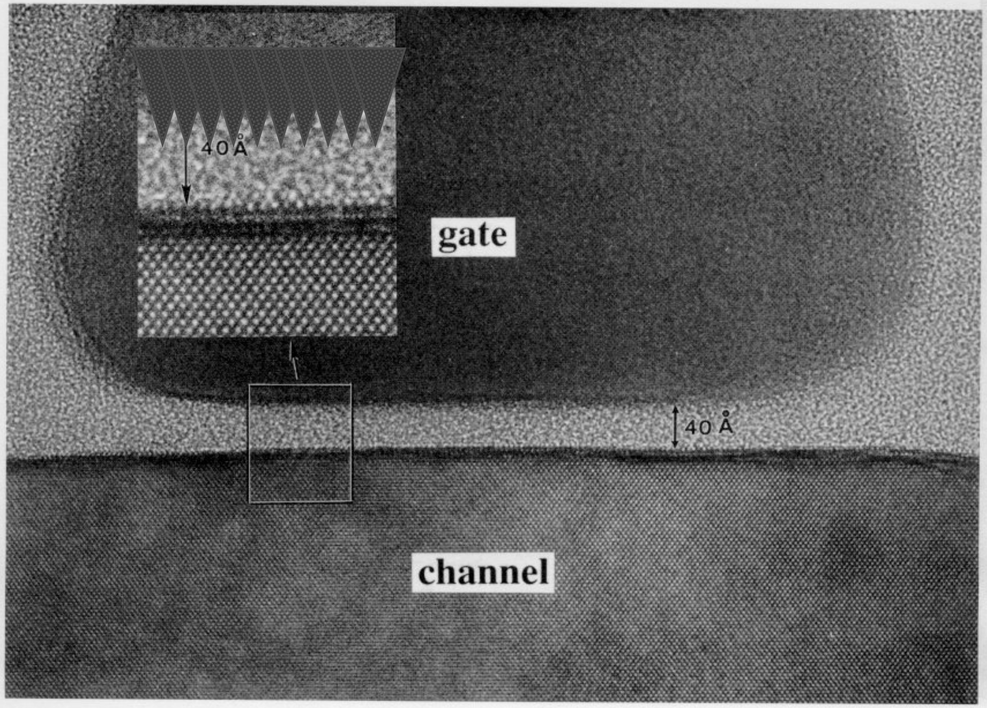
Early MOSFET: SiO_2 Gate Oxide, Aluminum (Al) Source/Drain/Gate metals

Problem: As sizes shrank, devices became unreliable due to metallic spiking through the gate oxide.

Solution: Replace Metal Gate with a heavily doped poly-silicon.

This change carried us for decades with challenges in fabrication (lithography) being the primary barriers that were overcome …until…

Cross section of a MOSFET. This high resolution transmission electron micrograph of a silicon Metal-Oxide-Semiconductor Field Effect Transistor shows the silicon channel and metal gate separated by a thin (40Å, 4nm) silicon-dioxide insulator. The inset shows a magnified view of the three regions, in which individual rows of atoms in the crystalline silicon can be distinguished. (Photograph courtesy of AT&T Bell Laboratories.)



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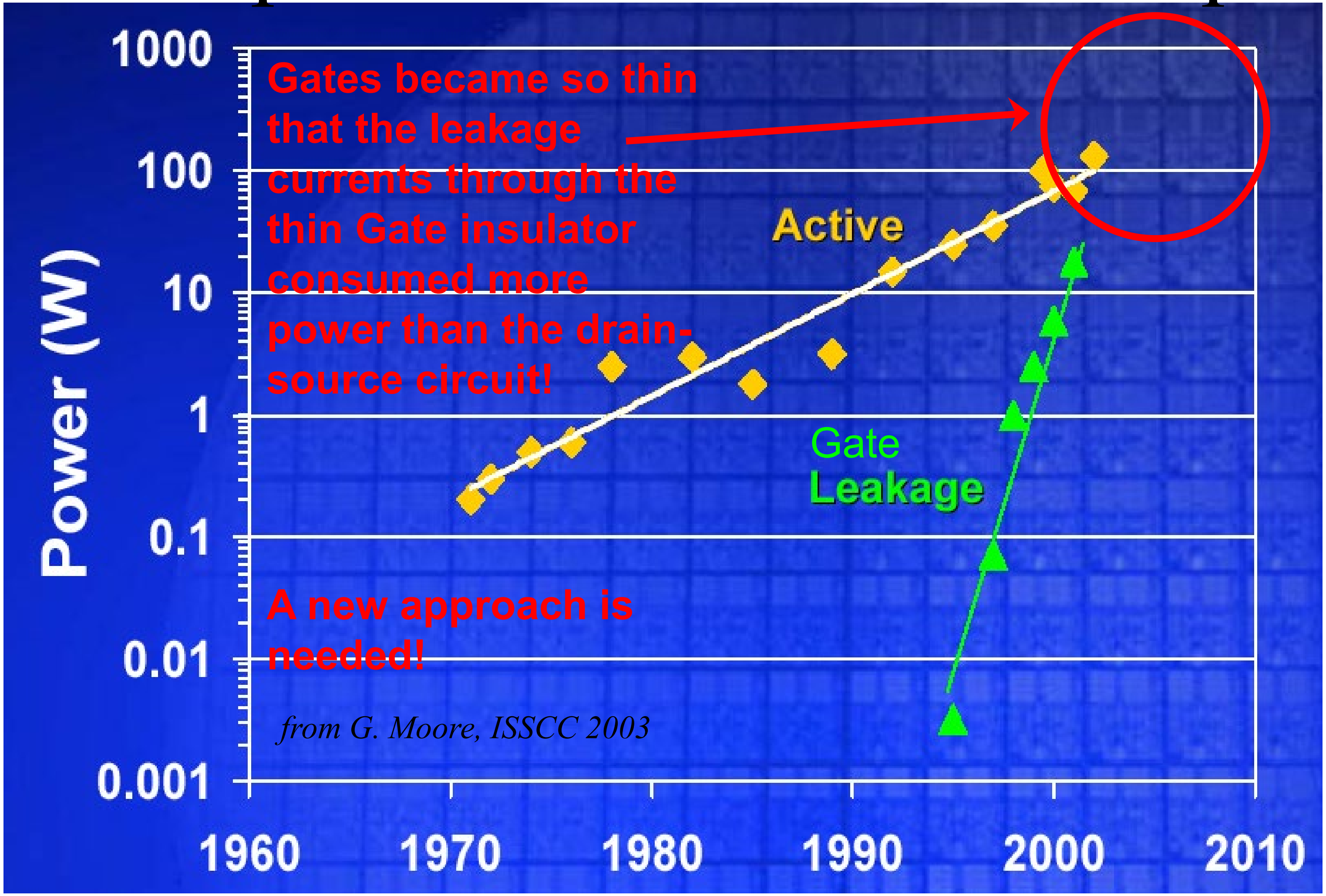
Microprocessor Power Consumption

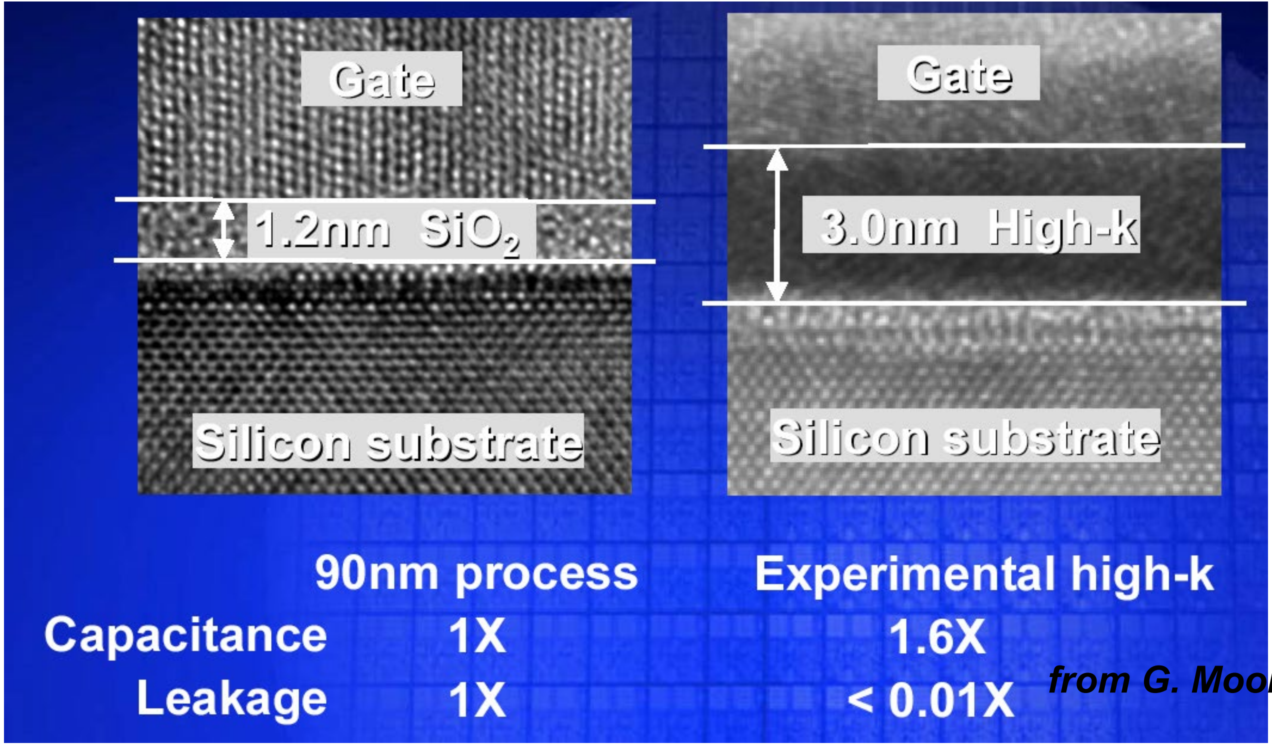


Gates became so thin that the leakage currents through the thin Gate insulator consumed more power than the drain-source circuit!

A new approach is needed!

from G. Moore, ISSCC 2003

Why do we need to know about Nano-electronic “materials” details? – A Case study of the evolution of the Transistor



	90nm process	Experimental high-k
Capacitance	1X	1.6X
Leakage	1X	< 0.01X

from G. Moore, ISSCC 2003

$$D_{insulator} = k_{insulator} E$$

$$D_{insulator} = k_{insulator} \left(\frac{V_{Gate}}{t_{Gate}} \right)$$

$$I_{Gate\ Leakage} \propto e^{t_{Gate}}$$

Gate leakage current can be dramatically lowered by increasing Gate insulator thickness but to do so without changing the channel conductivity, you have to increase the dielectric constant of the insulator. NEW GATE INSULATORS FOR THE FIRST TIME IN 60 YEARS!!!!

2008 Vintage Intel Microprocessor and Beyond Uses $HfSiO_2$ but this is Losing Steam