Copper Integration

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Outline

- Copper-based transition
- Copper integration processes
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  - ➔ Technological changes
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Cu transition

Advantages of **Cu** vs. **Al**

- better conductance (lower resistance)
  - ➔ smaller interconnects
    - ➔ fewer metal layers
      - ➔ lower production costs
  - ➔ faster speeds
- better resistance to Electromigration
  - ➔ improved reliability
- better yield

Conclusion: Many high performance semiconductor companies have made the transition to copper-based circuits to take advantage of these benefits.

Cu integration processes

Successful copper integration involves a broad range of processes and technologies to work in succession properly:

1. Dielectric etch
2. Cleaning
3. Barrier/seed deposition
4. Electroplating
5. CMP
6. Metrology

As feature sizes continue to shrink, several changes are necessary to successfully metalize such structures, which in turn can have negative effect on subsequent processing.

Cu defects

Defects have a profound effect on the performance and reliability of semiconductor circuits. In copper interconnects, defects can appear as scratches, surface roughness, corrosion stains, pits, voids, or protrusions. These defects have a variety of root causes that may originate in the current processing step or may evolve from a previous processing flaw.

Typical Copper Defects and Causes		
	Defect	Root Cause
Seed layer	Bottom voids	Marginal coverage
	Bottom voids/pinholes	Corrosion
	Center seam voids	Thickness variations
Via	Voids	Sidewall shape
	Poor step coverage/notching	Over-/under-etch

Etch challenges

Since copper is difficult to etch, an alternative patterning method is used known as dual damascene, where trenches and holes are cut into a dielectric and then filled with copper.

The most popular dual damascene process used in industry is the via-first approach.

Basic steps: (there are several more steps involved, not shown)

- ➔ Deposition of a thick dielectric
- ➔ Etch via pattern in dielectric
- ➔ Photoresist processing for trench pattern
- ➔ Photoresist removal

Note: More advanced processing eliminates the use of a trench stop etch to reduce cost and improve performance.

Etch defects

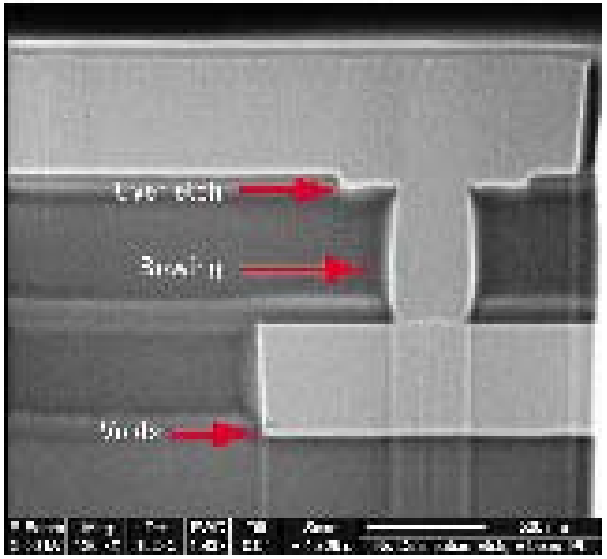
One of the biggest challenges due to not having a stopping layer in the via-first etch process is to prevent the formation of a fence or veil around the via inside the trench.

- Creates microvoids
- Increases resistance
- Compromises reliability

To get around this, manufacturers use a via plug to protect the via during the trench etch.

- Residue
- Bowing or sidewall damage

During plug removal, the strip process must remove the plug and resist, minimize, residue, and prevent any damage to the via.



Diffusion barrier challenges

Following the trench and via etching, a diffusion barrier is deposited, usually by PVD. The barrier must not only block copper diffusion, but also have good adhesion to the dielectric to prevent delamination during subsequent processing or thermal stressing.

- Electromigraiton
- Stress migration

(TaN adheres well to SiO_2 and Ta to copper)

Furthermore, the barrier must have good step coverage to reduce cusping and void production. It must be smooth, defect free, relatively thin, and have a low resistance, otherwise it may harm the integrity of the seed layer.

Other deposition technologies are of interest such as ALD, atomic layer deposition, which offers enhanced step coverage and good uniformity, and works at low temp. However, it is slow and may only be cost-effective for very thin layers.

Seed layer challenges

Like the diffusion barrier, the seed is deposited using PVD. The seed is very susceptible to contamination. A residue may remain from previous processing that doesn't allow the seed to plate properly. Areas where this occurs are certain to create microvoids during the electroplating process. Most problems in the this area of processing and with interconnect reliability start with an improper via clean.

- ➔ Voids

It is possible to do a seed repair, using an electroless deposition process, although this is considered a "band-aid" tactic to solving the problem, and not a cure for the initial problem of putting the seed down properly.

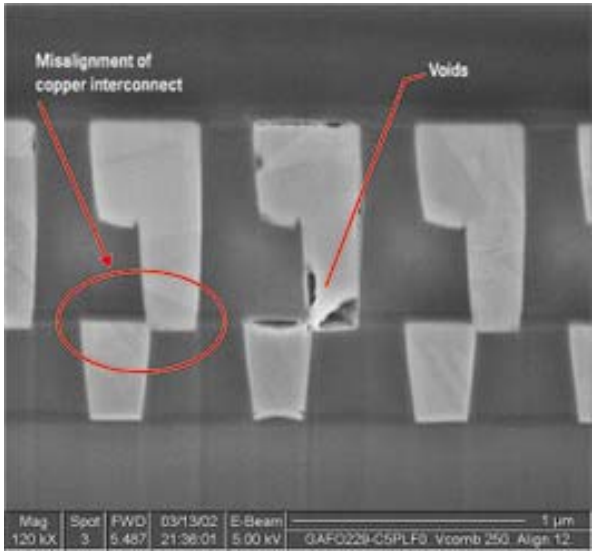
ALD is being researched for seed deposition, however electroless plating is one of the front runners to one day eliminate the seed layer completely.

Diffusion-Seed defects

Very thin diffusion barriers and poor step coverage at the bottom of vias are a major concern when looking at pore size, because large pore size can produce yield problems and via poisoning.

Voids may appear when the seed layer does not completely cover the bottom contact of an undersized via.

It is important to detect microvoids and voids that are not fully open or resistive vias that eventually open under stress or in the field causing reliability problems.

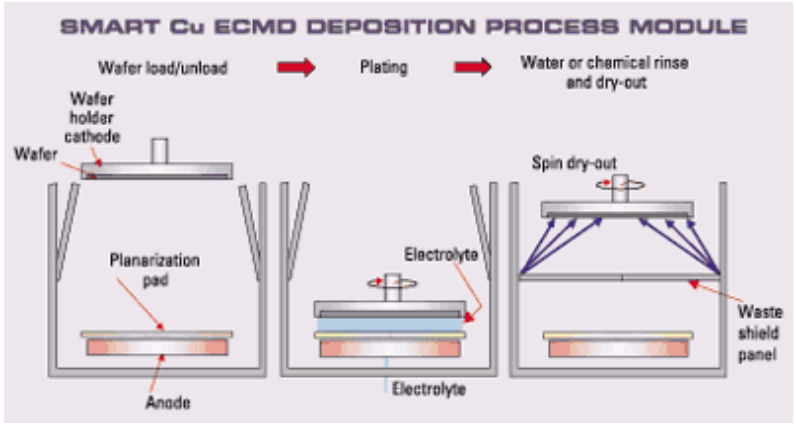


Electrofill challenges

The key to good copper electroplating is to get good uniformity and planarization across the wafer. Uniformity depends largely on how easy it is to get adequate current to the middle of the wafer. Technologies today are using larger wafers and thinner seeds causing difficulties with current distribution.

One solution is to reduce the pH of the bath keeping the electrons closer to the copper seed.

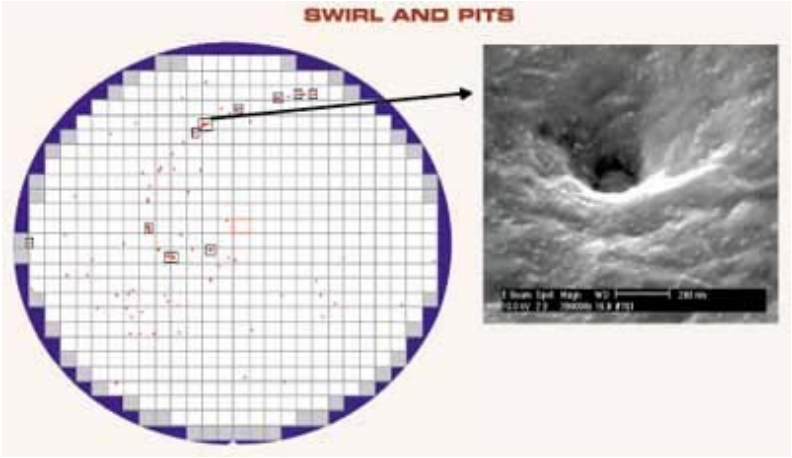
To achieve planarization, one technology is contact plating, where a rotating wafer is placed in contact with a pad and the electroplating solution is introduced through the pad.



Electrofill defects

One unique electrofill defect is a “swirl” mark-a series of pit defects that follow the wafer pattern of rotation during plating. Normally, the defect is associated with incomplete wetting of the seed surface, resulting in dry spots or bubbles on the wafer. As plating continues around the spot a circular defect is formed, hence the name swirl.

Many factors can be attributed to such defect such as time between seed deposition and plating, equipment ie. quality, cleanliness, etc. as well as chemistry.



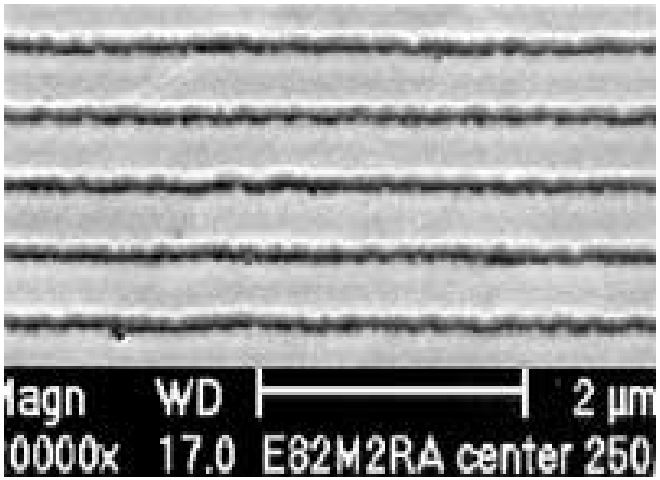
CMP challenges & defects

A number of defects may be credited to the CMP process mainly scratches and missing metal, though being close to the end of the process line enhances ones originated in earlier processing.

- Open and shorts in metal lines
- Galvanic corrosion

Missing metal may occur on the edge of an interconnect resulting in a defect known as a “mousebite.”

Careful filtration of the slurry, regular maintenance of cleaning equipment, and a post-plating anneal method can significantly reduce scratches on the wafer.

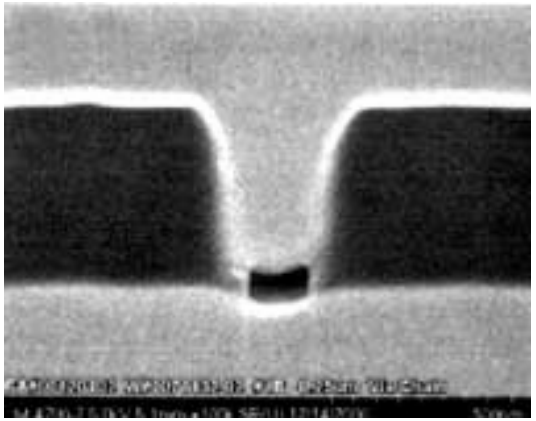


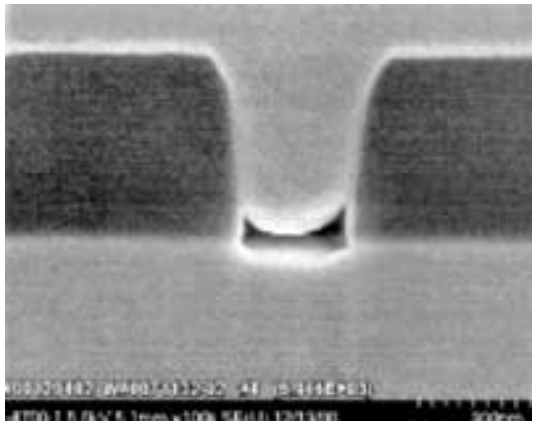
Post-plating anneal

It is thought that a post-plating anneal procedure will reduce not only the mousebite effect but also the overall number of defects.

Pullout voids in vias are a consequence of insufficiently annealed damascene features, where stress occurs during later thermal cycling.

For damascene imperfections to anneal, either high temp or a long anneal time is needed. Since high temps are unfavorable with copper in damascene features, the result must be a low temp. and a long anneal time to limit voiding.





Summary

Manufacturing challenges occur in almost every aspect of copper interconnect integration because of its relatively new adoption by semiconductor companies, and their reluctance to share information on developments in this area.

As design rules and feature sizes continue to change, the biggest challenges for copper lies in integration.

New materials initiate several problems for manufacturers, because defects can occur in any integration process, but may not become noticeable until later on. A fix in one step may cause more trouble in another.

Therefore, detecting defects is primary, not necessarily controlling them.