Stencil mask Ion Implantation for high performance MOSFETS

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MOTIVATION

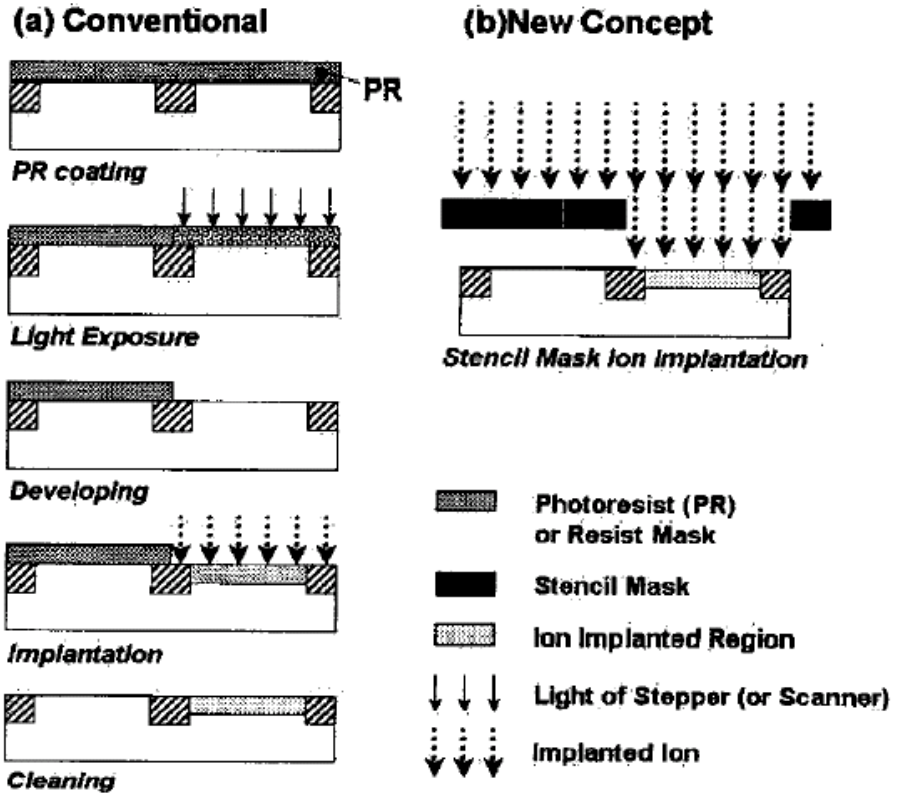
- In the last decade the demand for production of MOS transistors having channels of opposite conductivity type or different threshold voltages in the same substrate has increased greatly

- Conventional methods involve a sequence of processes (resist coating, exposure to light , resist development, ion implantation, removal) which is time consuming.

- Hence the new proposed method Stencil mask ion implantation technology (SMIT) for better performance, shorter process times and lower manufacturing costs.

Variation from conventional system

- The SMIT can revolutionize the ion implantation process by eliminating the need of the photo resist lithography process
- The ion implantation process by itself has not changed but SMIT is based on developing ion implanter with high throughput.
- The stencil mask acts as the resist mask

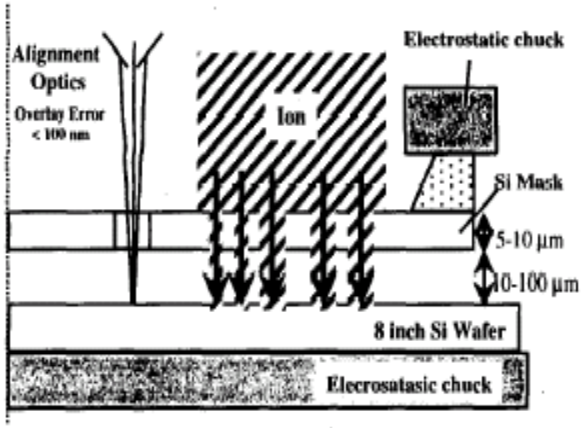


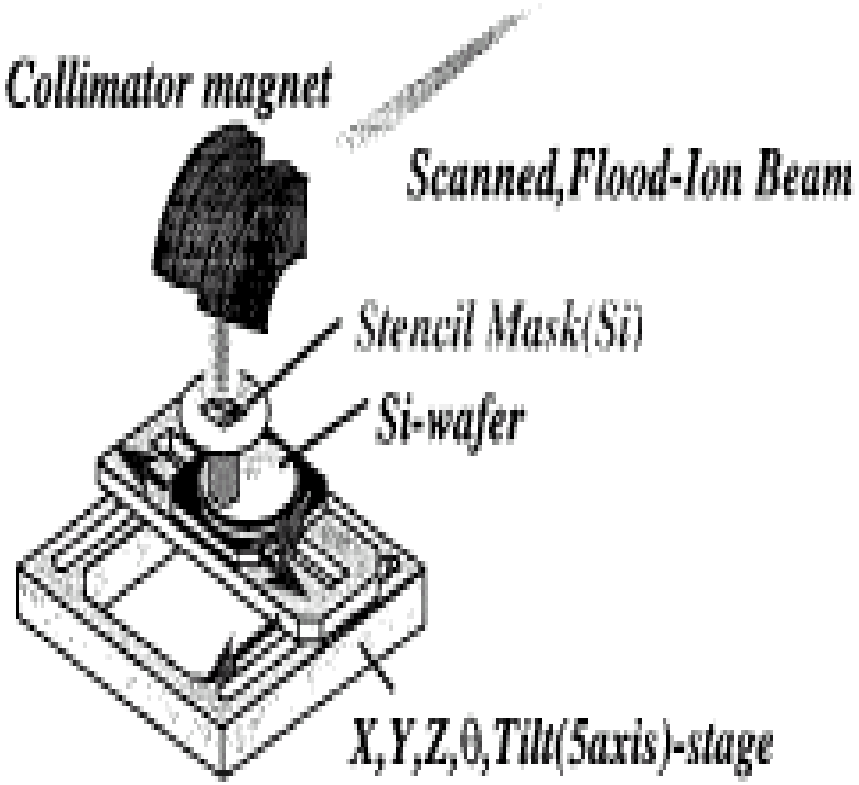
Stencil Mask Ion Implantation

Description of System

Outline of SMIT Scheme

1) Parallelism of the Ion beam is checked
2) Stencil mask is set in position using the alignment marks
3) The wafer moves to Ion Implantation position and the wafer is aligned to stencil mask
4) Ion beam is implanted into the wafer
5) Steps 3 and 4 are repeated for all chips on the wafer



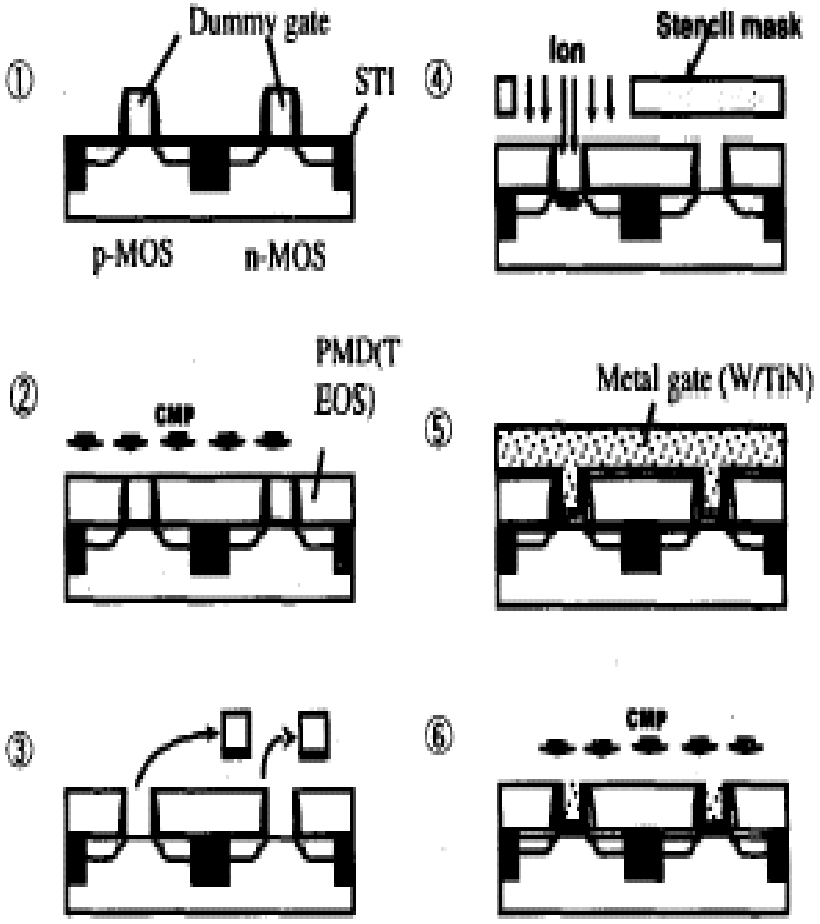


Stencil Mask Ion Implantation

Application of SMIT

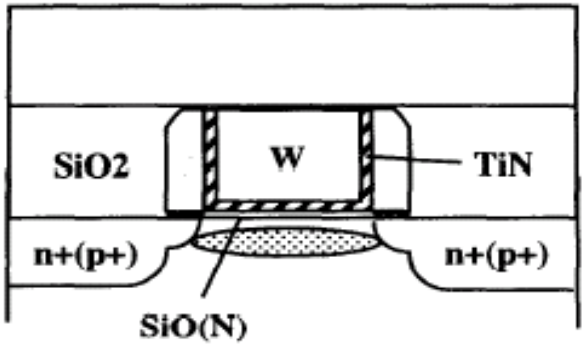
SMIT technology was applied to Damascene metal gate p-MOSFET Process

1) A self aligned dummy gate is formed after the shallow trench isolation formation.
2) A pre-metal dielectric film(SiO_2) is deposited by LP-CVD and planarized by the CMP process.
3) The dummy gates are etched away
4) By using SMIT, the ions are selectively implanted into the channel region
5) As a gate electrode , W/TiN is deposited in the groove
6) Then the CMP is performed to produce the metal Damascene gate structures.

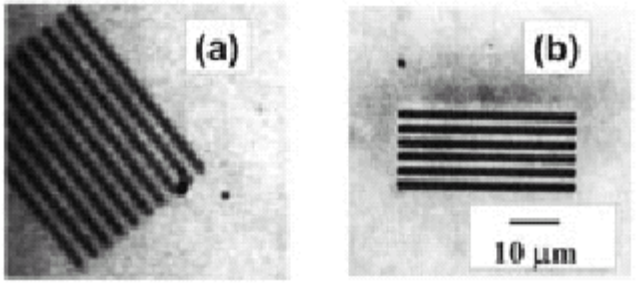


Stencil Mask Ion Implantation

Experimental results



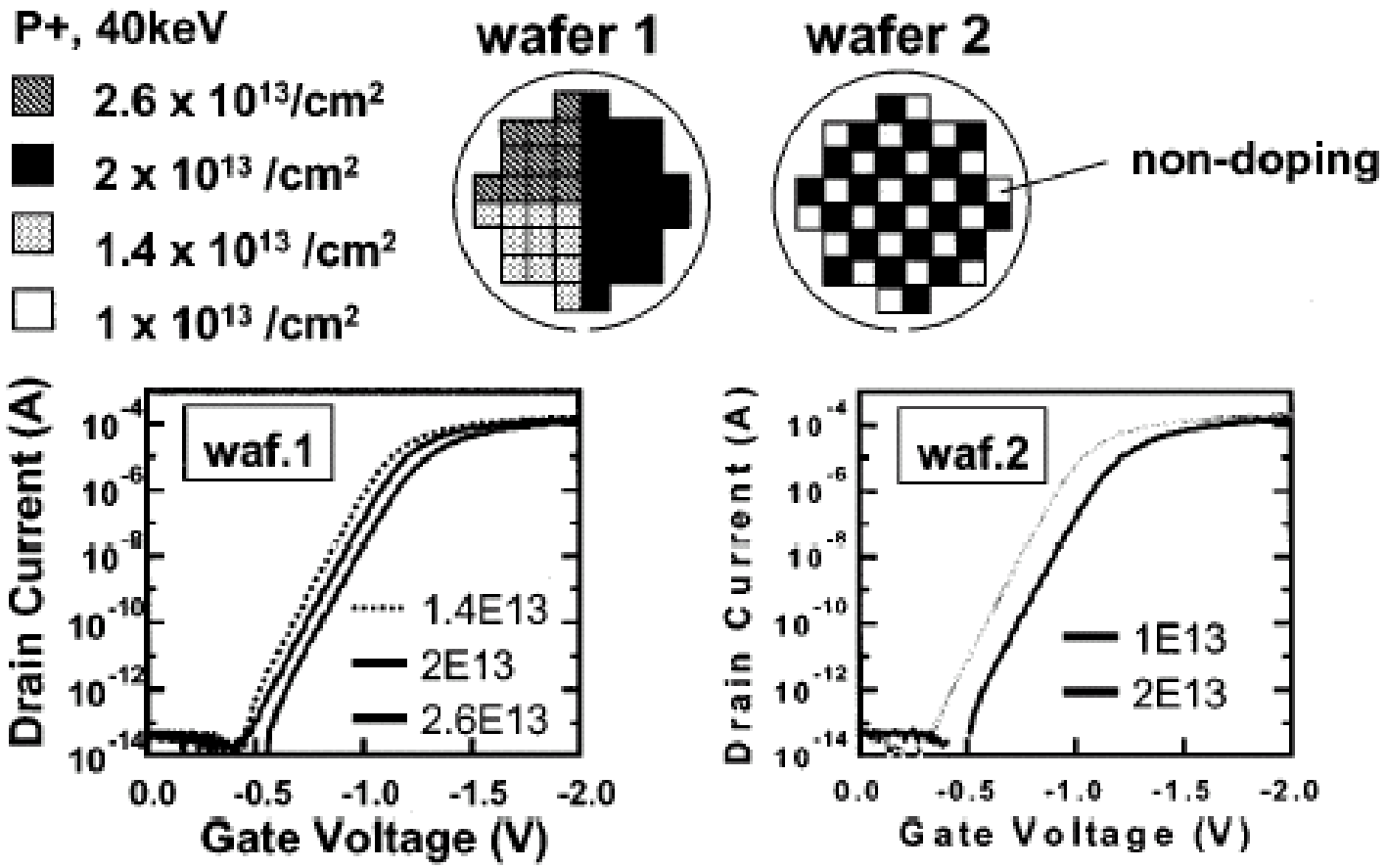
Schematic of Damascene metal gate p-MOSFET with selected area doped channel



Line pattern implanted region delineated by defect etching. Phosphorus ions are implanted into (a) a Si substrate and (b) a SiO_2 film on a Si substrate

Experimental results

Subtreshold characteristics of MOSFET in wafers.
Channel dose is varied chip by chip



Stencil Mask Ion Implantation

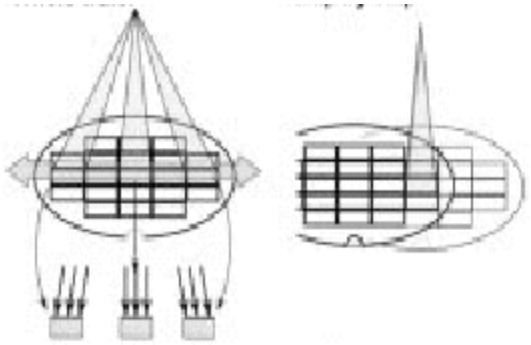
Device performance

SMIT offers the following advantages in device performance

1) *Reproducibility of implantation conditions*: The ability to reproduce implanted angular distributions

The implanted angle in the conventional method depends on the chip position and the angular distribution is about 0.5 degrees

In the case of SMIT the implantation is done over a very small area i.e. chip by chip and the implanted pattern does not change

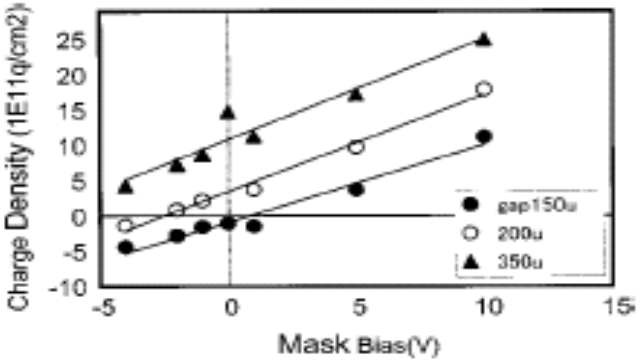


Improvement Device performance

2) *Reduction in Charge build up*

Ion implantation processing induces charge build up of wafer and hence causes the destruction of devices.

- **In conventional systems a secondary electron flood was used to neutralize the charges**
- **In SMIT it was observed that the charge buildup of wafer can be considerably reduced by charge neutralization.**
- **The mask bias is linearly related to the charge build up. Hence the charge build up is reduced by setting the mask bias to zero.**
- **The neutralizing effect also depends on the gap between the stencil mask and the wafer**



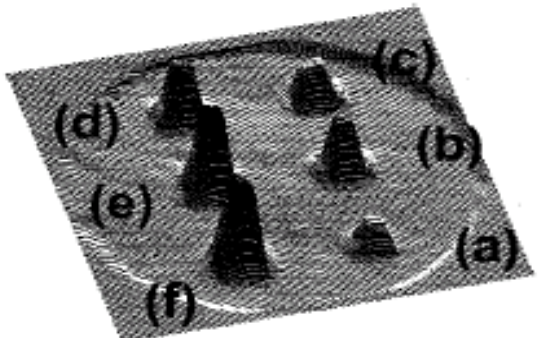


Fig. 6. A particular potential surface of implanted wafer using SMIT. Mask bias is 0 V. Distances between mask and wafer are (a) 150, (b) 200, (c) 250, (d) 300, (e) 350, and (f) 450 μm. The height of the potential corresponds to charge density due to charge buildup.

Justification

Economy

- As explained, the SMIT helps to reduce time
- The cost of ownership (COO) is reduced
- Power required is reduced to ¼th that of conventional processes because of avoiding the waste of power in wet processes
- The clean room necessary for this process is smaller than that of the conventional one.
- The target lifetime for the stencil mask is 10,000 wafers

In the case of 5E13/cm[2]

100 chips/8" wafer

	Time (sec)
Die alignment	0.25
Ion implant	0.20 [a]
Step movement	0.35
Waiting time	0.20

Through put is 25 wafers/hr
Conventional takes 3.8hrs

	RPT (Hour/Lot)	COO (Dollar/wafer)
Conventional	3.8 [a]	9
SMIT	1 [b]	4.5

Issues of SMIT

In order to use SMIT in all future implantation processes the following two issues are discussed

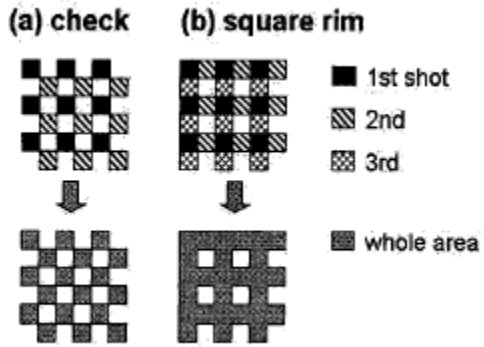
Pattern Formation

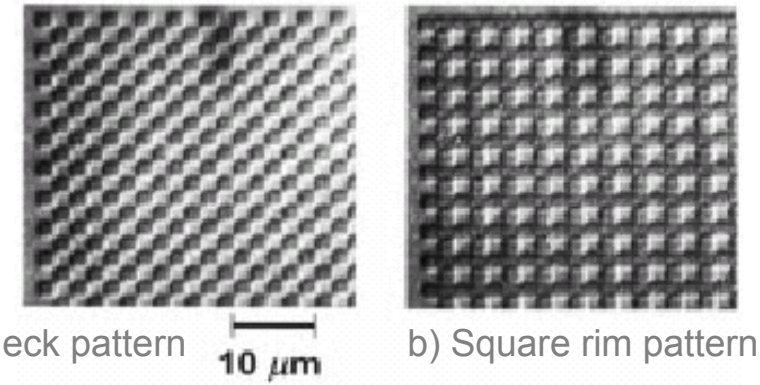
- **We know that it is impossible to make stencil mask with isolated patters**

Solution:

Such patterns were formed by performing implantation twice or more and some results obtained for check and square rim pattern are shown

A stencil mask with a n array of 2um square hole pitched 4um was used



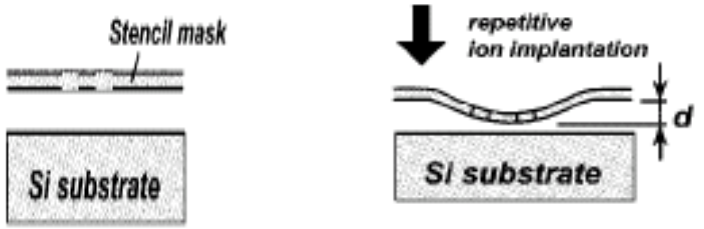


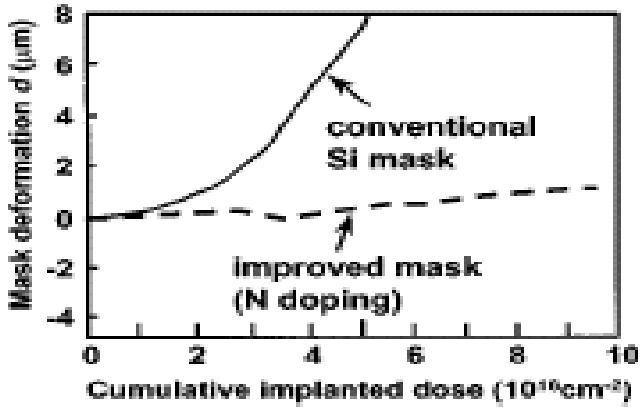
a) Check pattern b) Square rim pattern

Issues of SMIT

2) *Hardening of Stencil Mask*

- The stencil mask consists of Si membrane with 5-10 micron in thickness surrounded by 500 micron thick Si substrate.
- The distance between the stencil mask and Si substrate is set less than 100um and so the deformation of the mask membrane is very important.
- In order to harden the stencil mask impurities like nitrogen which increases the young's modulus of Si mask were implanted to the membrane.
- Work is going on in developing a non deforming mask and it has almost been achieved in the case of a doping exceeding 10^{18} ions/cm^2. This no corresponds to 1000 wafers with 100chips/wafer for process of 10^{13} ions/cm^2





Summary

- The SMIT technology is effective in reducing row process time, equipment cost an clean room space because process steps for photolithography can be eliminated from the implantation process.
- The advantages SMIT lie not only in fabrication but also in device performance as indicated.
- The SMIT was applied to the Damascene metal gate MOSFET fabrication process and the improved results were shown.

References

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