Gate Oxide Scaling for sub 100 nm Transistors

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To be covered

- Why to scale oxides?
- Benefits of oxide scaling
- ITRS Road Map
- Limitations of scaling
- Methods of scaling
- Viewpoints
- References

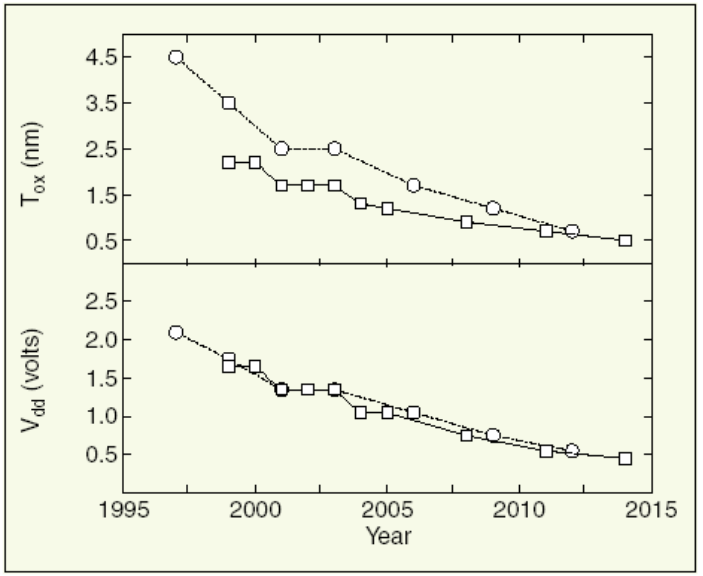
Why Scale?

- Higher Integration Density
- Higher performance
- Higher On Current
- Power dissipation maintained low
- Reduced gate delay
- Improved circuit speed
- Low program voltage of non-volatile memory

Roadmap by ITRS

Year	2000	2001	2002	2003	2004	2005	2008	2011	2014
Technology Generation	165nm	150nm	130nm	120nm	110nm	100nm	70nm	50nm	35nm
Gate Length (nm)	120	100	85	80	70	65	45	32	22
V_{dd} (V)	1.8	1.5	1.5	1.5	1.2	1.2	0.9	0.6	0.6
T_{ox} (nm)	2.5	1.9	1.9	1.9	1.5	1.5	1.2	0.8	0.6
Nominal I_{on} ($\mu A/\mu m$)	750/350	750/350	750/350	750/350	750/350	750/350	750/350	750/350	750/350
Maximum I_{off} ($nA/\mu m$)	7	8	10	13	16	20	40	80	160
Gate Delay CV/I (ps)	9.4	8.6	7.3	6.9	6.1	5.7	3.7	2.6	2.4
Gate R_s ($\Omega/\square$)	4-6	4-6	4-6	4-6	4-6	4-6	4-6	4-6	4-6
I_g @ 100℃ ($nA/\mu m$)	7	8	10	13	16	20	40	80	160
Sidewall Spacer (nm)	65-130	59-108	52-104	48-96	44-88	40-80	28-56	20-40	14-28
Active Poly Doping	2.2E20	3.1E20	3.1E20	3.1E20	3.9E20	4.6E20	5.4E20	7.3E20	1.2E21
Silicide Thickness (nm)	45	40	34	32	28	25	20	15	12
Drain Ext. X_j (nm)	36-60	30-50	25-43	24-40	20-35	20-33	16-26	11-19	8-13
Drain Ext. R_s ($\Omega/\square$)	310-760	280-730	250-700	240-675	220-650	200-625	150-525	120-450	100-400

Table 1 SIA's 1999 ITRS. High performance logic technology requirements.



1. The National Technology Roadmap for Semiconductors (NTRS) specifies expected trends for oxide thicknesses and supply voltages so that requirements of power dissipation and circuit speed for each successive technology generation are met. The predicted trends are based on simple models and historical scaling data. These roadmaps are often revised (dashed line: 1997, solid line: 1999) to accommodate industry's desire for faster ICs at an earlier date.

Issues: sub 100 nm

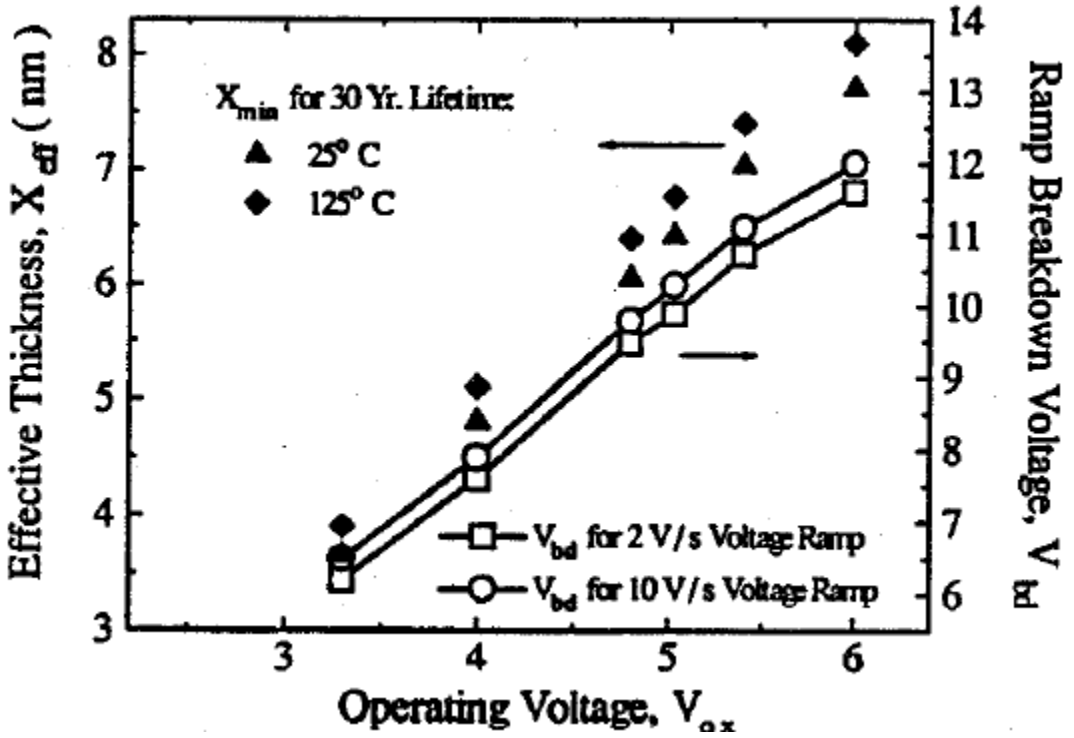
Issue	Due to
Short Channel Effect	Reduced channel length with less reduced junction depth and broadness.
Gate Leakage Current	Direct tunneling through ultra-thin oxide.
V_{th} Fluctuations	Gate length fluctuation, Dopants density fluctuations.
Gate Poly Depletion	Solid solubility limit, Increased vertical field, Boron penetration
Junction Capacitance	Higher doping and abrupt junction.
Mobility Degradation	Increased channel doping, Increased vertical field, Boron penetration.
Junction Leakage	Shallow junctions with silicide metallization.
S/D Resistance	Shallow junctions.
Gate Sheet Resistance	Narrow gate length.

Table 2 Issues of the CMOS scaling beyond 100nm.

Limitations

- Oxide breakdown
- Process induced damages
- Oxide leakage and device drift
- Higher I_{off}
- Transistor current and speed
- Reliability

Oxide breakdown



Process induced damage

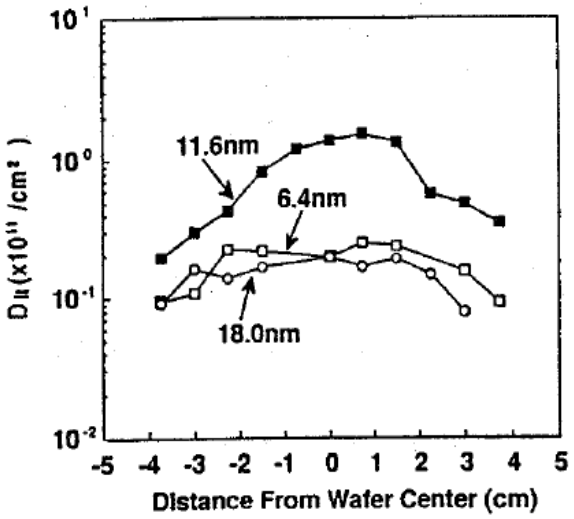


Fig. 3 Plasma process antenna-effect actually causes less damage to 6.4 nm oxide than 11.6 nm oxide.

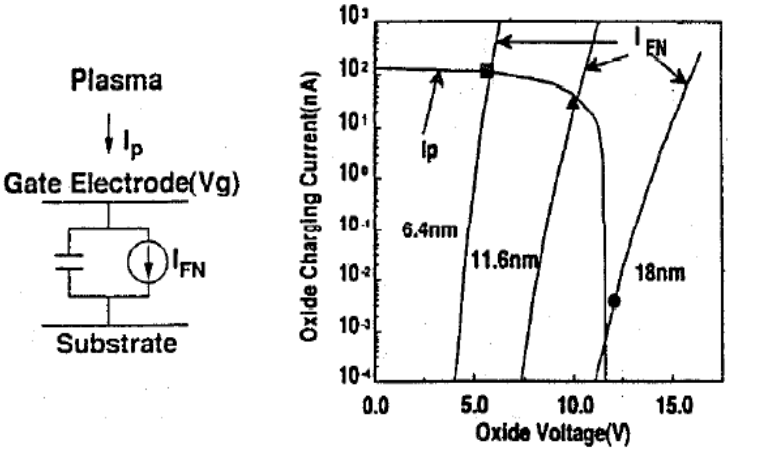
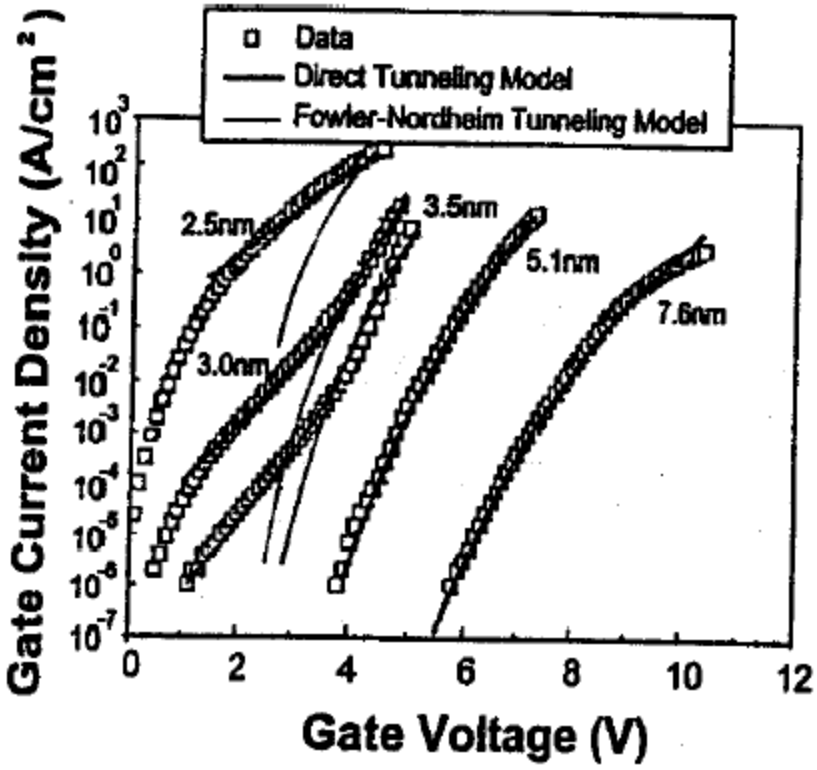


Fig. 4 Plasma charging (I_p) resembles a constant-current source rather than a fixed voltage source, therefore does not devastate very thin oxides. Included are three data points.

Oxide leakage and device drift

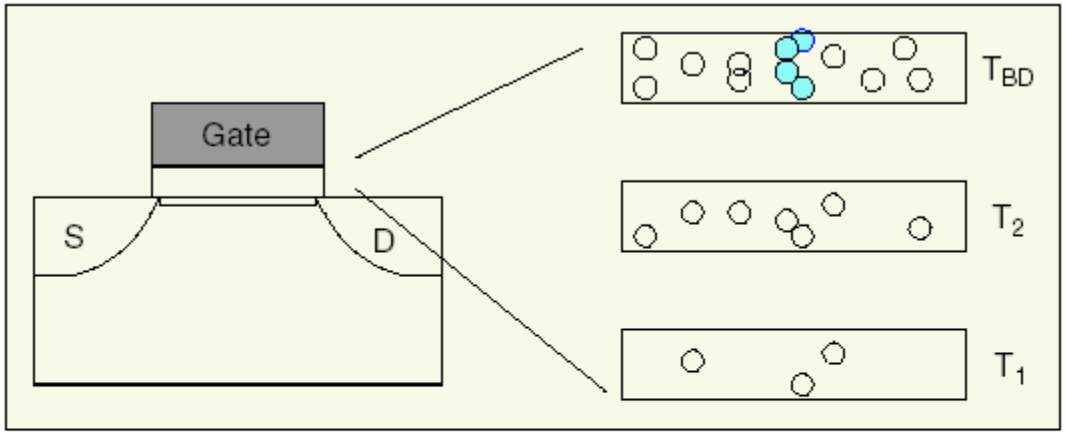


Direct tunneling may limit oxide scaling to around 2.5 nm.

How to achieve thinner oxides:

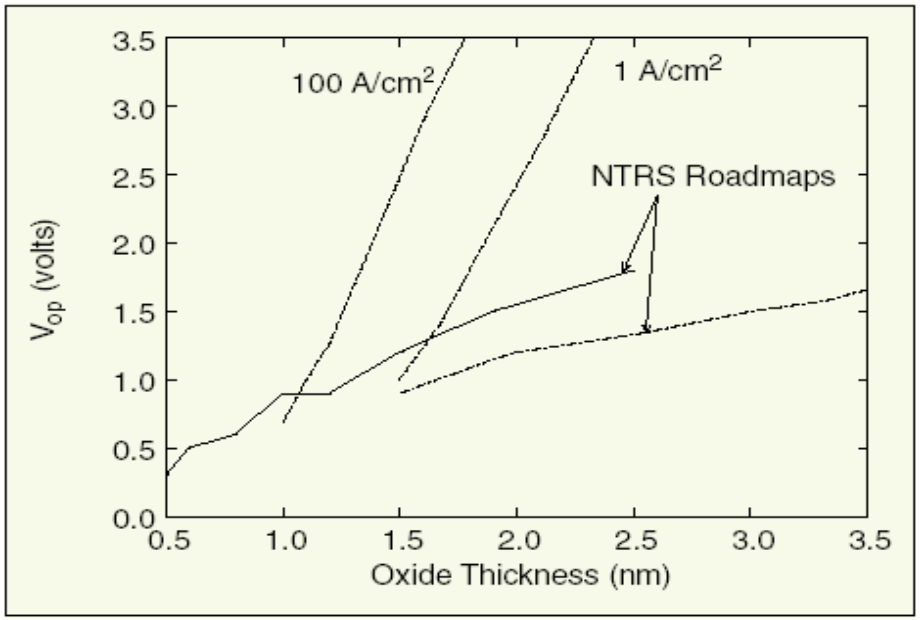
- Oxide scaling can be achieved if the following two main issues are addressed
  - Reliability
  - Gate leakage current

Reliability



2. Time sequence of the formation of the percolation path in an oxide film. Initially, at time t_1, the traps are distributed sparsely. With time, however, the traps begin to form clusters (t_2), one of which may eventually (T_{BD}) short-circuit the gate electrode to the substrate causing device malfunction. Since trap generation is a statistical process, different transistors will require different number of traps before the percolating bridge is completed.

Leakage problem



10. As oxide thickness is reduced, smaller applied voltage results in a specified leakage level. It is clear from this figure that 1 A/cm^2 limit of leakage current will be exceeded for oxides thinner than 1.6 nm if NTRS roadmap voltages are mandated. For 100 A/cm^2, the thickness limit is 1.1 nm

Alternatives

- replacing SiO_2 with other insulators having lower leakage
- Intelligent circuits
- Higher k-dielectrics
- Use of nitrided oxides
- Metallic gates

Viewpoints

- 1st group:
  - CMOS will continue to scale with corresponding scaling in gate oxide.
  - reliability is ensured
  - leakage will be managed by circuit techniques
  - "mobility limit" will be crossed with better processing.
- 2nd group:
  - leakage and mobility considerations will stop oxide scaling
  - double-gated structures will be necessary to obtain higher drive current.
- 3rd group:
  - leakage would prevent oxide scaling
  - layout difficulties could prevent double-gated structures.
  - alternate dielectrics with planar CMOS topology may be needed.

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