SOI Wafer Manufacturing

By Yong Wang

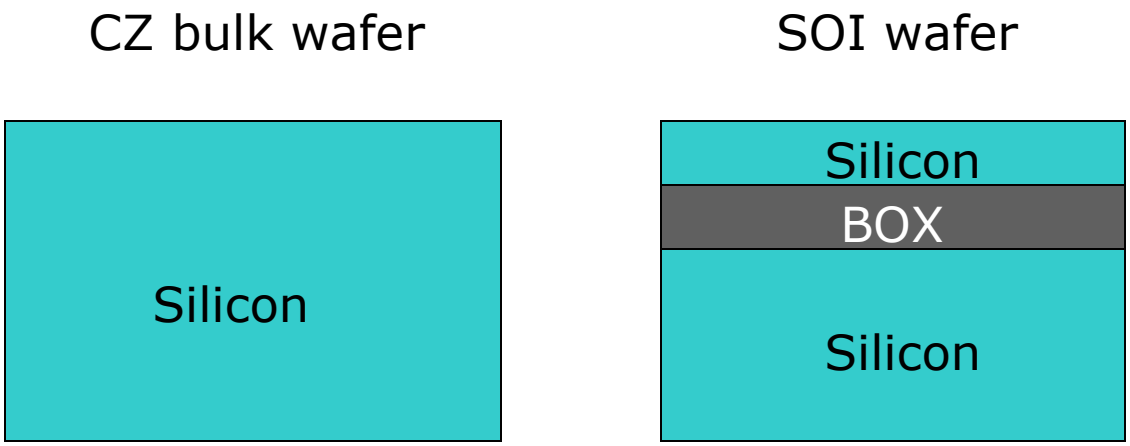
Outline

- What is SOI?
- Why SOI?
- SOI wafer manufacturing
- Conclusions

What is SOI?

- SOI is Silicon On Insulator-on the top of an insulator layer, a layer of silicon thin film is used to build active devices and circuits
- The first SOI devices were developed for early satellite and space exploration systems in the 1960s
- SOI wafer has a buried silicon oxide (BOX) layer extending across the entire wafer

CZ bulk wafer vs. SOI wafer

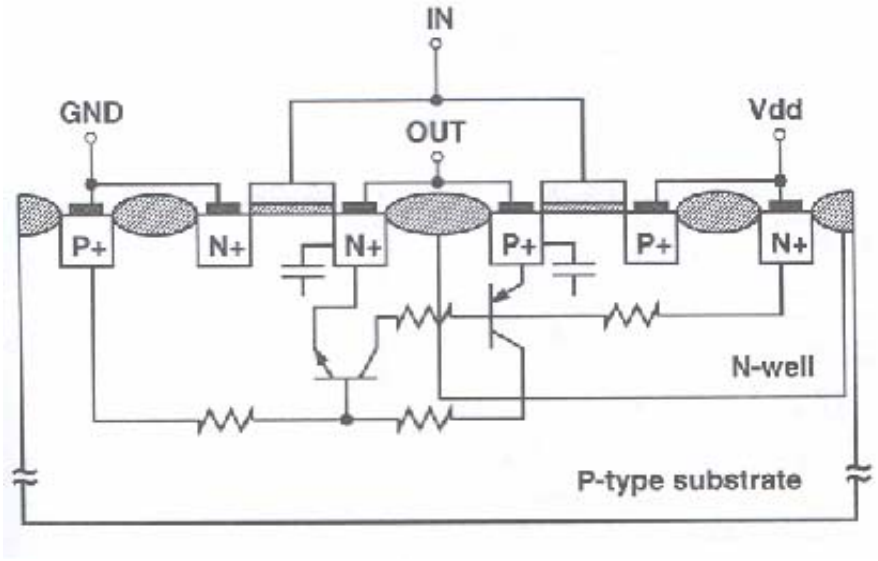


Why SOI?

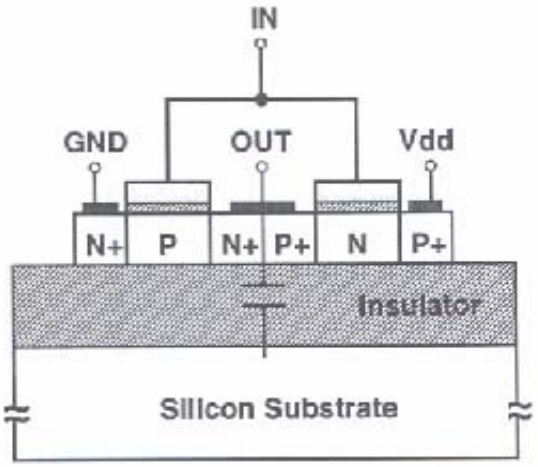
- High resistance to radiation
- Perfect transistor isolation
- Tighter transistor packing density
- Reduced parasitic capacitance

SOI CMOS devices

Bulk silicon CMOS

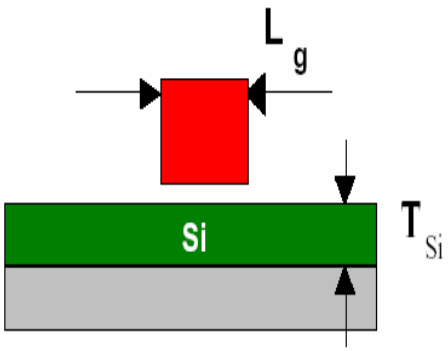


SOI CMOS

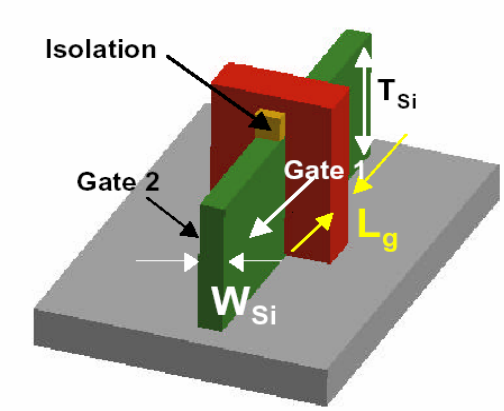


SOI devices

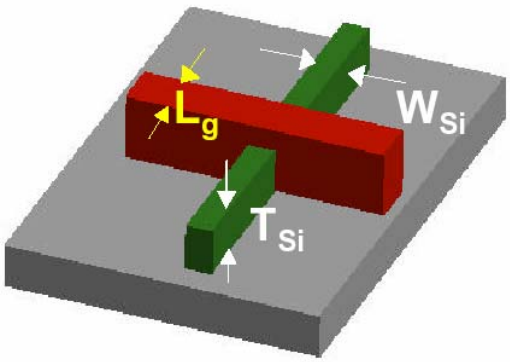
Single-gate SOI



Double-gate SOI



Tri-gate SOI



SOI wafer technology

- SIMOX (Separation by Implanted Oxygen)

  Vendors- Ibis, Epitronics/Nippon Steel, Mitsubishi
- Layer transfer approaches

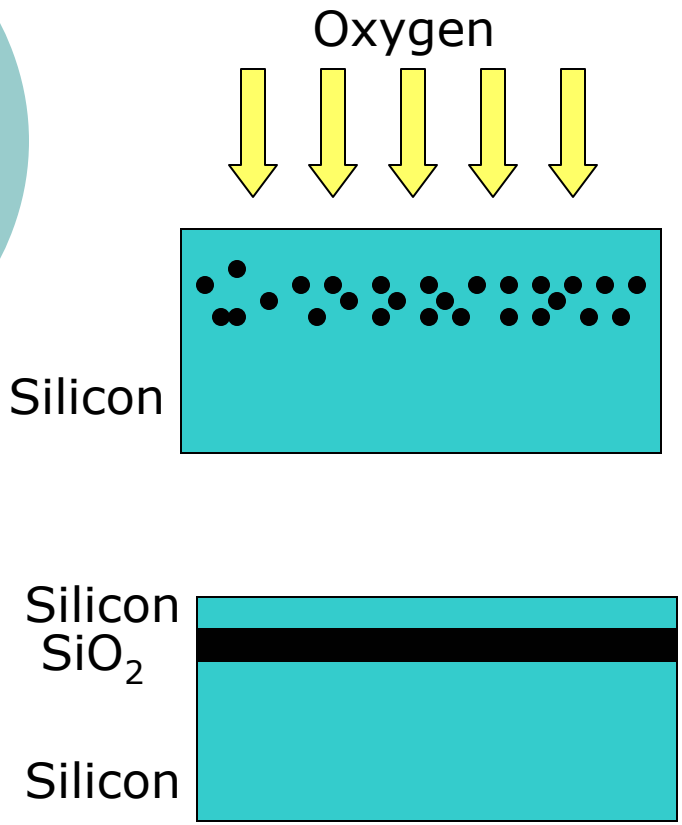
  - UNIBOND

  Vendors-SOITEC, SEH, SiGen

  - ELTRAN

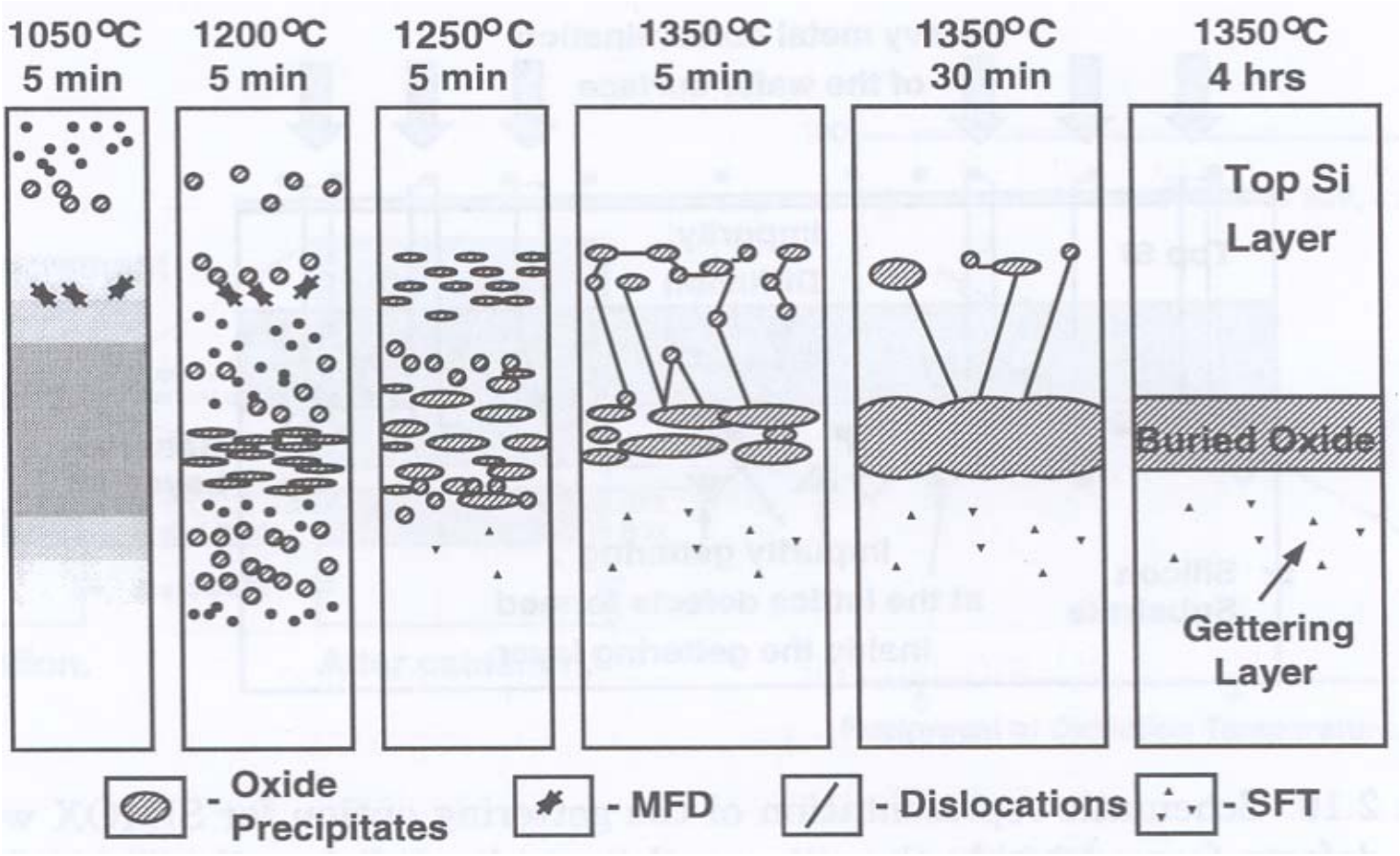
  Vendor- Canon

SIMOX



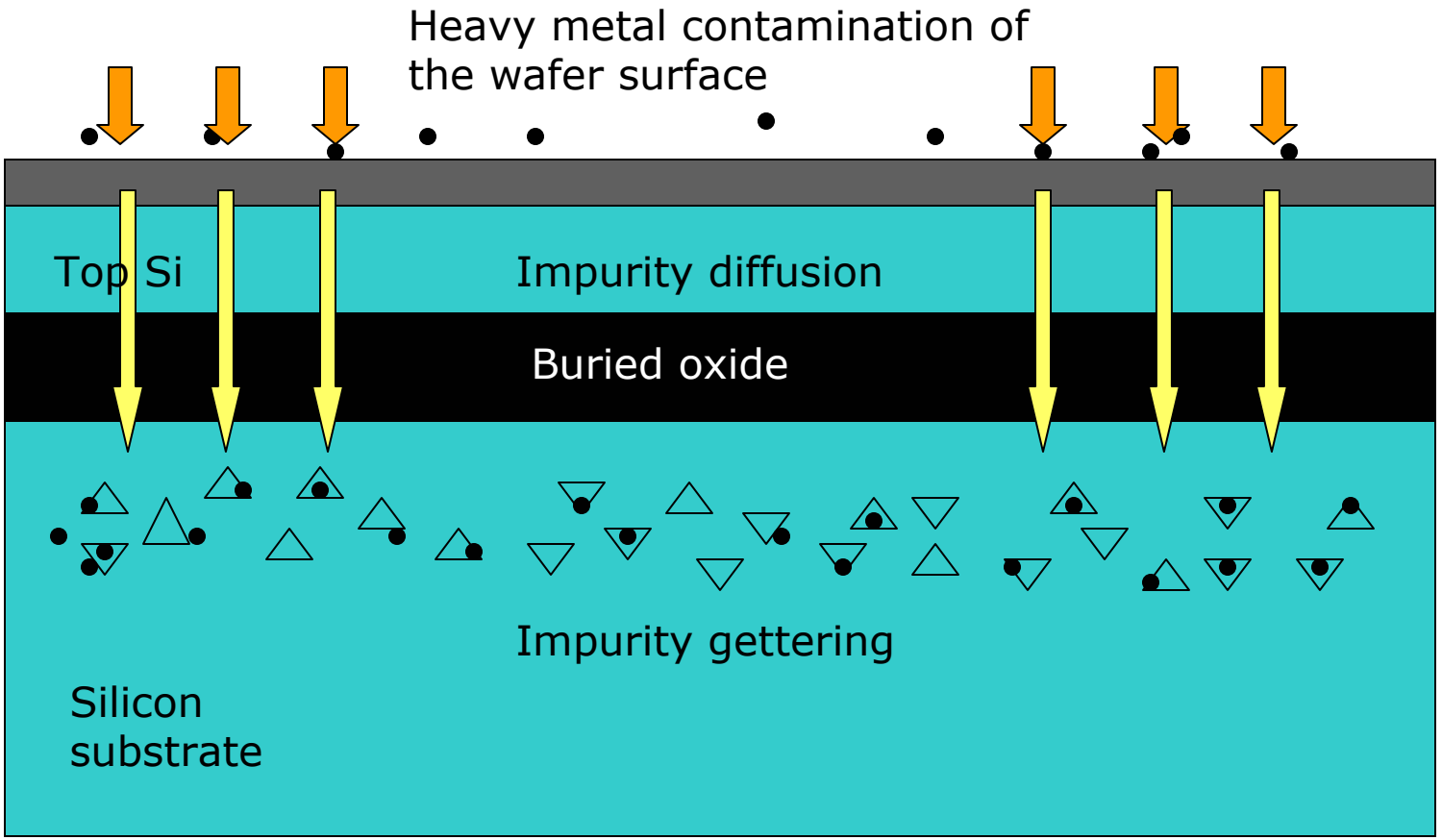
- Implant oxygen
- Anneal to form SiO_2
- Grow CVD EPI to required Silicon thickness
- Fabricate wafer

Evolution of SIMOX wafers

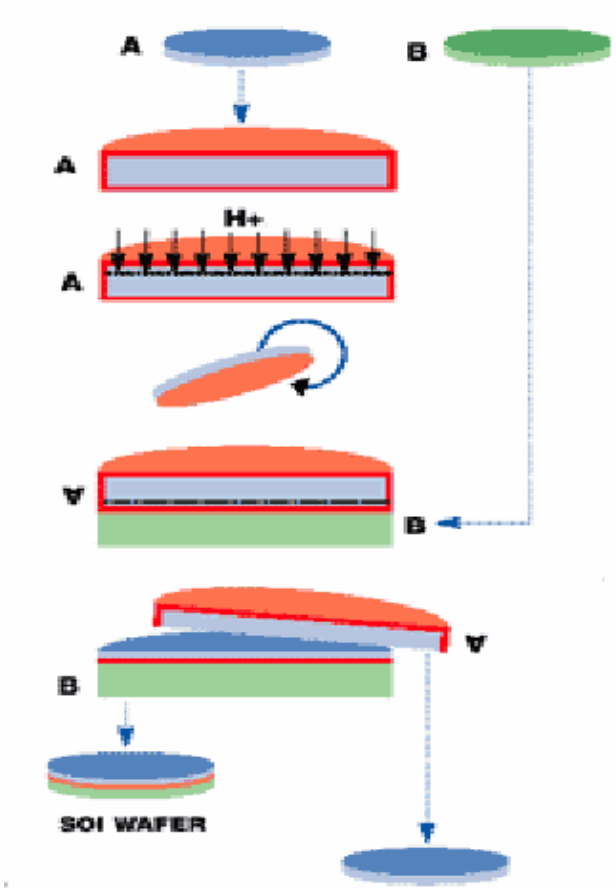


- James B. Kuo and Ker-Wei Su, *CMOS VLSI Engineering Silicon-on-Insulator (SOI)*

Gettering option for SIMOX wafers

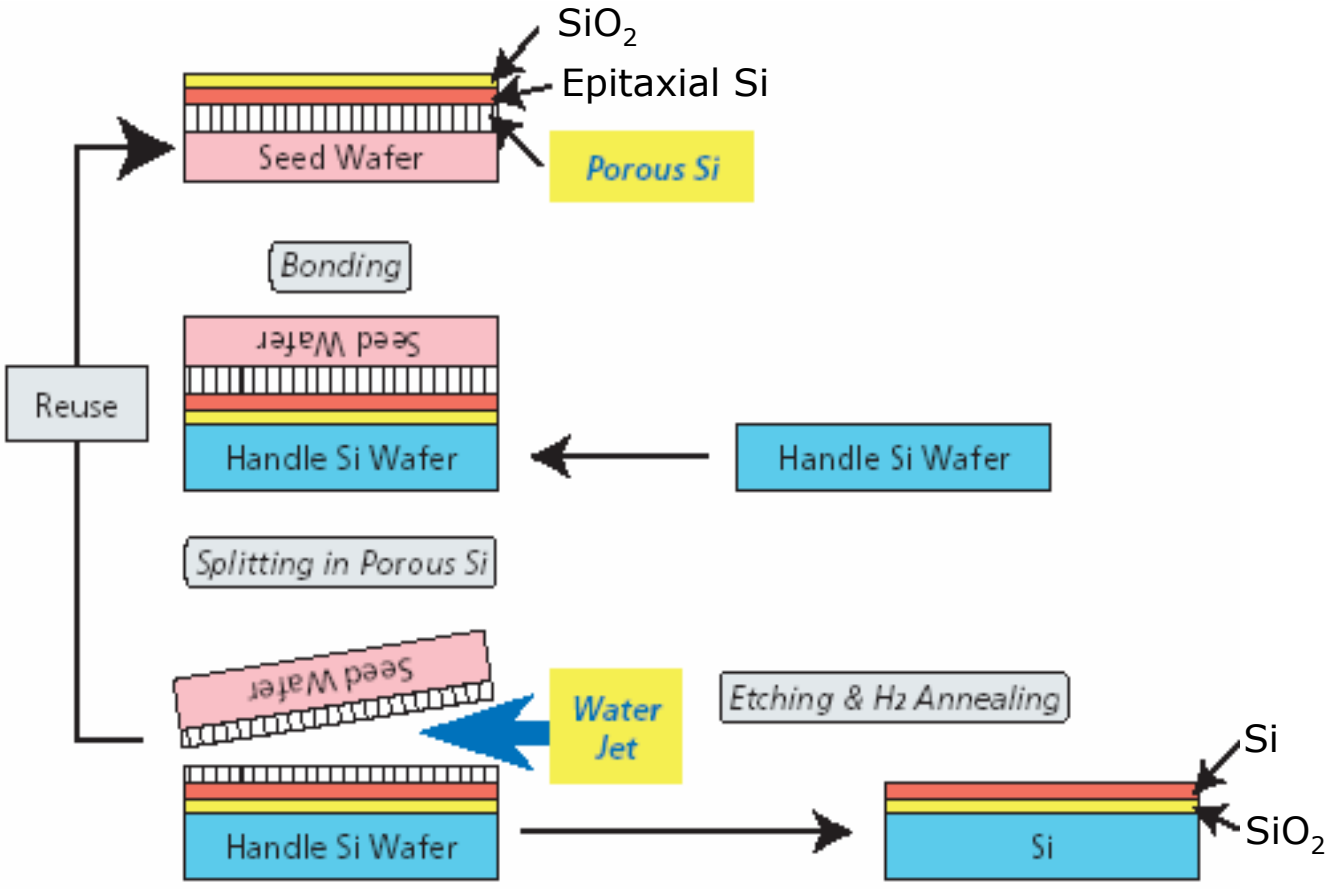


UNIBOND



- Initial silicon
- Thermal oxidation
- Hydrogen implantation
- Cleaning & bonding
- Splitting
- Annealing & CMP touch polishing
- Wafer A becomes new A

ELTRAN


SiO_2
Epitaxial Si
Seed Wafer
Porous Si
Bonding
Seed Wafer
Reuse
Handle Si Wafer
Handle Si Wafer
Splitting in Porous Si
Seed Wafer
Water Jet
Etching & H_2 Annealing
Si
SiO_2
Handle Si Wafer
Si

Conclusions

Property	NTRS target for 0.18 µm^2	Material Type		
		SIMOX [17]	Unibond [6]	ELTRAN [18]
Film thickness uniformity [Å]	50 - 200	20	50 [8]	16
BOX thickness uniformity [Å]	200	50	50 [8]	20
Surface roughness [Å]	1 – 1.5	3.0 [7]	1.5	1.5
Dislocation density [1/cm^2]	—	1000	100	Unknown
BOX (pipe) defects [1/cm^2]	0.09 – 0.12	1 [16]	— [7]	—
HF defects [1/cm^2]	0.11 – 0.14	0.1	1.0 [8]	0.05
Secco defects [1/cm^2]	4 - 5 x10^4	500	2x10^2 [10]	1x10^1
Surface metals [atm/ cm^2]	2.5x10^{10}	7x10^{10}	5x10^{10}	5x10^{10}
Price/Wafer for <1000 wafers		$1300	$1800	Unknown

- SIMOX is projected to be the winner for 300 mm SOI wafer fabrication because it is less expensive, logistically more straightforward, and already possesses widespread industry acceptance