# Strained Silicon (SiGe)

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# Outline

- Motivation / Introduction
- Advantages / Disadvantages
- Fabrication
- Problems / Future Work

# Motivation

- Device scaling
  - Decrease distance electrons/holes travel
  - Reaching limitations
- Mobility Enhancement
  - Decrease channel resistance
  - Decrease collisions

# What is Strained Silicon?

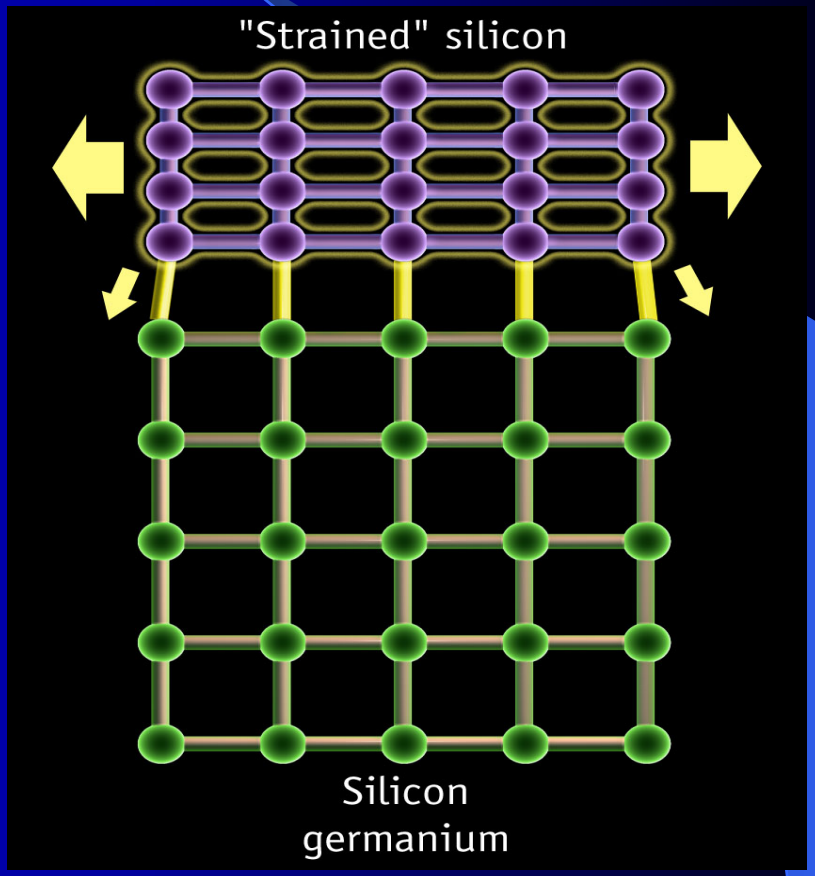
- Low-defect Strained Si Channel Layer
- Intentional Strain of channel
  - Mismatch of lattice constants (Si, Ge)
  - Increase in Silicon Lattice Spacing
  - Increase in Carrier Mobility
- $Si_{1-x}Ge_x$
  - Typical x ~ .15-.30

# What is Strained Silicon?

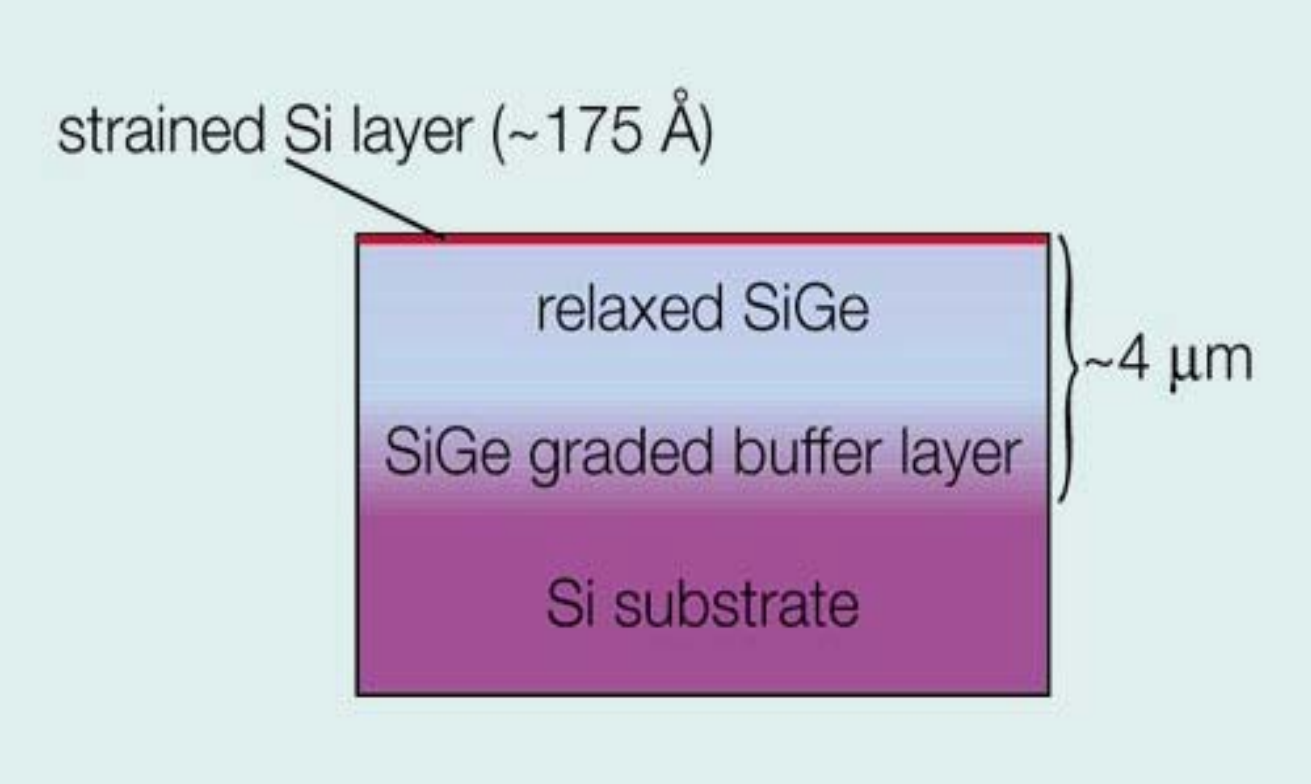
- Start with a conventional silicon wafer
- A thin layer of a SiGe
- A very thin layer of silicon is added on top of the SiGe layer.
- The Si layer atoms tend to align themselves with the more widely spaced atoms in the underlying layer.

# Strained Silicon Lattice

- Si – Ge Lattice Mismatch ~4.17%
- Si layer spreads out to match Ge lattice structure
- Decrease in channel resistance



# Strained Silicon Channel



# Advantages / Disadvantages

- Up to +70% Electron/Hole Mobility
- ~35% (nFET/pFET) drain current increase
- Less power consumption
- Unequal nFet / pFET carrier mobility improvement
- SiGe self-heating
- Addition of Fabrication steps
- Precise thin films

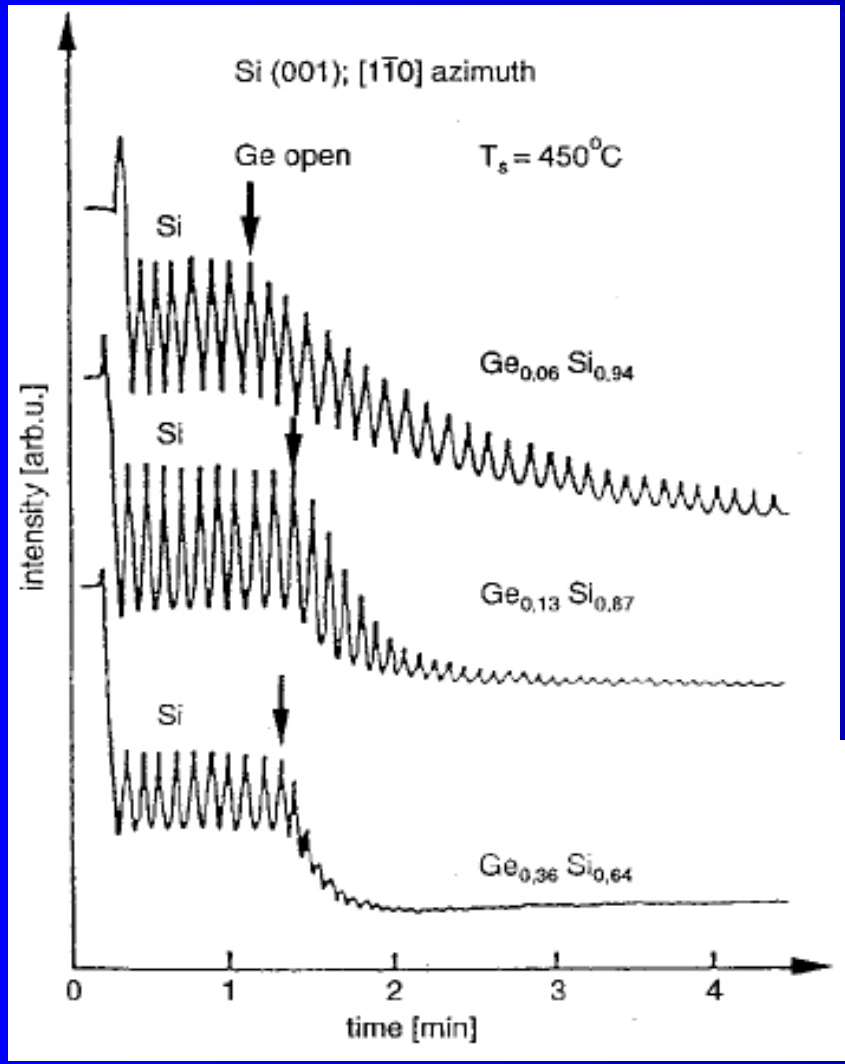
# Fabrication

- Difficult to produce dislocation-free SiGe layers on Si substrates due to mismatch
- CMP necessary of SiGe layer to remove surface roughness (reduce dislocations)
- MBE or UHV CVD

# Fabrication (MBE)

- Low density defects
- Addition of small amounts of Carbon to adjust strain ($Si_{1-x}Ge_xC_y$)
  - Gradual SiGe concentration on Si substrate
- Thin films
  - Reduce islanding
- RHEED monitoring of growth

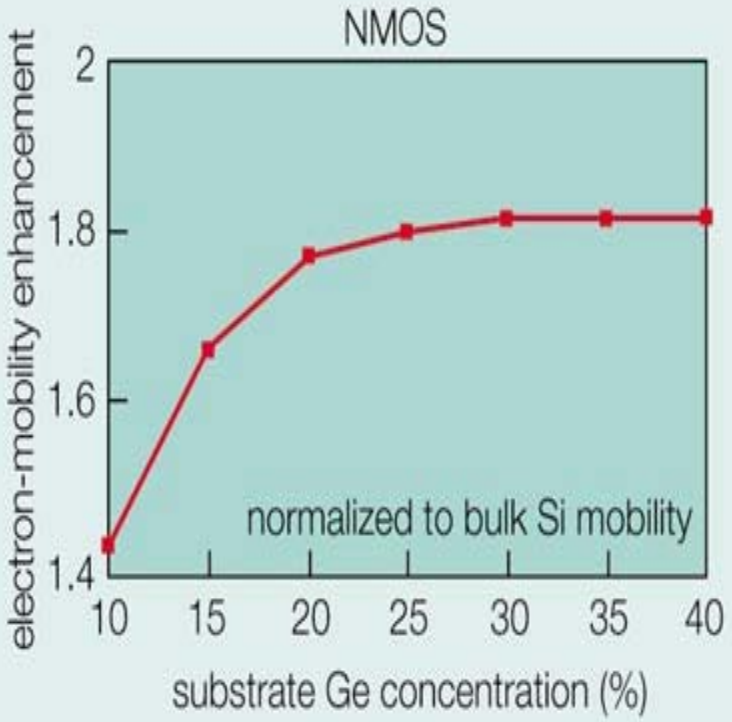
# Fabrication - RHEED

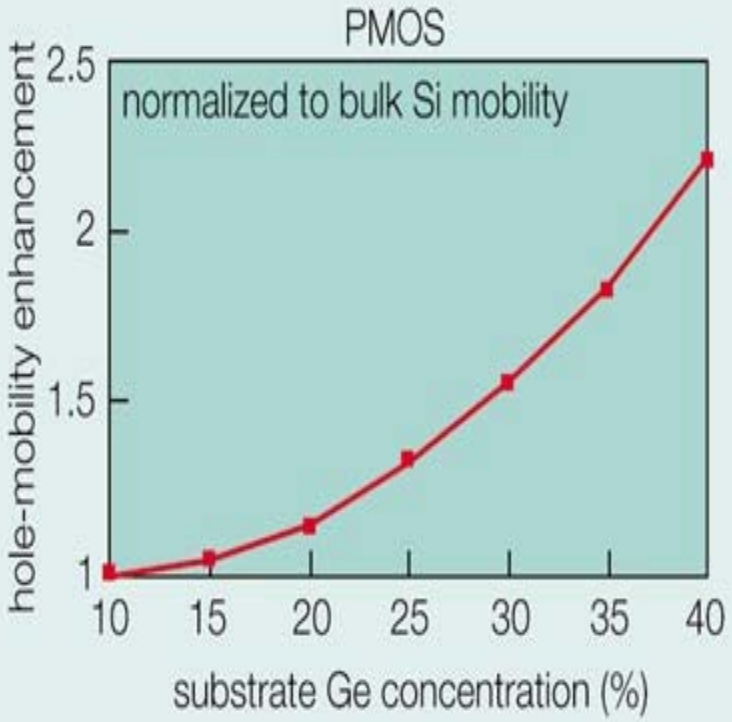



- Reflection High-Energy Electron Diffraction
- Accurate/Quick method to monitor MBE growth rates based on reflection

Fig.8: RHEED intensity oscillations of the specular beam during growth of $Si_{1-x}Ge_x$ on Si(001) at 450°C taken from the [1 $\bar{1}$ 0] azimuth for various Ge mole fraction. The Si growth (stable oscillation amplitude) preceded the alloy growth to determine alloy compositions (from SAKAMOTO et al. 1987).

# Problems


NMOS
electron-mobility enhancement
2
1.8
1.6
1.4
normalized to bulk Si mobility
10
15
20
25
30
35
40
substrate Ge concentration (%)


PMOS
hole-mobility enhancement
2.5
2
1.5
1
normalized to bulk Si mobility
10
15
20
25
30
35
40
substrate Ge concentration (%)

# Problems

- SiGe thermal characteristics cause self-heating in the Si and SiGe structures.
- Thin Si film above SiGe is necessary to eliminate “islanding”
- Increased Junction Capacitance
  - Lower bandgap
  - Higher dielectric constant

# Current Involvement

Table 1 – Selected Companies Involved in Strained Silicon
Source: Lubab Sheet, SEMI 2002

| Company | Strained Silicon Announcement | Implement Strained Silicon in Production | Initial Strained Silicon Geometry | Demonstrated Device Performance | Initial Strained Silicon Device Type |
|---|---|---|---|---|---|
| AmberWave Systems Corp. | 2001 | Not applicable | Not available | Electron and hole mobility enhancement factors of 1.5-2.2 | Various (HBT, MOSFET, PMOSFET) |
| IBM Microelectronics | 2001 | 2005 | 65 nm | 30% improvement in drain current | Demonstrated NMOSFET with strained silicon channel |
| Hitachi Ltd. | 2001 | Not available | <100 nm | 70% improvement for current drive in n-channel and 51% for p-channel | MOS transistors with strained silicon channel |
| Intel Corp. | 2002 | 2H2003 | 90 nm | 10-20% increase in transistor current flow or drive current | Demonstrated on 52 megabit SRAM chips to be used as a prototype in the production of Pentium 4 microprocessor "Prescott" |

# Future Work

- Maintaining the integrity of the strained Si channel through subsequent processing at higher temperatures to prevent the relaxation of the strain
- Managing Self-heating Problem
- Combining Strained Si and SOI for faster transistors