Fabrication of ultrashort MOSFET

-----presented by Yan Yi

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Outline

- Introduction
- Fabrication of the devices
- Electrical characterization
- Conclusion

Introduction

- To scale down MOSFET , requires the development of devices with increasingly shorter channel lengths.
- Constrains on MOSFE of extremely small size
  - the processing technologies
    - the limited resolution of lithographic tool
  - the operating principles
    - short channel effect
- To improve device output characteristics

  a combination of

  1) ultra-shallow source and drain junctions

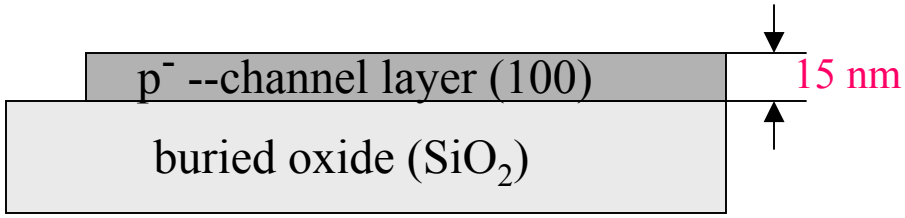
  2) an extremely thin gate oxide film

  3) a thin active silicon layer

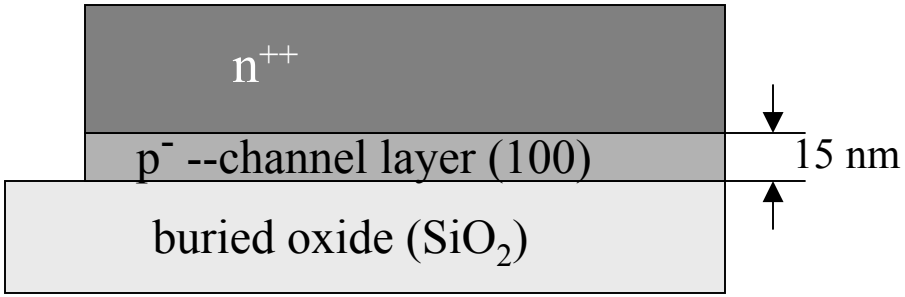
---- by Wong et al

Fabrication of the devices

- an SOI wafer with a thin, undoped silicon-(100) film (p^- ~ 5×10^{14} cm^{-3}) on top

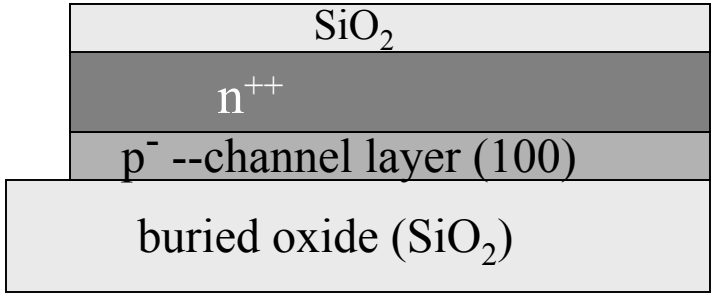


- molecular beam epitaxy to grow a highly Sb doped n^{++} layer (approx. ~ 10^{20} cm^{-3})

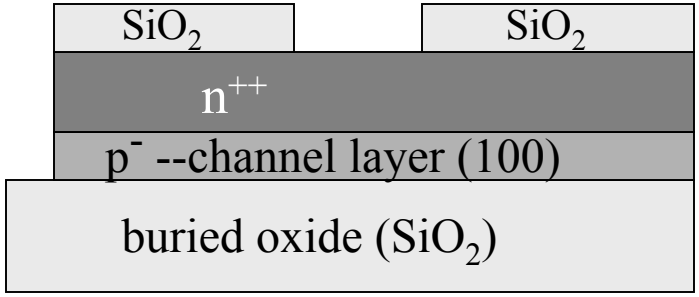


Fabrication of the devices

- a thin SiO_2 film is generated on top of the n^{++}/p^{-} stack



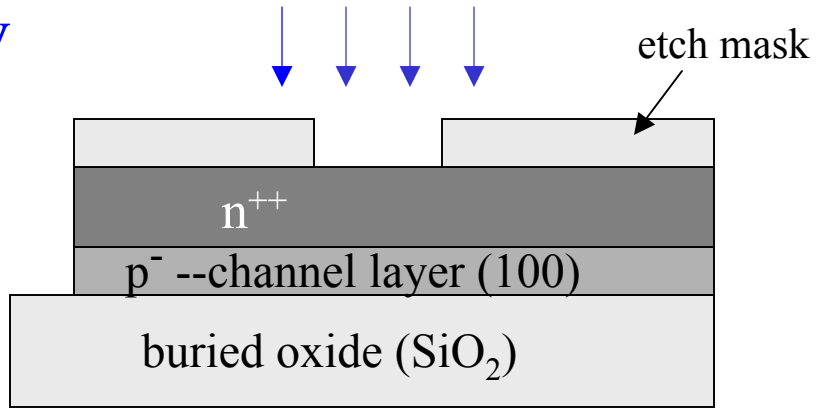
- SiO_2 is etched in buffered oxide etch (BOE)



Fabrication of the devices

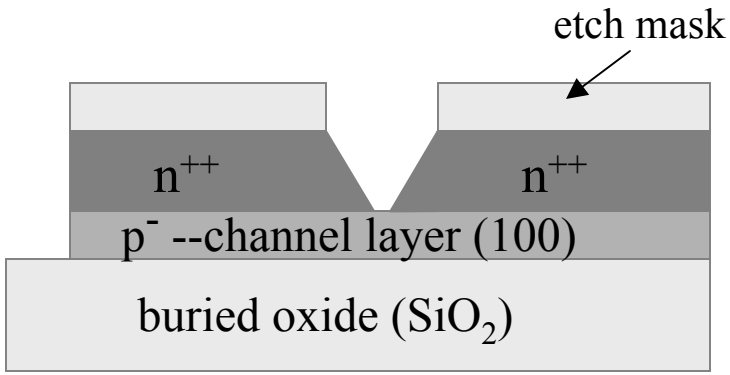
- etch the n^{++} layer anisotropically

  a solution of 40% KOH solution mixed with 5% isopropyl alcohol at room temperature



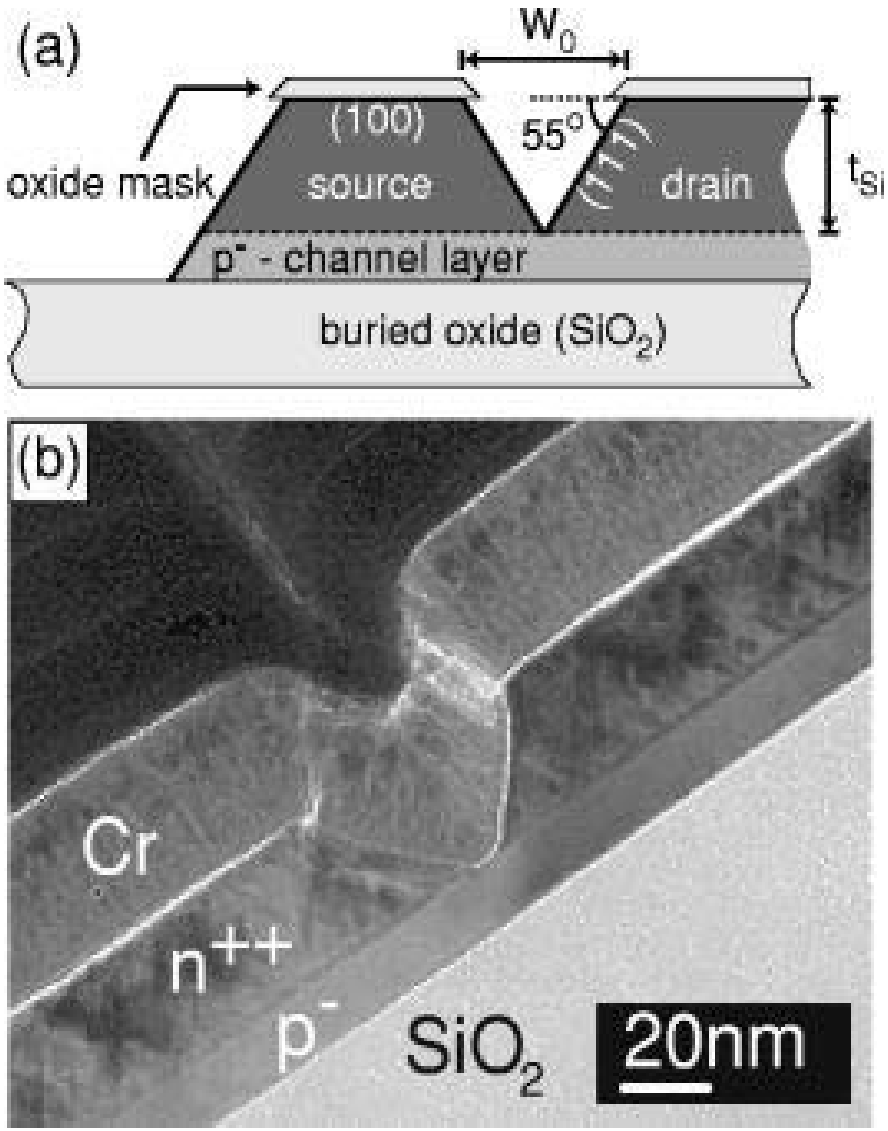
Etching results

- a V-groove is formed in the n^{++} layer
- the separated n^{++} areas serve as source and drain
- the channel is formed in the p^- region at the tip of the V-groove in between source and drain.



Reasons

- the etch ratio between the {100} and {111} plans is about 400:1.
- the flanks of the V-groove consist of two intersecting {111} planes.



Figure(b)

sub-10 nm MOSFET

(30 nm n^{++} layer grown on a 15 nm p^- SOI wafer)

(b)TEM image

Two major benefits

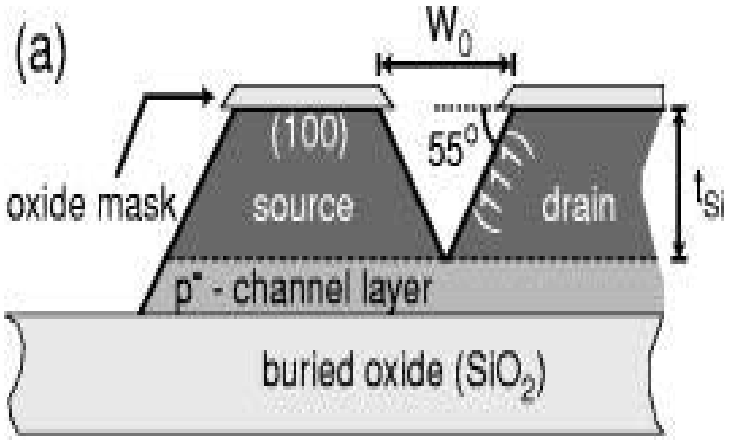
- Compensate for the limited resolution of the lithographic tool by adjusting the thickness t_{si} of the epitaxy layer

  W_o can be much larger and depends only on the thickess t_{si} .

- The process is self-limiting

  once the V-groove is formed the etching essentially stop

$$t_{si} \approx W_o / \sqrt{2}$$



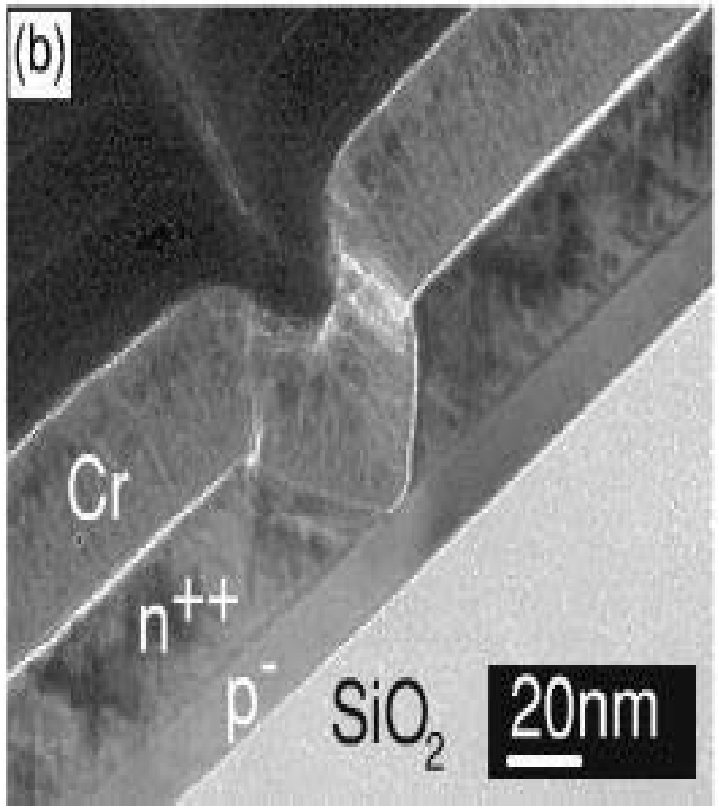


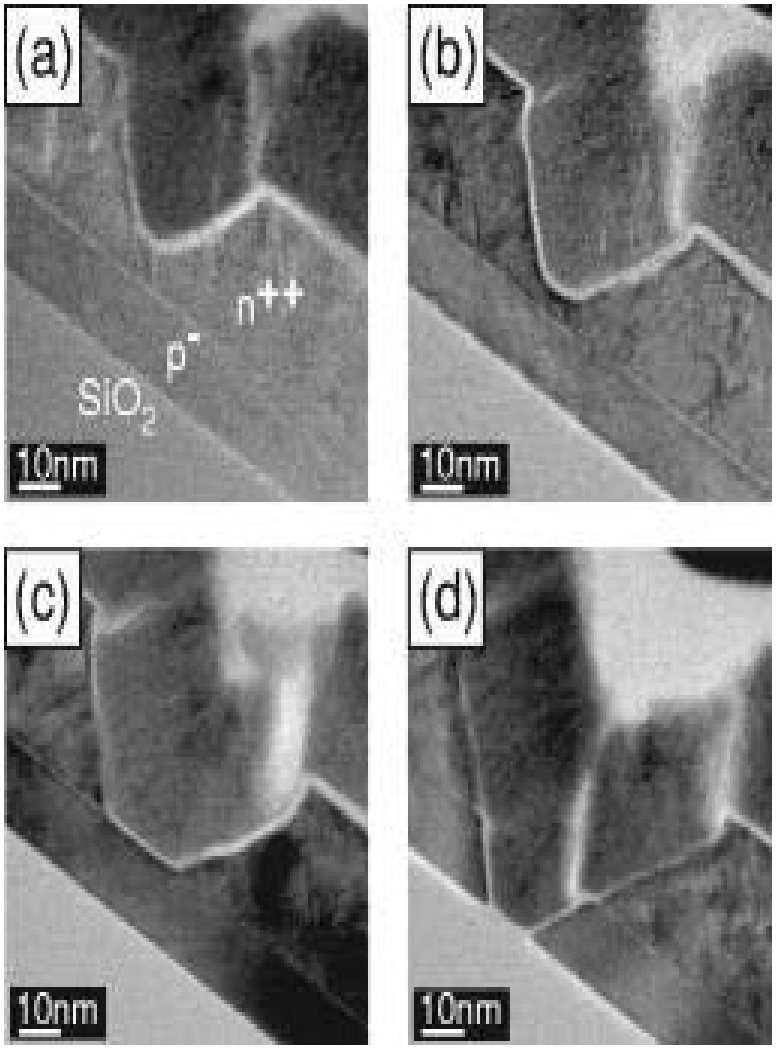
Figure: The resulting profiles for different openings in the oxide mask but the same etching time

(a)(b) small openings in the oxide mask which lead to incomplete etching of n^{++} layers. The source and drain regions are short.

(d)large opening: the whole n^{++} / p^{-} stack is etched away and the source and drain regions are isolated from each other.

(c)a smaller etching rate at the n^{++} / p^{-} interface which yield a V-groove with a flat bottom

A device can only be formed when the channel length is ultrashort (smaller than approximately 35 nm)



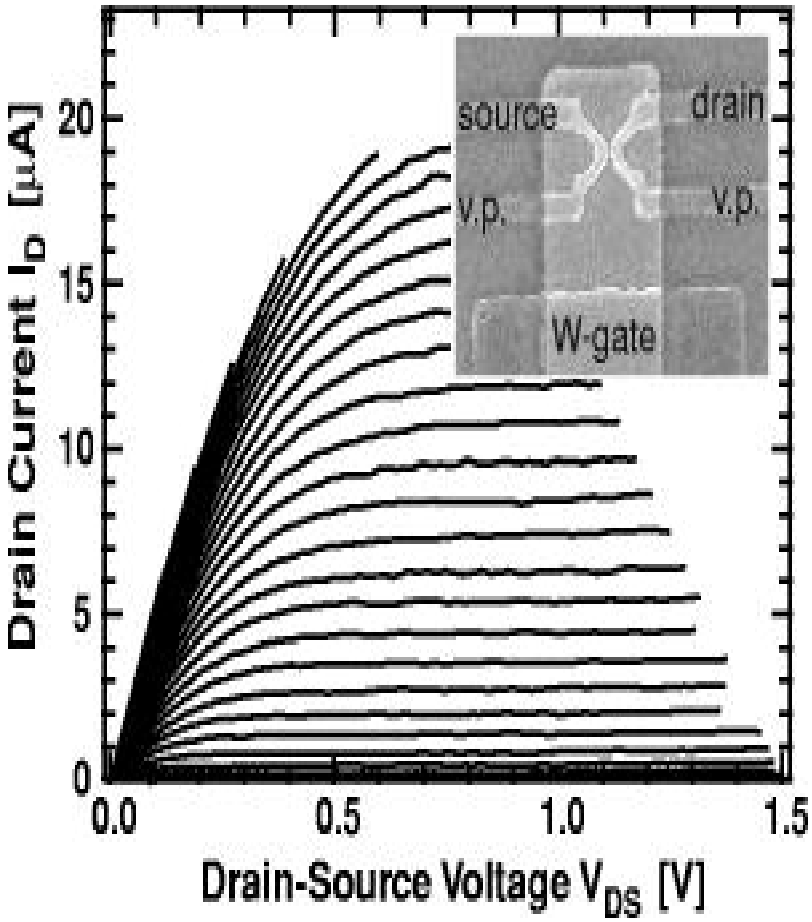
Fabrication of the devices

- grow gate oxide film
- pattern gate tungsten layer

Electrical characterization

- An efficient suppression of SCEs in the transistor

  The slope of the curve in the saturation region is close to zero
- Vthreshold ~0.5V which is close to the expected value for the midgap work function of the W-gate electrode.
- The slope of the subthreshold characteristics is ~100mV/decade close to the value for a typical long channel device (roughly 80mv/decade)
- A current modulation of more than 5 orders of magnitude



Conclusion

- A source-drain separation as small as 10nm can be achieved
- Only small impact of short-channel effect can be fabricated in the described way
- The well reproduced dependence between etch depth and V-groove opening allows to generate sub-30 nm channel lengths with lithographical structures of 150nm or more. Thus, it is possible to use optical lithography for the generation of ultra-small transistors showing ballistic electron transport at room-temperature.