# ECE 3040B Microelectronic Circuits

*Exam 2*

*March 21, 2002*

*Dr. W. Alan Doolittle*

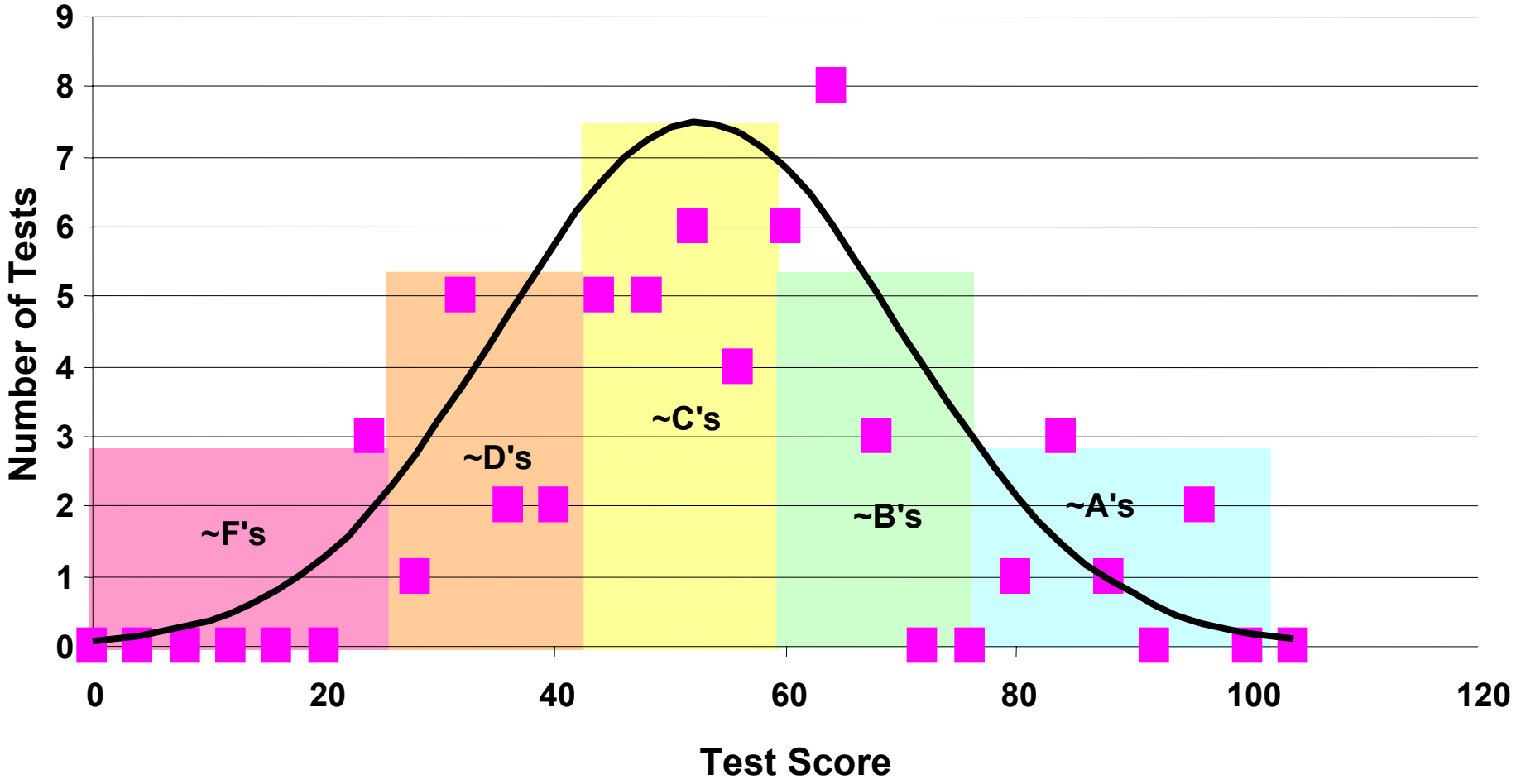
Print your name clearly and largely: Solutions

**Instructions:**
Read all the problems carefully and thoroughly before you begin working. You are allowed to use 1 new sheet of notes (1 page front and back), your note sheet from the previous exam as well as a calculator. There are 100 total points in this exam plus 10 points bonus (all or nothing). Observe the point value of each problem and allocate your time accordingly. SHOW ALL WORK AND CIRCLE YOUR FINAL ANSWER WITH THE PROPER UNITS INDICATED. Write legibly. If I can not read it, it will be considered to be a wrong answer. Do all work on the paper provided. Turn in all scratch paper, even if it did not lead to an answer. Report any and all ethics violations to the instructor. Good luck!

Sign your name on **ONE** of the two following cases:

I DID NOT observe any ethical violations during this exam:

I observed an ethical violation during this exam:




| Class Totals | Problem # ==> | #1 | #2 | #3 | #4 | #5 | #6 | #7 | #8 | Bonus |
|---|---|---|---|---|---|---|---|---|---|---|
| Number of Tests= | 57 | | | | | | | | | |
| Point Value of problem= | | 5 | 5 | 5 | 5 | 5 | 15 | 20 | 40 | 10 |
| Individual Problem Average= | | 22.8 | 36.8 | 93.0 | 82.5 | 80.7 | 81.4 | 30.5 | 45.4 | 3.5 |
| Exam Average= | 52.6 | | | | | | | | | |
| Exam Standard Deviation= | 17.4 | | | | | | | | | |
| Exam Max= | 95.0 | | | | | | | | | |
| Exam Min= | 23.0 | | | | | | | | | |

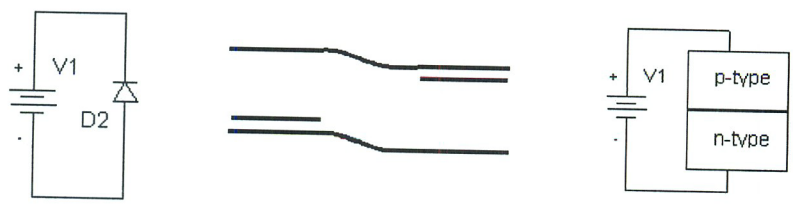
***First 40%*** **Multiple Choice (Select the most correct answer)**

1.) (5-points) The built in potential of a p-n junction is:
   a.) Is smaller when the doping concentrations in the n and p regions are large
   b.) Sets a practical upper limit to voltage that can be applied in reverse bias
   c.) Sets a practical upper limit to voltage that can be applied in forward bias
   d.) Is equal to 0.6 to 0.7 for all diodes.
   e.) None of the above.

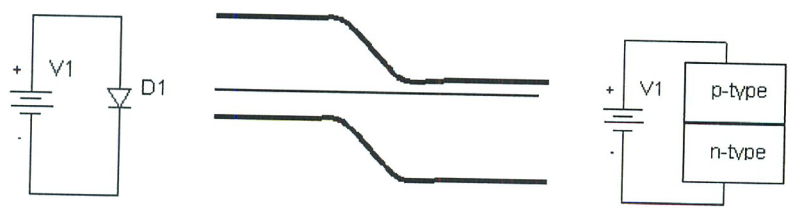
2.) (5-points) The diffusion capacitance of a p-n junction…
   a.) …is negligible in forward bias.
   b.) …is always larger than the depletion capacitance
   c.) …results from minority carrier injection across the junction under forward bias
   d.) …results from majority carriers seperated by the depletion region
   e.) both a and c

3.) (5-points) Which of the following bias diagrams is consistent with reverse bias (all three diagrams must be correct, i.e. the schematic symbols, energy band diagrams and the material drawing must have the correct polarity)?

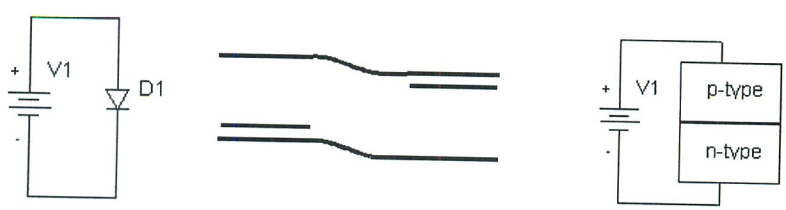
a.)



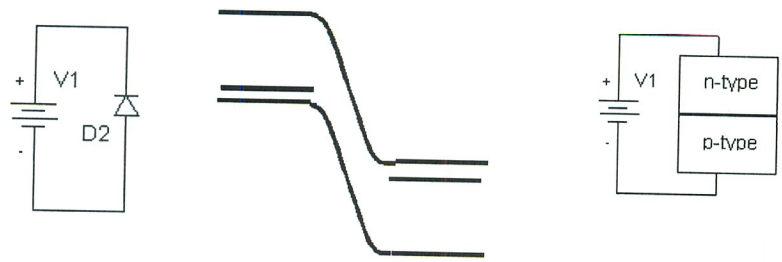

b.)



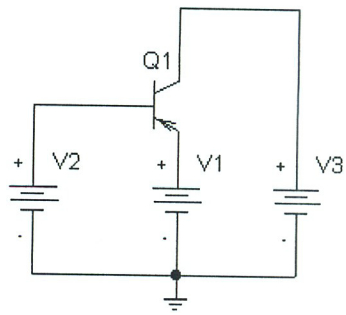

c.)




d.)



4.) (5-points) If a Clemson engineer wanted to bias this transistor into inverse active mode, which of the following is true?




a. V3>V1 and V1>V3
b. V1>V2 and V3>V2
c. V2>V3 and V1>V3
d. V2>V1 and V2<V3
e. You cannot bias a transistor without resistors.

5.) (5–points) For what conditions can the Ebers-Moll model be used?

a. DC solutions
b. Transient solutions
c. AC solutions
d. All of the above
e. None of the above (the Ebers-Moll Model can never be solved).

6.) (15-points)
For the each of the following transistor bias modes circle the letter of all phrases that are true:
Saturation:

a.) Useful for amplifiers
b.) Useful as a conducting switch
c.) Useful as a switch that is not conducting
d.) Has a forward biased base-emitter junction
e.) Has a reverse biased base-collector junction
f.) Has a reverse biased base-emitter junction
g.) Has a forward biased base-collector junction
h.) Can be analyzed using the Ebers-Moll Model
i.) Can be analyzed using the small signal model

Not true ⟹

Cutoff:

j.) Useful for amplifiers
k.) Useful as a conducting switch
l.) Useful as a switch that is not conducting
m.) Has a forward biased base-emitter junction
n.) Has a forward biased base-collector junction
o.) Has a reverse biased base-emitter junction
p.) Has a reverse biased base-collector junction
q.) Can be analyzed using the Ebers-Moll Model
r.) Can be analyzed using the small signal model

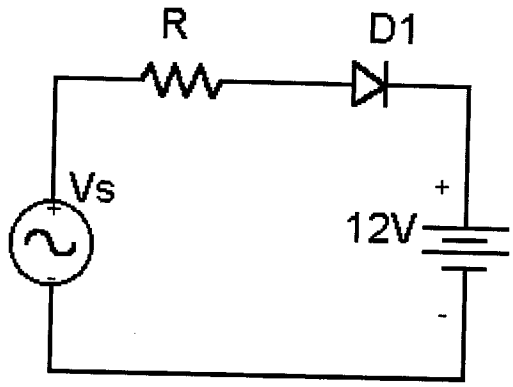
Forward Active:

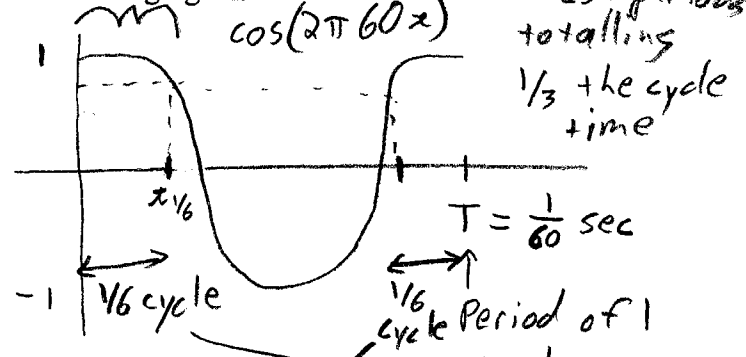
s.) Useful for amplifiers
t.) Useful as a conducting switch
u.) Useful as a switch that is not conducting
v.) Has a forward biased base-emitter junction
w.) Has a forward biased base-collector junction
x.) Has a reverse biased base-emitter junction
y.) Has a reverse biased base-collector junction
z.) Can be analyzed using the Ebers-Moll Model
aa.) Can be analyzed using the small signal model

***Third 20%***

7.)(20-points)

You are asked to design a automotive battery charger using a 60 Hertz sinusoidal voltage source described by, $V_s=V_{amp}\cos(2\pi 60t)$. In order to prevent the battery from overheating (and possibly exploding) two conditions must apply: 1.) The charging duty cycle (percentage of the 60 hertz cycle the for which the battery is charging) must be kept to 1/3 a cycle (i.e. charging only occurs for 1/3 of the 60 Hertz cycle) and 2.) the peak current drawn must be less than 0.12 A. Using the ideal diode model, determine the proper value of $V_{amp}$ and R to achieve the design goal.




Charging will only occur during these periods totalling 1/3 the cycle time

The diode only conducts current (charges the battery) when $V_s > 12$ V. This means we need to pick $V_{amp}$ such that $V_{amp}\cos(2\pi 60x)$ is only greater than 12 V for 1/3 of a cycle. Note: At the instant the Diode sees from off to on no current flows so $V_s = 12$V. Thus, $V_{amp}\left[(2\pi 60)\frac{1}{360}\right] = 12$ V

add together to get 1/3 cycle

Some need to use $x = \frac{1}{6}T$ or $\frac{1}{360}$ sec

$$V_{amp} = 24\text{ V}$$

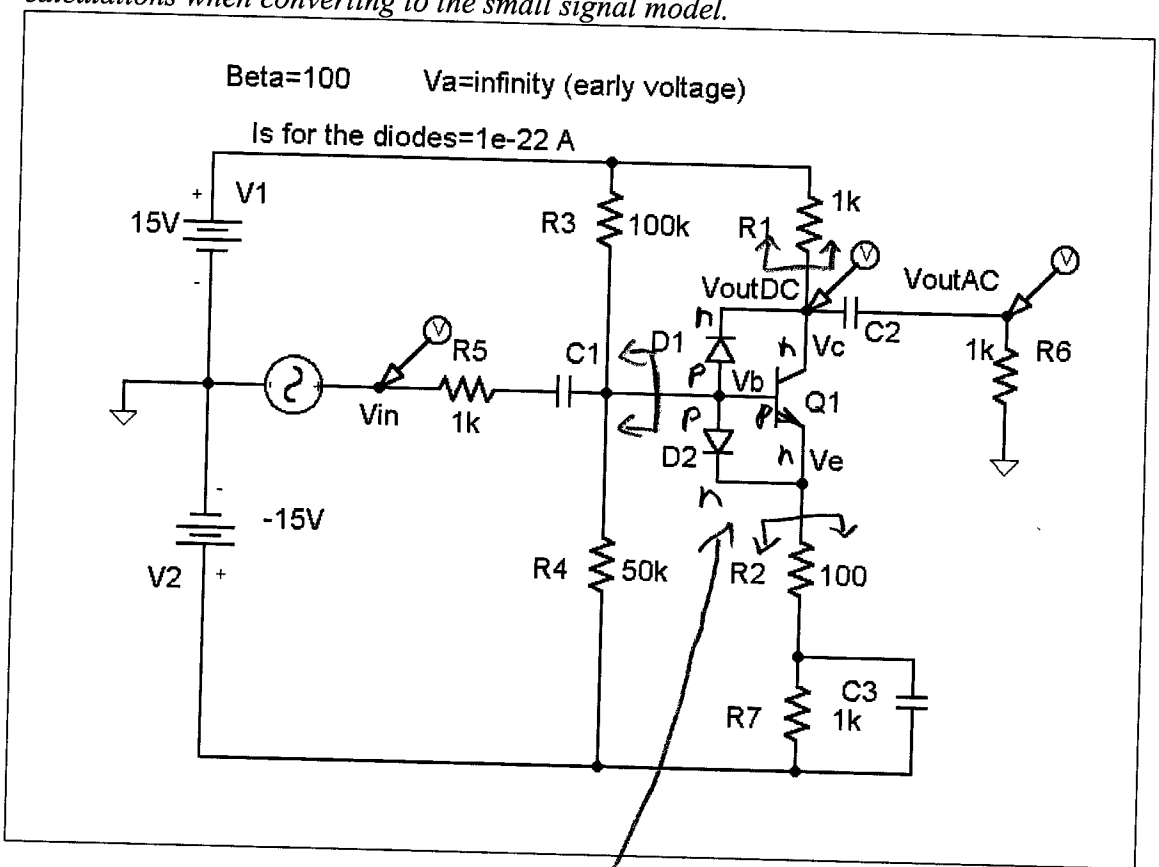
At the peak voltage, peak current will be drawn. Thus,

$$\frac{24\text{V} - 12\text{V}}{0.12\text{ A}} = R$$

$$R = 100\,\Omega$$

(4th Section - 40%) Pulling all the concepts together for a useful purpose:

8.) (40-points) Given the following amplifier circuit and BJT Parameters, what is the AC voltage gain, VoutAC/Vin? Assume: $\beta_{DC}$=100, Early voltage, $V_A$ is infinite, turn on voltages for all forward biased junctions are 0.7 V, the saturation current, $I_S = I_o$=1e-22A for D1 and D2. You may assume all capacitors are very large values and are thus, AC shorts. Additionally consider the circuit to be operated at low frequencies where you can neglect all small signal capacitances. Also, neglect all resistances that result from quasi-neutral regions. *Hints: Due to the very small $I_S$ of the diodes, the DC diode currents can be neglected in the calculation of the transistor bias condition. Use the CVD model for DC solutions. You may need to use the full mathematical diode model in part of your calculations when converting to the small signal model.*

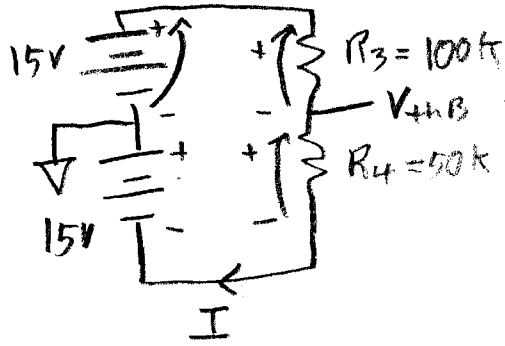



D.C. Solution: Noting that the p-n junctions of the diodes are aligned with the p-n junctions of the transistors, the diodes do not effect the DC solution. Thus we assume forward active mode.

(See next page)

Extra work can be done here, but clearly indicate with problem you are solving.

Thevenizing the base circuit to the left of D2.



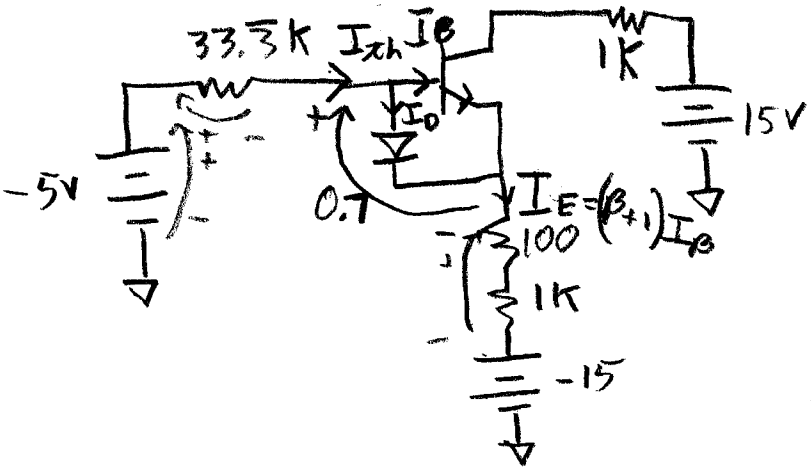

$15 - IR_3 - IR_4 + 15 = 0$

$I = \frac{30V}{R_3 + R_4} = \frac{30}{150k} = 0.2mA$

$V_{thB} = 15 - 100k\,I$

$= -5V$

$R_{thB} = 100k \,||\, 50k = 33.3k$




$I_{th} = I_B + I_D$

$\approx I_B$

You are told to Neglect $I_D$. Proof this works:

$I_D = 1e\text{-}22 \left(e^{0.7/0.0259} - 1\right)$

$= 5.5e\text{-}11\ A$

$-15V = +(-5V) - I_{th}(33.3k) - 0.7 - I_E(100+1k)$

$9.3 = I_B(33.3k + (\beta+1)(1.1k)$ (100)

$I_D < I_B$

5.5e-11 6.44e-5

$I_B = 64.4\,\mu A$

$I_C = 6.44mA$

$I_E = 6.5\,mA$

$V_E = -15 + I_E(1.1k) = -7.85\,V$

$V_B = V_E + 0.7 = -7.15\,V$

$V_C = 15V - I_C\,1k = 8.56\,V$

$V_B > V_E$ + $V_C > V_E$

Forward active + Diode assumptions verified.

Extra work can be done here, but clearly indicate with problem you are solving.

AC Solution:

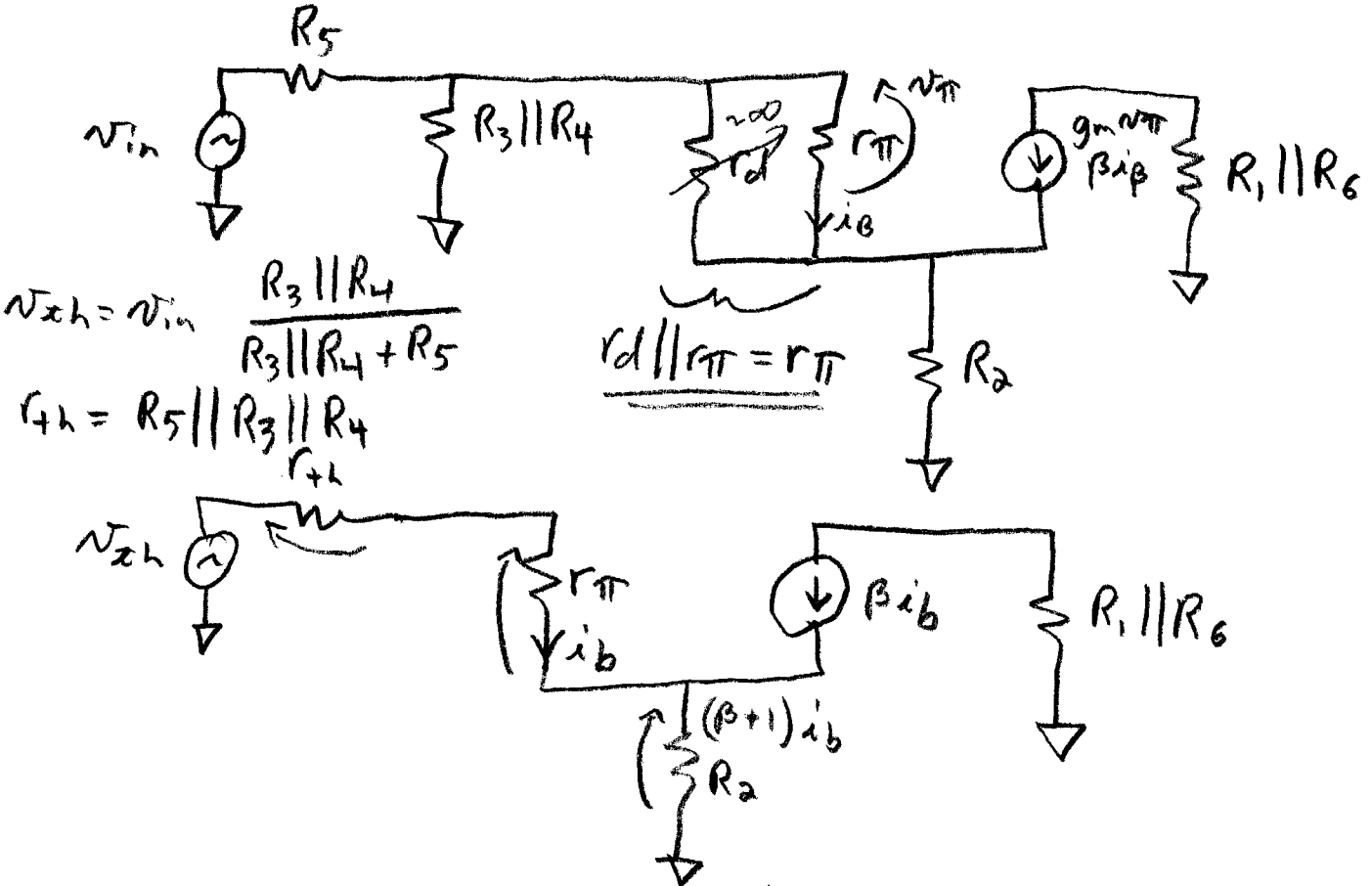
$$g_m = \frac{I_C}{V_T} = \frac{6.44\,mA}{0.0259} = 0.2486$$

$$r_o = \frac{V_A + V_{CE}}{I_C} = \frac{\infty + \ldots}{\ldots} = \infty$$

$$r_\pi = \frac{\beta}{g_m} = 402\ \Omega$$ see last page

$$r_d = \left(\frac{I_D + I_S}{V_T}\right)^{-1} = \left(\frac{5.4e\text{-}11 + 1e\text{-}22}{0.0259}\right)^{-1}$$

$$= 4.7e8\ \Omega \text{ (huge!)}$$




$$v_{th} = i_b(r_\pi + r_{th}) + (\beta+1) i_b R_2$$

$$\frac{v_{th}}{i_b} = r_\pi + r_{th} + (\beta+1) R_2$$

Extra work can be done here, but clearly indicate with problem you are solving.

$$v_{out} = -\beta i_b (R_1 \| R_6)$$

$$\frac{v_{out}}{i_b} = -\beta (R_1 \| R_6)$$

$$\frac{v_{out}}{v_{in}} = \left(\frac{v_{out}}{i_b}\right)\left(\frac{i_b}{v_{th}}\right)\left(\frac{v_{th}}{v_{in}}\right)$$

$0.035\ S$

$$= \left[-\beta (R_1 \| R_3)\right]\left[\frac{1}{r_\pi + R_5 \| R_4 \| R_3 + (\beta+1) R_2}\right] \cdots$$

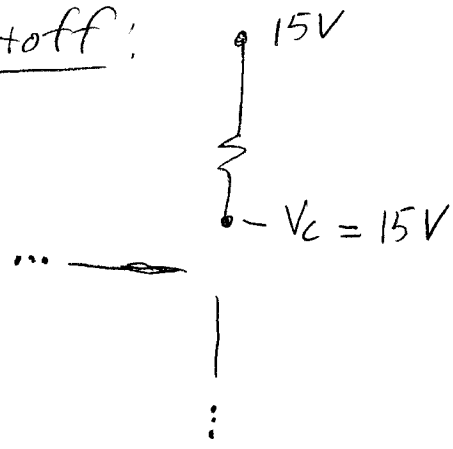
$-124.3\ \Omega$ ... $\left[\frac{R_3 \| R_4}{R_3 \| R_4 + R_5}\right]$

$0.97$ unitless

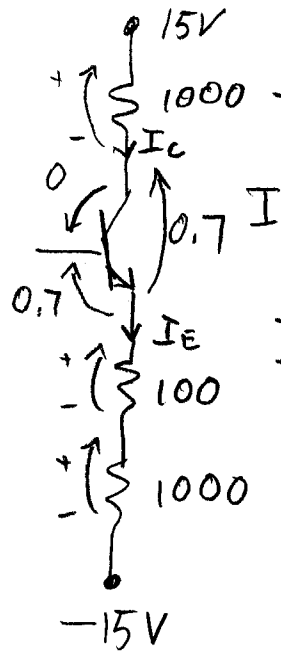
$$\boxed{A_v = \frac{v_{out}}{v_{in}} = -4.2\ V/V}$$

Bonus (10 points): In problem 8, if the diodes are removed, what is the maximum amplitude of a voltage sine wave at the collector that can be generated without distortion.

Onset of Cutoff:




Onset of Saturation:




$15 - 1000 I_C - 0.7 - 101000 I_E = 0$

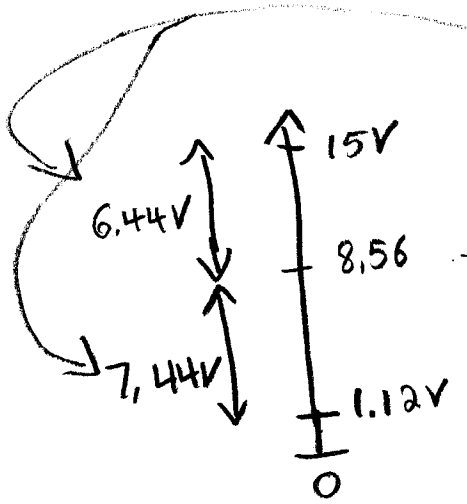
$I_C = \frac{29.3}{1000 + (100+1000)\left(\frac{\beta+1}{\beta}\right)}$

$I_C = 13.8\ mA$

Not valid in saturation but valid for forward active + $V_{CB} = 0\ V$ (onset of Sat)

$V_C = 15 - I_C(1000)$

$= 1.12\ V$




Max Amplitude would be smaller of the (2)

Thus, max. amp. without distortion = 6.44 V