ECE 3040B Microelectronic Circuits

Exam 3

July 24, 2001

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Print your name clearly and largely: Solution

Instructions:
Read all the problems carefully and thoroughly before you begin working. You are allowed to use 1 new sheet of notes (1 page front and back), your note sheets from the previous exams as well as a calculator. There are 100 total points in this exam. Observe the point value of each problem and allocate your time accordingly. SHOW ALL WORK AND CIRCLE YOUR FINAL ANSWER WITH THE PROPER UNITS INDICATED. Write legibly. If I cannot read it, it will be considered a wrong answer. Do all work on the paper provided. Turn in all scratch paper, even if it did not lead to an answer. Report any and all ethics violations to the instructor. Good luck!

Sign your name on **ONE** of the two following cases:

I DID NOT observe any ethical violations during this exam:

I observed an ethical violation during this exam:

***First 25%* Multiple Choice and True/False (Select the most correct answer)**

1.) (2-points) A MOS Transistor can be:
   a.) An enhancement mode NMOS device
   b.) A depletion mode PMOS device
   c.) An enhancement mode PMOS device
   d.) A depletion mode NMOS device
   e.) All of the above

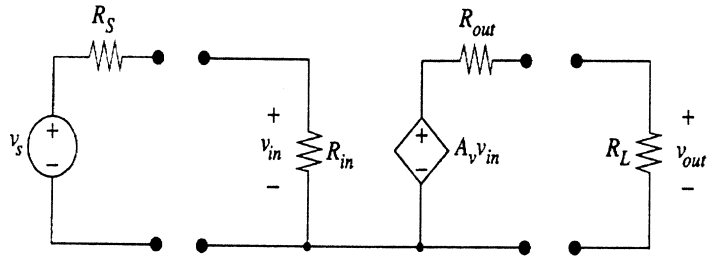
2.) (2-points) Depletion mode MOS transistors have large DC gate currents but enhancement mode MOS transistors have no DC gate current.
   a.) True
   b.) False
   c.) I am totally confused on this question

3.) (3-points) True (False) A "real world" (Non-ideal) Op-Amp has infinite open loop gain.

Error Corrected at the start of Class

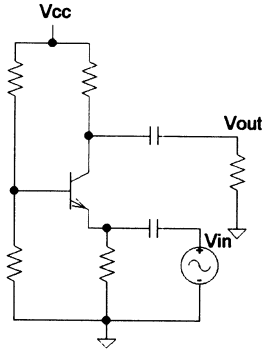
4.) (3-points) The following condition defines the triode or linear region of operation of a NMOS Enhancement mode transistor.
   a.) $V_{GS}<V_T$ and $V_{DS}<V_{GS}$ $- V_T$
   b.) $V_{GS}>V_T$ and $V_{DS}<V_{GS}$ $- V_T$
   c.) $V_{GS}>V_T$ and $V_{DS}>V_{GS}$ $- V_T$
   d.) All of the above
   e.) I would much preferred you not asking this question.

5.) (3-points / 1 point each) For the following amplifier:
   a.) Is this a : (Voltage,) Current, Transconductance, or Transresistance Amplifier
   b.) Should this amplifier have an (High) or Low input impedance for maximum voltage gain?
   c.) Should this amplifier have an High or (Low) output impedance for maximum voltage gain?

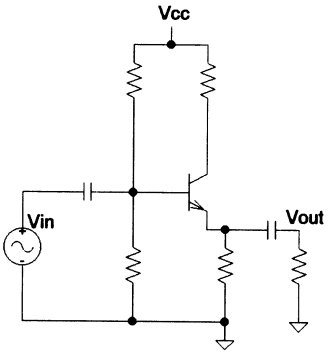


6.) (12 points total: 2-points each)

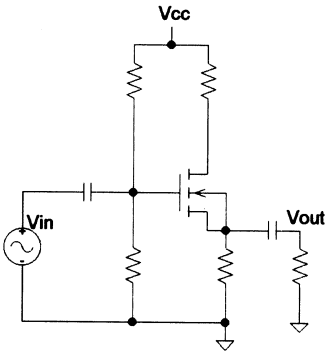
For each of the following circuits, identify the transistor configuration as Common _____.



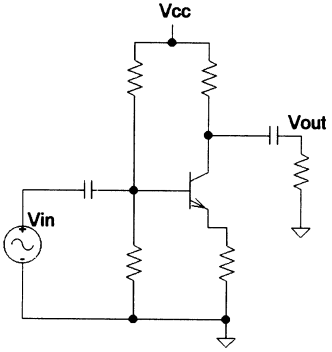
Common Base



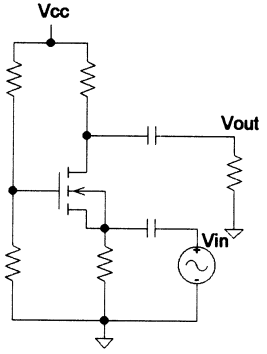
Common collector



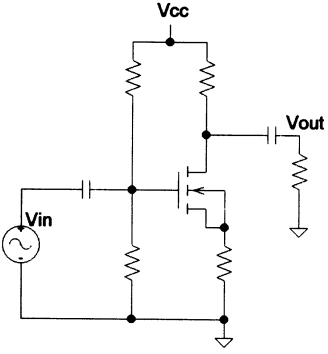
Common Drain



Common emitter



Common Gate



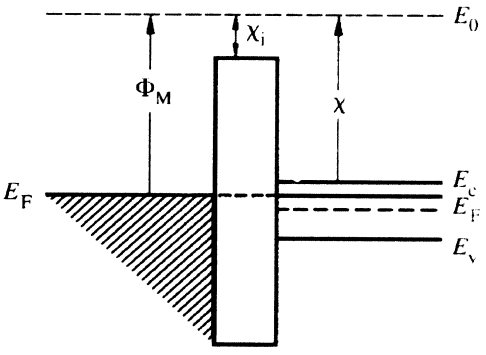
Common Source

Second 25% Short Answer:

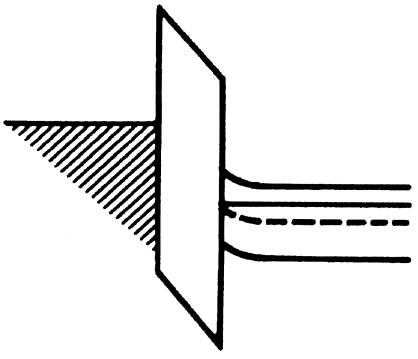
7.) (25-points) Draw and label the energy band diagram of a PMOS Enhancement mode Capacitor in equilibrium, depletion and deep inversion (3 drawings) labeling the fermi, intrinsic, conduction and valence energies.

The intrinsic energy is the dashed line.

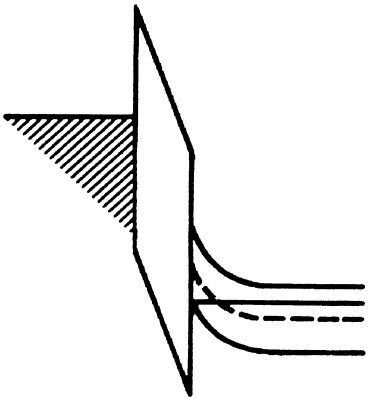
Equilibrium



Depletion (see above labels)



Deep Inversion (see above labels): Note the inverted layer is now p-type, thus the PMOS designation.

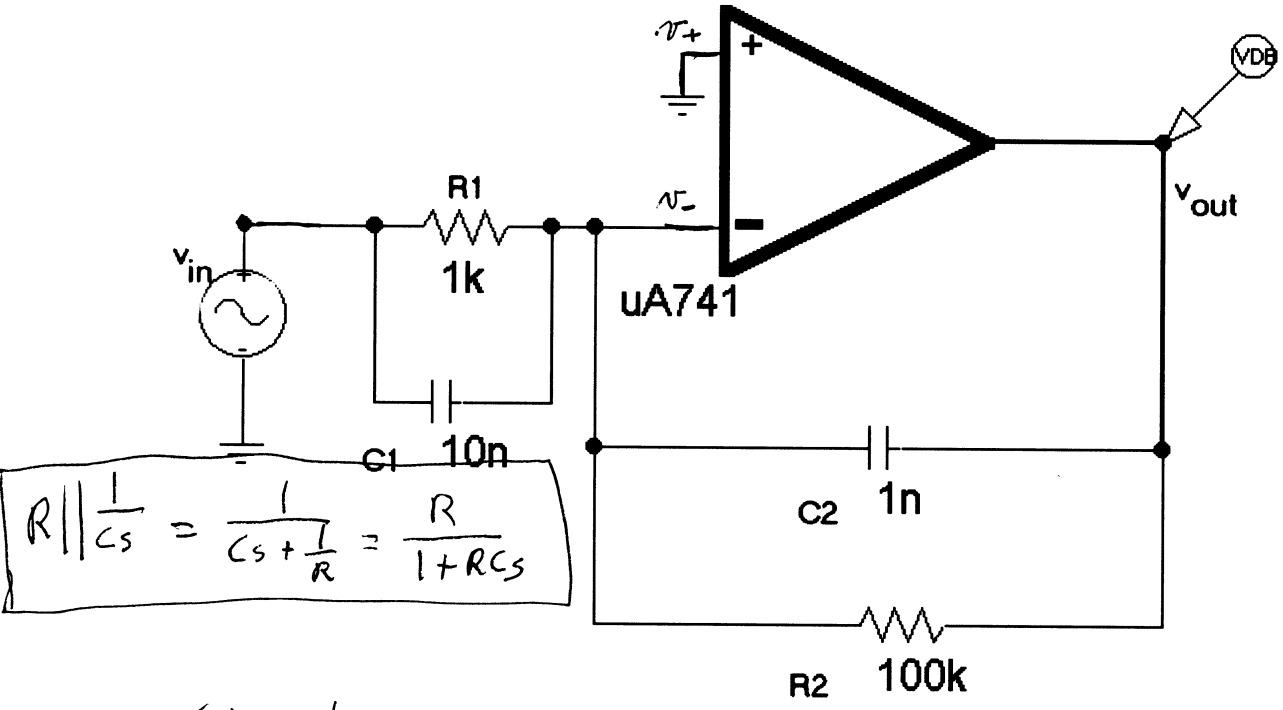


Third 25% Problems (3rd 25%)

8.) (a. 15-points) Plot the voltage gain transfer function (Voltage gain in dB vs. Log(frequency)), v_{out}/v_{in} of the following circuit from 1Hz to 10MegHz showing the break frequencies and low and high frequency gains in dB.

(b. 10-points) Determine the input resistance and output resistance of the following circuit.

Hints for both parts: Treat the parallel resistor/capacitor combination as one impedance. If you do so, you can write the gain expression directly from the configurations we derived in class. Once you do this, you can simplify the transfer function into the standard form, from which the poles and zeros can be extracted. You may assume that the Op-Amps are ideal.



$$R \| \frac{1}{Cs} = \frac{1}{Cs + \frac{1}{R}} = \frac{R}{1+RCs}$$

Similar to inverting configuration:

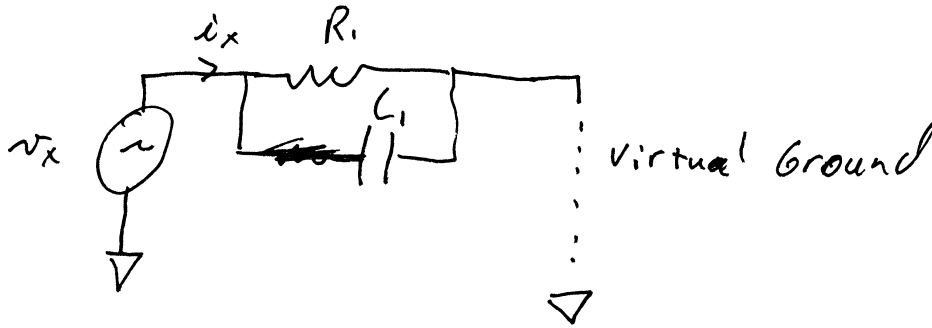
$$A_V = \frac{v_{out}}{v_{in}} = -\frac{R_2}{R_1} \Rightarrow -\frac{R_2 \| \frac{1}{C_2 s}}{R_1 \| \frac{1}{C_1 s}}$$

$$= -\frac{\frac{R_2}{1+R_2 C_2 s}}{\frac{R_1}{1+R_1 C_1 s}} = \boxed{-\frac{R_2}{R_1}\left(\frac{1+R_1 C_1 s}{1+R_2 C_2 s}\right) V/V}$$

$$= -100\left(\frac{1+\frac{s}{1e5(rad)}}{1+\frac{s}{1e4\,rad}}\right)$$

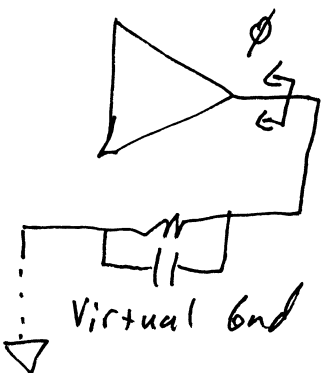
Input Impedance:

Due to the virtual ground at the v_- terminal,



$$R_{in} = \frac{v_x}{i_x} = R_1 \| \frac{1}{C_1 s}$$

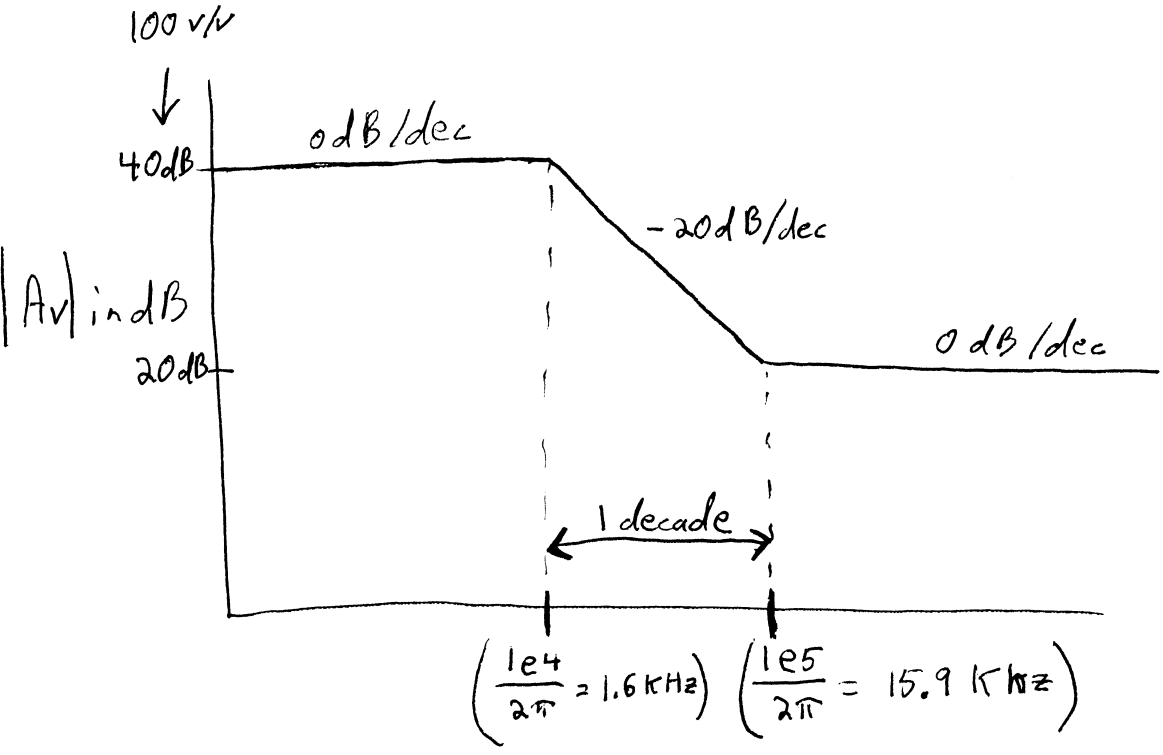
Output Impedance:



$$R_{out} = \phi \| R_2 \| \frac{1}{C_2 s}$$

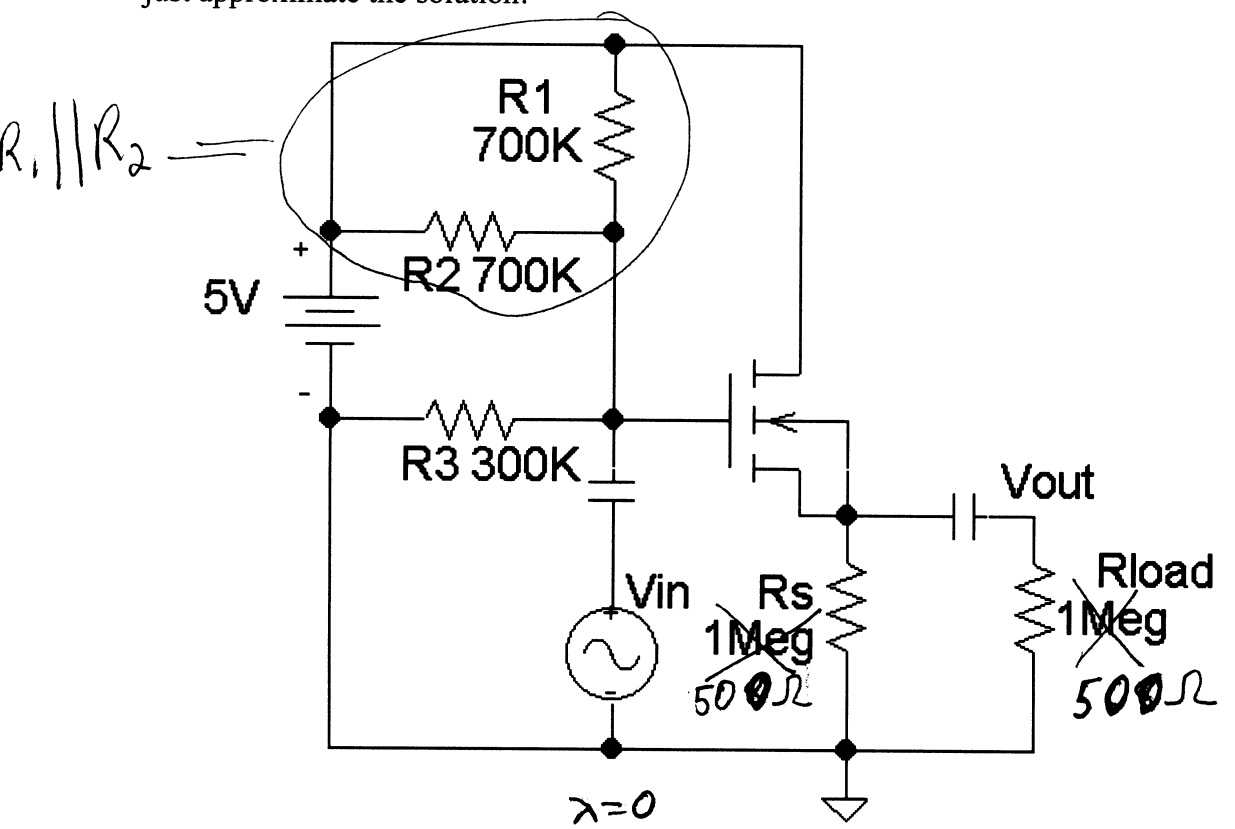
$$R_{out} = \phi$$

Extra work can be done here, but clearly indicate with problem you are solving.



Pulling all the concepts together for a useful purpose: (4^{th} 25%)

9.) (25-points) Given the following circuit, what is the AC voltage gain, V_{out}/V_{in}? You may assume all capacitors have infinite capacitance and are thus, AC shorts. Additionally consider the circuit to be operated at low frequencies where you can neglect all small signal capacitances. Grading will be based as such: 10 points for DC solution, 15 points for small signal conversion/small signal analysis. Work out the answer. Do not just approximate the solution!



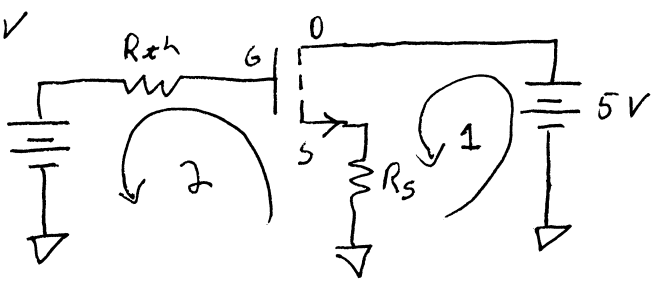
$R_1 || R_2$ =

K_n'=250 uA/V^2 V_T=1V ~~λ=0.1 V^{-1}~~ Length (L)=10 um Width (W)=1000 um

D.C. Solution: $R_1 || R_2 = 350K$

$$V_{th} = \frac{R_3 (5V)}{R_1 || R_2 + R_3} = 2.308V$$

$R_{th} = R_1 || R_2 || R_3 = 161.5 K\Omega$



$K_n = 250e\text{-}6 \frac{1000um}{10um} = 0.025\ A/V^2$

Assume Saturation:

$$I_{DS} = \frac{K_n}{2}(V_{GS} - V_{TN})^2(1 + \lambda V_{DS})$$ ($\lambda V_{DS} \to 0$)

(Loop 2) $V_{GS} = V_{th} - I_{DS} R_S$

Extra work can be done here, but clearly indicate with problem you are solving.

(Loop 1) $5V - V_{DS} - I_{DS} R_S = 0$

$* V_{DS} = 5V - I_{DS} R_S$

$$I_{DS} = \frac{0.025}{2}\left((2.308-1) - 500 I_{DS}\right)^2$$

$$= 0.0125\left((1.308)^2 - 1308 I_{DS} + 250{,}000 I_{DS}^2\right)$$

$$= \cancel{0.01635}\ 0.02138 - 16.35 I_{DS} + 3125 I_{DS}^2$$

$$3125 I_{DS}^2 - 17.35 I_{DS} + \cancel{0.01635}\ 0.02138 = 0$$

$$I_{DS} = \frac{17.35 \pm \sqrt{(17.35)^2 - 4(3125)(\cancel{0.01635}\ 0.02138)}}{2(3125)}$$

$I_{DS} = \cancel{0.0012\,A}\ 1.85\,mA$ $\quad * V_{DS} = 5 - \cancel{0.0012}\ 0.00185(500)$

$= \cancel{\text{[illegible]}}\ 4.076\,V$

or $\cancel{0.00435\,A}\ 3.7\,mA$ $\quad * V_{DS} = 5 - \cancel{0.00435}\ 0.0037(500)$

$= \cancel{2.825\,V}$

$3.15\,V$

$$V_{GS} = 2.308 - I_{DS}(500)$$

$$V_{GS} = 1.383\Big|_{I_{DS} = 1.85mA}$$

or

$$0.458\Big|_{I_{DS} = 3.7mA} V \quad < V_{TN} = 1$$

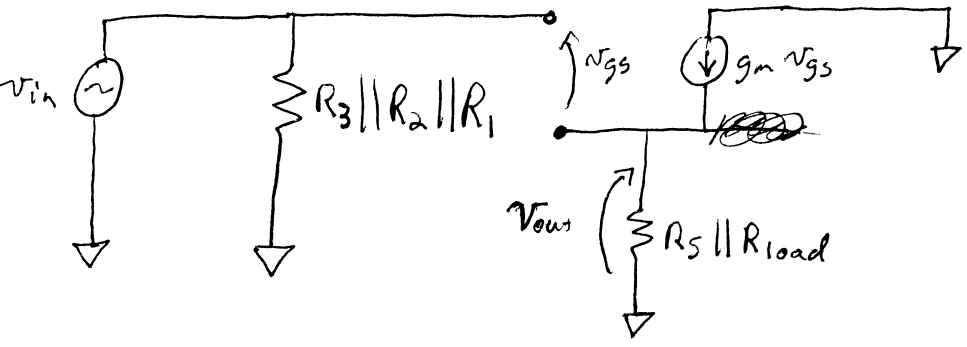
for saturation,

use $V_{GS} = 1.383$, $V_{DS} = 4.076$, $I_{DS} = 1.85mA$

Extra work can be done here, but clearly indicate with problem you are solving.

$$g_m = \frac{I_{DS}}{\frac{V_{GS} - V_{TN}}{2}} = \frac{1.85mA}{\frac{1.383 - 1}{2}} = 0.00966 \ S$$

$$r_o = \left[\frac{I_{DS}}{\frac{1}{\lambda} + V_{DS}}\right]^{-1} = \left[\frac{1.85e-3}{\frac{1}{0} + 4.076}\right]^{-1} = \infty$$



1) $v_{out} = g_m v_{gs} (R_S || R_{load})$

2.) $v_{in} = v_{gs} + v_{out}$

Using (1) in (2)

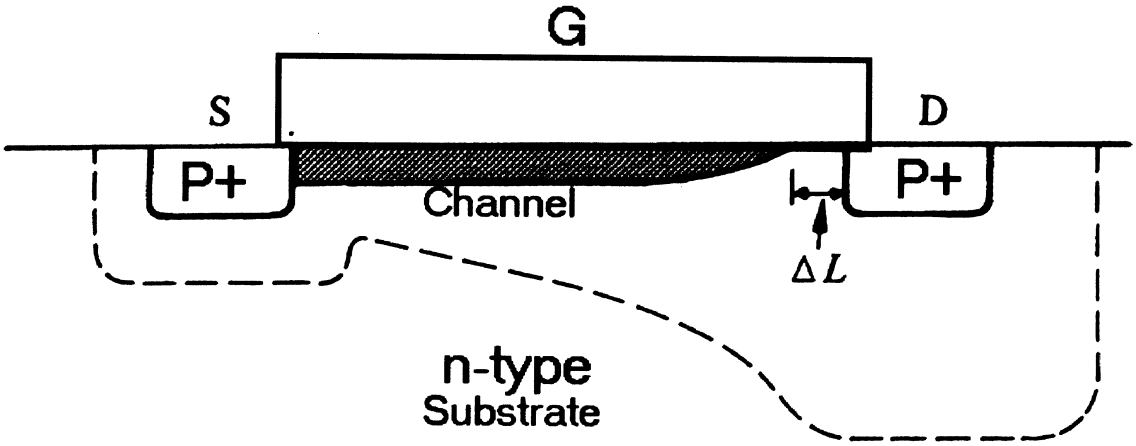
$$v_{in} = \frac{v_{out}}{g_m (R_S || R_{Load})} + v_{out}$$

$$v_{in} = v_{out} \left(\frac{1}{g_m (R_S || R_{Load})} + \frac{g_m (R_S || R_{Load})}{g_m (R_S || R_{Load})} \right)$$

$$\frac{v_{out}}{v_{in}} = \frac{g_m (R_S || R_{Load})}{1 + g_m (R_S || R_{Load})}$$

$$\boxed{\frac{v_{out}}{v_{in}} = 0.707 \ V/V}$$

Bonus: (10-points "All or Nothing") Draw the cross-sectional view (view from the side) of a PMOS transistor biased in saturation mode. Label the source, gate, drain, channel, substrate and indicate the doping type of the source, drain and substrate. Also, indicate the relationship between V_{SG} and V_{SD} for which saturation is maintained.



$V_{SD} > V_{SG} + V_{TP}$ (>0)