ECE 3040B Microelectronic Circuits

Exam 3

April 12, 2001

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Solutions

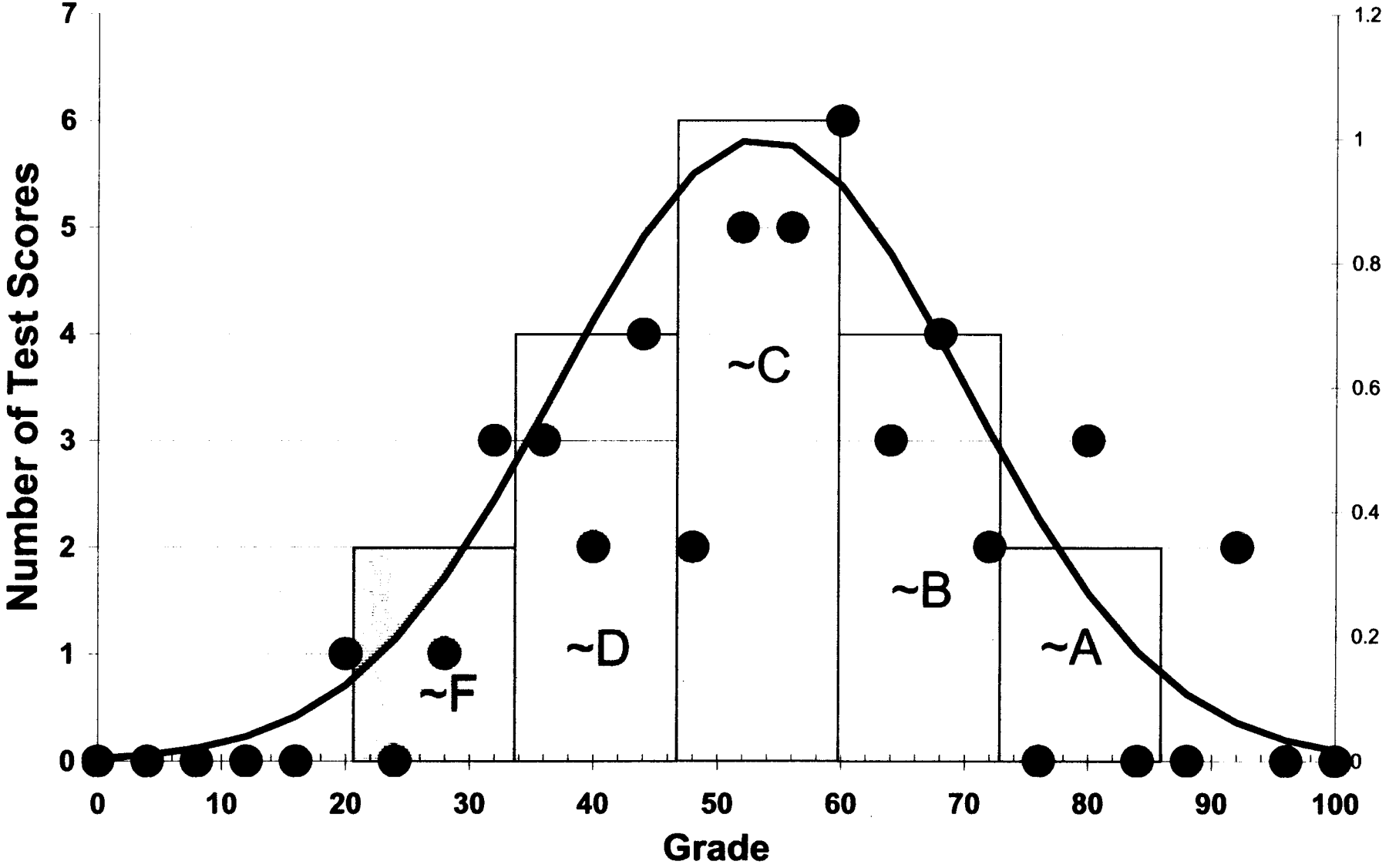
Print your name clearly and largely:

Test Average	53.52174
Test Standard Deviation	16.32413

Broken down by question

Question	1	2	3	4	5	6	7	8	9	10	11	12
% Score per Question	100	71.7	73.9	56.5	68.1	71	60.9	72.6	65.1	38.7	46.7	28.5

1st 25%	62.81159
2nd 25%	65.94203
3rd 25%	68.84058
4th 25%	28.52174


Number of Test Scores
Grade
~F
~D
~C
~B
~A
0
1
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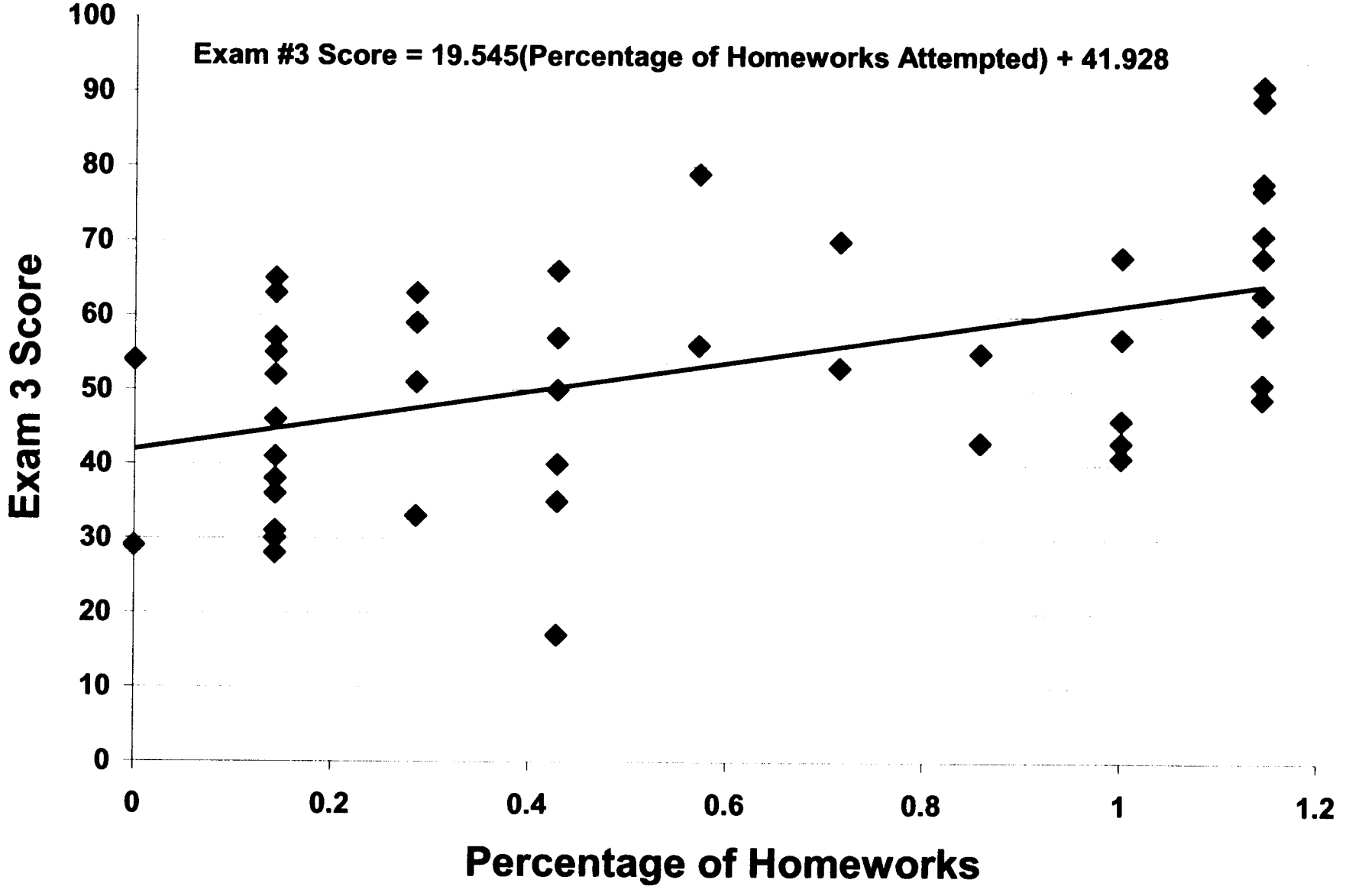
1
1.2


Exam #3 Score = 19.545(Percentage of Homeworks Attempted) + 41.928
Exam 3 Score
100
90
80
70
60
50
40
30
20
10
0
0
0.2
0.4
0.6
0.8
1
1.2
Percentage of Homeworks

***First 25%* Multiple Choice and True/False (Select the most correct answer)**

1.) (5-points) A MOS Capacitor consists of three regions:
   a.) Metal, semiconductor and metal regions
   b.) Metal, semiconductor and plastic
   c.) Metal, Oxide, and Semiconductor
   d.) Wood, cement and gravel.

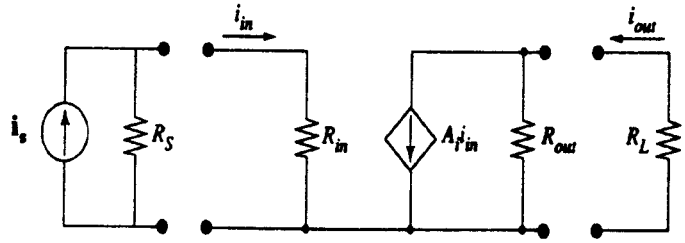
2.) (5-points) MOSFETs always need a non-zero Gate to Source Voltage to conduct a Drain-Source current (remember to consider PMOS and NMOS enhancement and depletion devices).
   a.) True
   b.) False
   c.) I am totally confused on this question

3.) (3-points) True / False Feedback always has to be negative otherwise the circuit will not work (think about this one carefully).

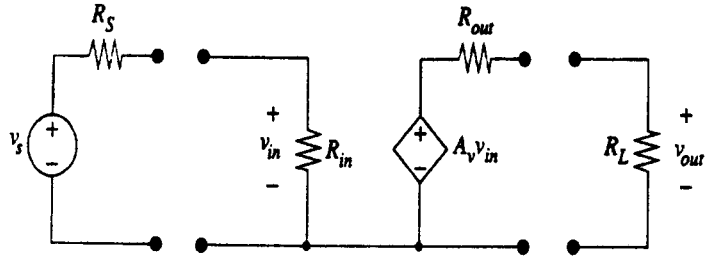
4.) (3-points) True / False The body terminal of a MOSFET should always be connected to ground, regardless of whether the device is PMOS or NMOS.

For each of the following amplifiers, identify the configuration (voltage, current, transconductance, transresistance), and whether you want to have a high or low input and output resistance. Circle your answer.

5.) (3-points)
a.) Voltage, Current, Transconductance, or Transresistance
b.) Input Impedance should be High / Low
c.) Output Impedance should be High / Low



6.) (3-points)
d.) Voltage, Current, Transconductance, or Transresistance
e.) Input Impedance should be High / Low
f.) Output Impedance should be High / Low

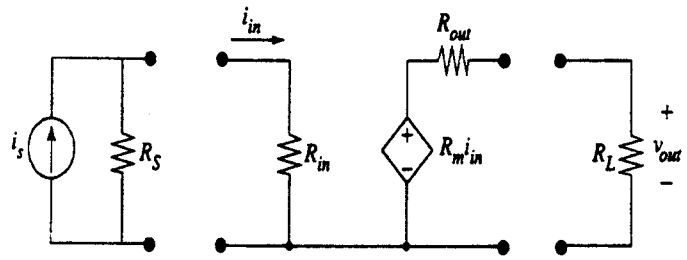


7.) (3-points)

g.) Voltage, Current, Transconductance or Transresistance

h.) Input Impedance should be High / Low

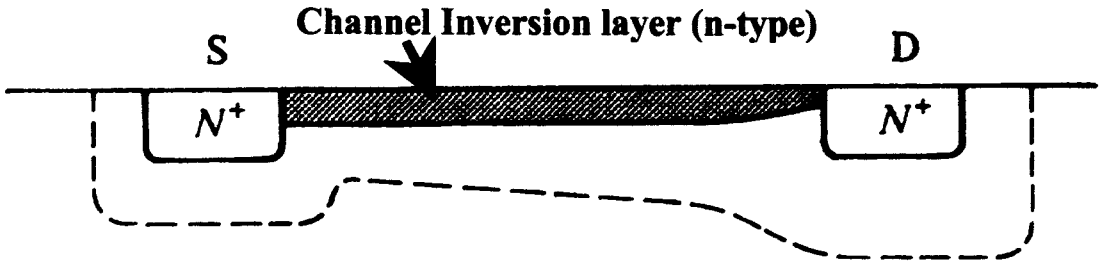
i.) Output Impedance should be High / Low



Second 25% Short Answer:

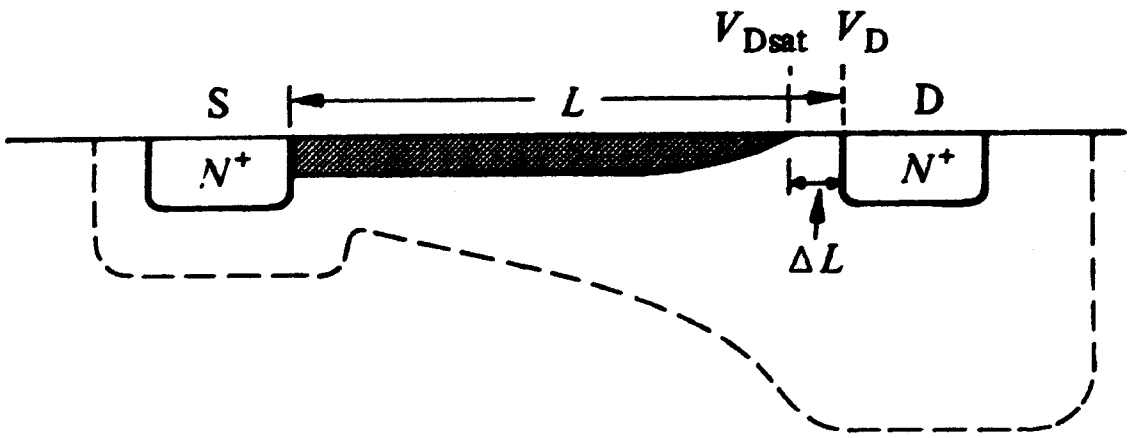
8.) (10-points) Draw the cross-sectional view (view from the side) of a NMOS transistor biased in linear and in saturation modes (two separate drawings). Label the source, gate, drain, channel, substrate and indicate the doping type of the source, drain and substrate.

Linear:

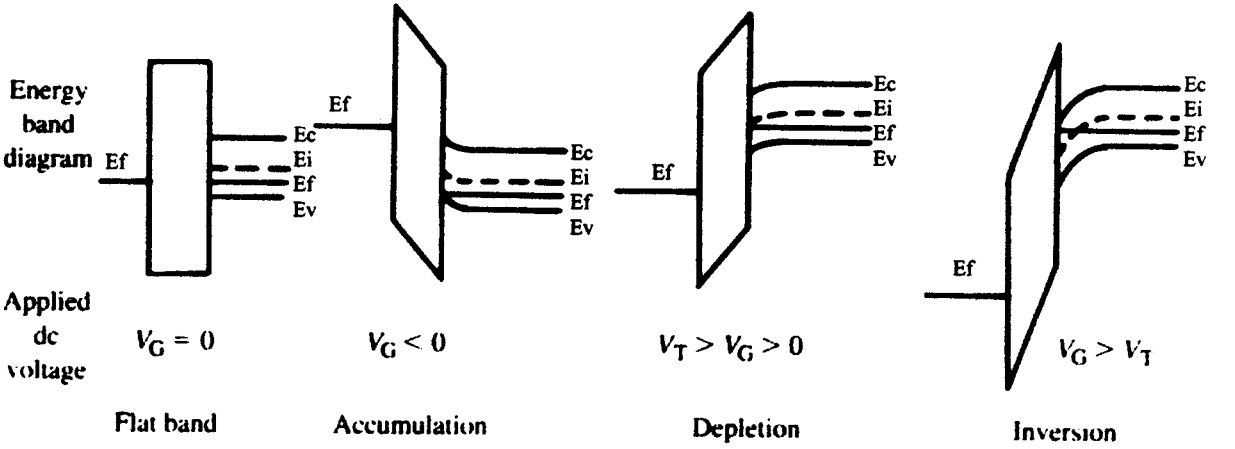


P-type Substrate

Saturation:

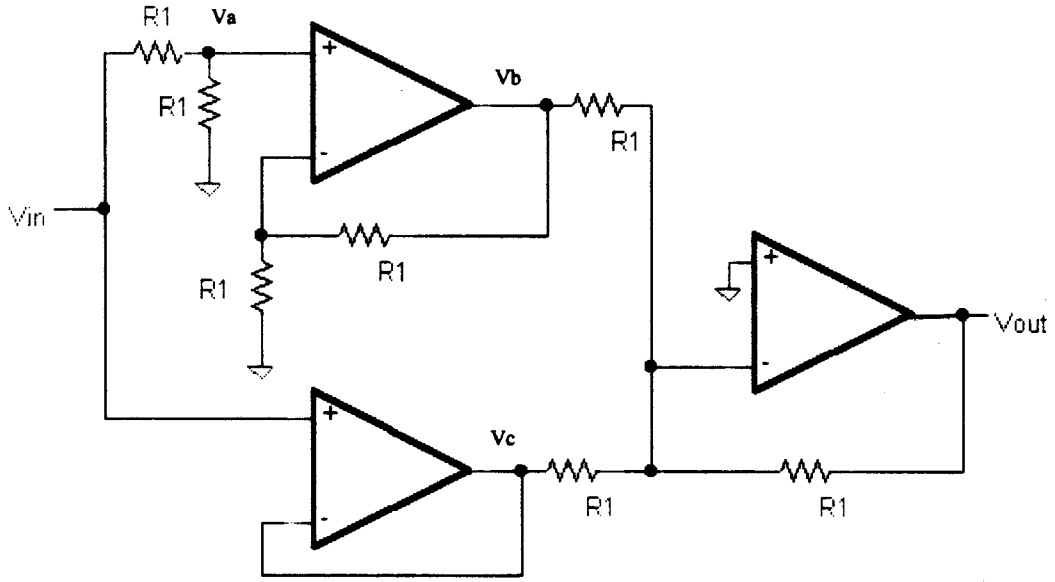


9.) (15-points) Draw and label the energy band diagram of a NMOS Enhancement mode Capacitor in equilibrium, depletion and deep inversion (3 drawings) labeling the fermi, intrinsic, conduction and valence energies.
All regions are shown below (including accumulation, which was not asked for). In each picture, the left most material is the metal, then the oxide, with the rightmost material being the semiconductor.



Third 25% Problems (3rd 25%)

10.) (10-points) Determine the voltage gain, input resistance and output resistance of the following circuit. You may assume that the Op-Amps are ideal.



$$Va = Vin\frac{R1}{R1+R2} = 0.5Vin$$

$$Vb = \left(1+\frac{R1}{R1}\right)Va = 2Va$$

$$Vc = Vin$$

$$Vout = -\frac{R1}{R1}Vb - \frac{R1}{R1}Vc$$

$$Vout = -2Va - Vin$$

$$Vout = -Vin - Vin$$

$$\frac{Vout}{Vin} = -2 \quad V/V$$

$R_{in} = 2R1$

$R_{out} = 0 \quad [V_{in} = 0 \Rightarrow V_b = V_c = 0]$

11.) (15-points total in two parts) **(a) (12-points)** As an integrated circuit designer, you are asked to determine the width (W in Jaeger, Z in Pierret) of a MOSFET gate required to achieve a small signal transconductance of 0.01 A/V when used in a circuit that will have a Source-to-Gate voltage, V_{GS}=1.5V, a Source-to-Drain voltage, V_{DS}=5V, and a Source-to-Body voltage, V_{BS}=0.0V. **(b) (3-points)** What is the drain-source current in this application? The fabrication process you are using has the following parameters:

Gate Length, L=1 μm
Effective mobility, $\overline{\mu_n}$=200 cm^2/VSec
Oxide Thickness, t_{ox}= x_{ox} =200nm
Channel Length Modulation parameter, λ=0.1 V^{-1}
Substrate Doping, N_A=1e15 cm^{-3}
Oxide relative Dielectric Constant, $\varepsilon_{r\text{-}oxide}=K_O=3.9$
Substrate relative Dielectric Constant, $\varepsilon_{r\text{-}semiconductor}=K_S=11.7$
Substrate intrinsic concentration, n_i=1e10 cm^{-3}
Dielectric Constant of free space, ε_O =8.854e-14 F/cm

$$0.01 = g_m = K_n (V_{GS} - V_{TN})(1 + \lambda V_{DS})$$

$$* \quad g_m = \frac{I_{DS}}{\frac{(V_{GS} - V_{TN})}{2}} = 0.01$$

$$K_n = \frac{Z}{L} \overline{\mu_n} C_{ox} \qquad C_{ox} = \frac{\epsilon_{ox}}{x_{ox}} = 1.726\text{e-}8 \text{ F/cm}$$

We need V_{TN}: Since $V_{BS} = 0$ and NMOS (N_A not N_D given)

$$V_{TN} = 2\phi_F + \frac{K_S \epsilon_O}{C_{ox}} \sqrt{\frac{2 q N_A}{\epsilon_S} (2\phi_F)}$$

$$\phi_F = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right)$$

$$= 0.0259 \ln\left(\frac{1e15}{1e10}\right) = 0.298 \text{ V}$$

$$\Rightarrow V_{TN} = 2(0.298) + \frac{(11.7)\,8.854\text{e-}14}{1.726\text{e-}8} \sqrt{\frac{2\,(1.6\text{e-}19)\,1e15}{(11.7)\,8.854\text{e-}14}(2)0.298}$$

$$= 0.596 + 0.814$$

$$V_{TN} = 1.41 \text{ V}$$

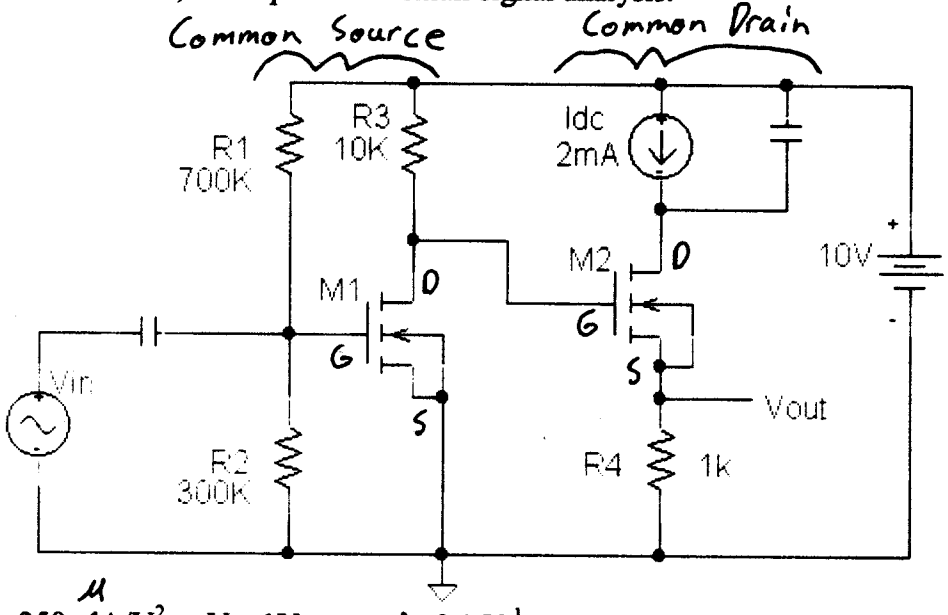
$$\Rightarrow 0.01 = \left[\frac{Z}{(1e\text{-}4)}(200)\,1.726\text{e-}8\right](1.5 - 1.41)(1 + 0.1(5))$$

$$\Rightarrow a) \boxed{Z = 2.15 \text{ cm}}$$ It takes a huge device to meet this design requirement

b) from * $\boxed{I_{DS} = 448\ \mu A}$

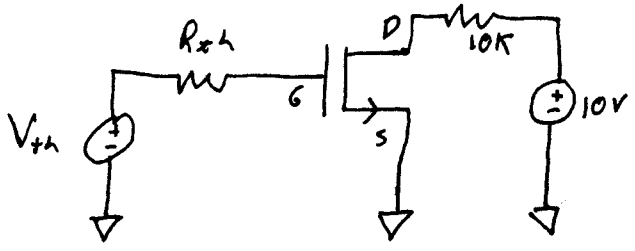
Pulling all the concepts together for a useful purpose: (4^{th} 25%)

12.) (25-points) Given the following circuit, (a) Identify the configuation of all stages in the amplifier. (b) What is the AC voltage gain, V_{out}/V_{in}? You may assume all capacitors have infinite capacitance and are thus, AC shorts. Additionally consider the circuit to be operated at low frequencies where you can neglect all small signal capacitances. Grading will be based as such: 4 points for configuration identification, 8 points for DC solution, 4 points for small signal conversion, and 9 points for small signal analysis.



K_n=250 μA/V² V_T=1V λ=0.1 V⁻¹

DC: M1: Taking a Thevenin in the Gate circuit.



$V_{th} = \frac{300K}{700K+300K} 10V = 3V$

$R_{th} = 300K \| 700K = 210K$

Note: $V_{th} = V_{GS_1}$: $V_{DS_1} = 10V - I_{DS_1}(10K)$

Now Assume Saturation:

$$I_{DS_1} = \frac{K_n}{2}(V_{GS_1} - V_{TN})^2(1 + \lambda V_{DS_1})$$

$$I_{DS_1} = 125(\mu A/V^2)(3-1)^2(1 + 0.1[10V - I_{DS_1}10K])$$

$$I_{DS_1} = 500e\text{-}6\,(1 + 1 - I_{DS_1}(1K))$$

$$I_{DS_1}(1+0.5) = 1mA$$

$$I_{DS_1} = 666\,\mu A$$

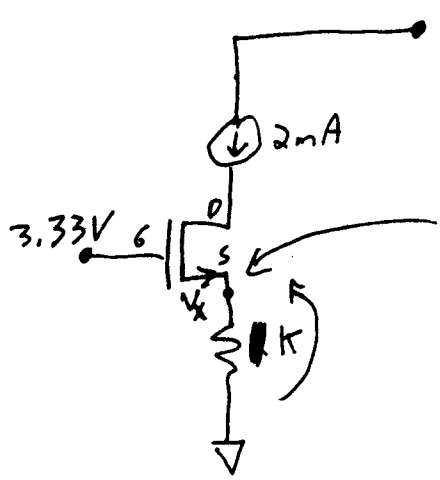
Extra work can be done here, but clearly indicate with problem you are solving.

$V_{DS_1} = 10 - 666\,\mu A\,(10k)$

$= 3.33\,V \overset{?}{>} V_{GS} - V_T = 3 - 1 = 2$ ✓

Assumption of saturation is valid.

DC M2: Since the DC current source insures a constant current, M2 must be in saturation.



$I_{DS_2} = 2\,mA$

$V_x = 2\,mA(1k) = 2V$

$V_{GS_2} = 3.33V - 2V$

$= 1.33\,V$

$$g_{m_1} = \frac{I_{DS_1}}{\frac{V_{GS_1} - V_T}{2}} = \frac{666\,\mu A}{\frac{3-1}{2}} = 666\,\mu A/V = 6.66 \times 10^{-4}$$

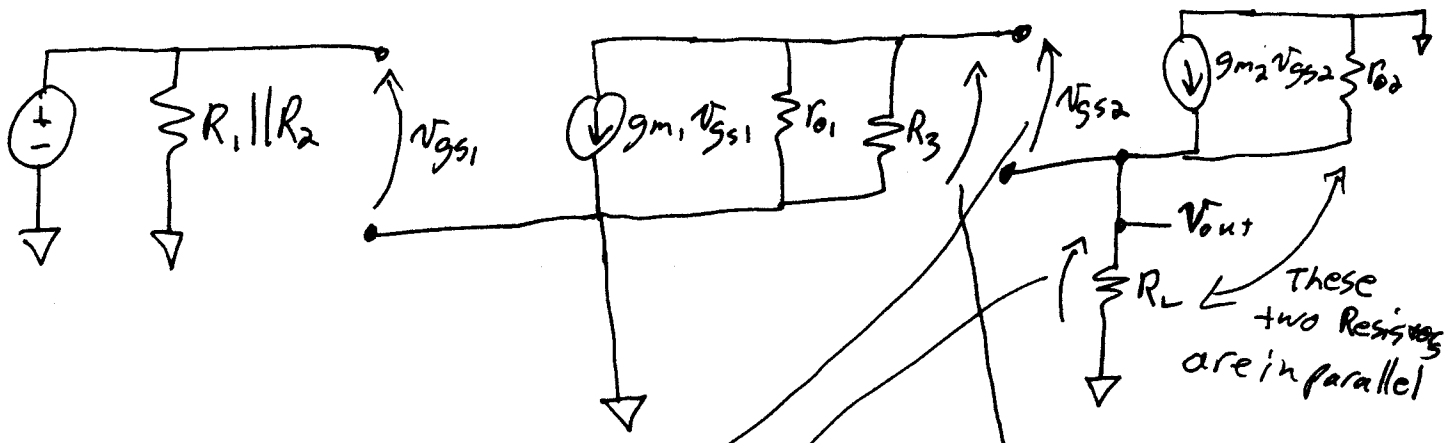
$$g_{m_2} = \frac{I_{DS_2}}{\frac{V_{GS_2} - V_T}{2}} = \frac{2\,mA}{\frac{1.33-1}{2}} = 0.012\ A/V$$

$$r_{o_1} = \frac{1}{\frac{\lambda K_n}{2}(V_{GS_1} - V_T)^2} = \frac{1}{\frac{0.1(250e\text{-}6)}{2}(3-1)^2} = 20\,k\Omega$$

$r_{o_2} = 720{,}000\ \Omega$

Extra work can be done here, but clearly indicate with problem you are solving.

AC Solution:



Step 1:

$$v_{in} = v_{gs1}$$

$$v_{gs2} + g_{m2} v_{gs2} \left(R_L || r_{o2}\right) = -g_{m1} v_{gs1} \left(r_{o1} || R_3\right)$$

$$v_{out} = g_{m2} v_{gs2} \left(R_L || r_{o2}\right)$$

$$\frac{v_{out}}{v_{in}} = \frac{v_{out}}{v_{gs2}} \frac{v_{gs2}}{v_{gs1}} \frac{v_{gs1}}{v_{in}}$$

$$= \left(g_{m2}\left(R_L || r_{o2}\right)\right)\left[\frac{-g_{m1} v_{gs1}\left(r_{o1} || R_3\right)}{1 + g_{m2}\left(R_L || r_{o2}\right)}\right] \quad (1)$$

$$\frac{v_{out}}{v_{in}} = \underbrace{-g_{m1}\left(R_3 || r_{o1}\right)}_{\text{Standard CS gain}} \underbrace{\frac{g_{m2}\left(R_L || r_{o2}\right)}{1 + g_{m2}\left(R_L || r_{o2}\right)}}_{\text{Standard CD gain}}$$

You could have written this down in step 1! Plugging in numbers,

$$\boxed{\frac{v_{out}}{v_{in}} = -4.1 \text{ V/V}}$$