

ECE 3040 Microelectronic Circuits

Exam 3

July 23, 2002

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Print your name clearly and largely:

Solutions

Instructions:

Read all the problems carefully and thoroughly before you begin working. You are allowed to use 1 new sheet of notes (1 page front and back), your note sheet from the previous exams as well as a calculator. There are 120 total points in this exam (100 points plus 20 bonus points). The exam will be graded on a 100-point basis. Observe the point value of each problem and allocate your time accordingly. **SHOW ALL WORK AND CIRCLE YOUR FINAL ANSWER WITH THE PROPER UNITS INDICATED.** Write legibly. If I cannot read it, it will be considered a wrong answer. Do all work on the paper provided. Turn in all scratch paper, even if it did not lead to an answer. Report any and all ethics violations to the instructor. Good luck!

Sign your name on ONE of the two following cases:

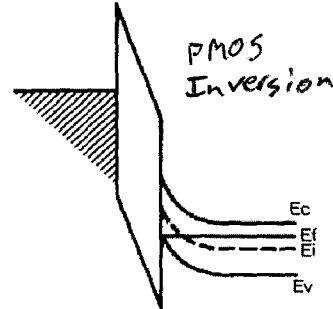
I DID NOT observe any ethical violations during this exam:

I observed an ethical violation during this exam:

First 20% Multiple Choice and True/False (Select the most correct answer)

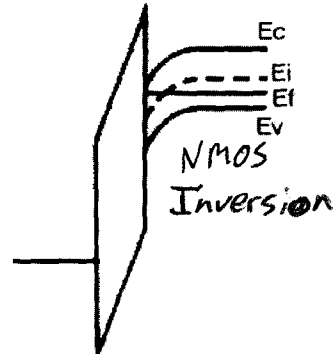
1.) (4-points) If the MOS capacitor shown in the diagram to the right were used in a MOSFET transistor, which of the following COULD result (more than one answer possible):

- a.) NMOS transistor biased into Cutoff mode
- b.) PMOS transistor biased into Cutoff mode
- c.) NMOS transistor biased into linear/triode mode
- d.) PMOS transistor biased into linear/triode mode
- e.) NMOS transistor biased into Saturation mode
- f.) PMOS transistor biased into Saturation mode



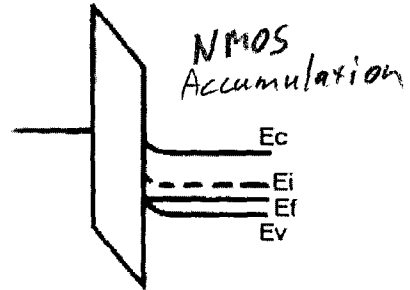
2.) (4-points) If the MOS capacitor shown in the diagram to the right were used in a MOSFET transistor, which of the following COULD result (more than one answer possible):

- a.) NMOS transistor biased into Cutoff mode
- b.) PMOS transistor biased into Cutoff mode
- c.) NMOS transistor biased into linear/triode mode
- d.) PMOS transistor biased into linear/triode mode
- e.) NMOS transistor biased into Saturation mode
- f.) PMOS transistor biased into Saturation mode



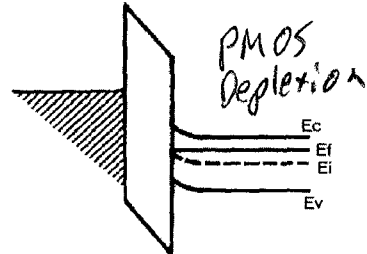
3.) (4-points) If the MOS capacitor shown in the diagram to the right were used in a MOSFET transistor, which of the following COULD result (more than one answer possible):

- a.) NMOS transistor biased into Cutoff mode
- b.) PMOS transistor biased into Cutoff mode
- c.) NMOS transistor biased into linear/triode mode
- d.) PMOS transistor biased into linear/triode mode
- e.) NMOS transistor biased into Saturation mode
- f.) PMOS transistor biased into Saturation mode



4.) (4-points) If the MOS capacitor shown in the diagram to the right were used in a MOSFET transistor, which of the following COULD result (more than one answer possible):

- a.) NMOS transistor biased into Cutoff mode
- b.) PMOS transistor biased into Cutoff mode
- c.) NMOS transistor biased into linear/triode mode
- d.) PMOS transistor biased into linear/triode mode
- e.) NMOS transistor biased into Saturation mode
- f.) PMOS transistor biased into Saturation mode



5.) (4-points) For a MOSFET biased into saturation...

- a.) The channel acts like a resistor connecting source to drain
- b.) The channel does not exist due to this region being fully depleted
- c.) The channel acts like a resistor connecting source to drain but has a depleted region at the drain end.
- d.) The channel needs to be changed because there is never anything good on TV anyway.
- e.) None of the above

6.) (20-points) In the two amplifier circuits below, the only difference in the top amplifier versus the bottom amplifier is the positions of the resistors/capacitors, which are reversed (swapped). Determine the voltage gains V_{out1}/V_{in} and V_{out2}/V_{in} . You may assume that the Op-Amps are ideal.

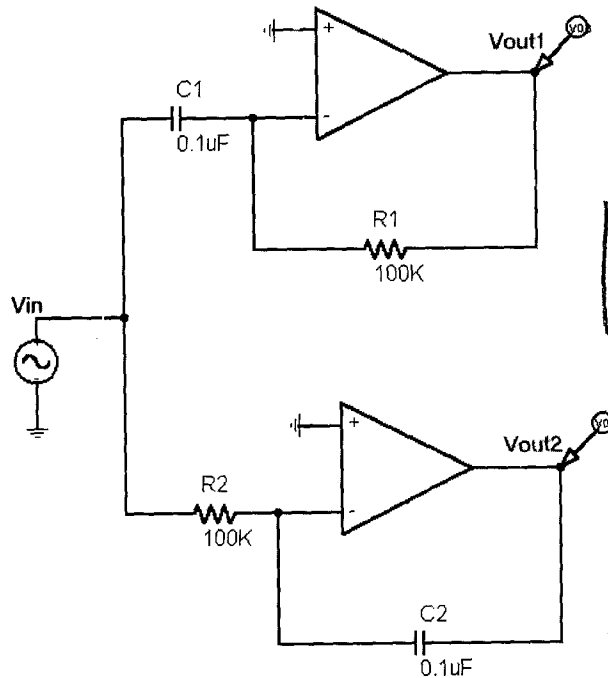
Bonus Points (each must be completely correct or no points awarded):

(10 points) Plot the shape of the transfer function from 0.1 Hz to 10KHz.

(5 points) What mathematical function does the top circuit implement?

(5 points) What mathematical function does the bottom circuit implement?

(5 points) The bottom circuit has a problem if implemented with real devices. Identify this problem and propose a solution.



$$\frac{V_{out1}}{V_{in}} = -\frac{R_1}{C_1 s}$$

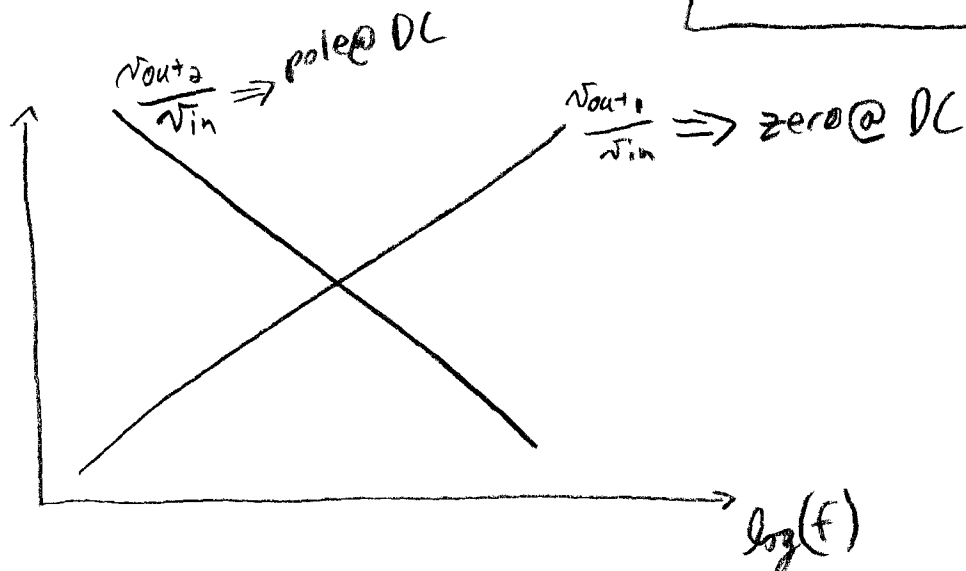
$$\frac{V_{out1}}{V_{in}} = -R_1 C_1 s$$

$$\frac{V_{out2}}{V_{in}} = -\frac{1}{C_2 s R_2}$$

$$\frac{V_{out2}}{V_{in}} = -\frac{1}{R_2 C_2 s}$$

10pt. Bonus

$$20 \log \left| \left(\frac{V_{out}}{V_{in}} \right) \right|$$



Extra work can be done here, but clearly indicate with problem you are solving.

5 pt. Bonus:

$$\frac{v_{out1}}{v_{in}} = (-R_1 C_1) s$$

$$\Rightarrow v_{out} = (-R_1 C_1) \underbrace{[s v_{in}]}$$

From your signals classes, this implements a derivative function

5 pt Bonus:

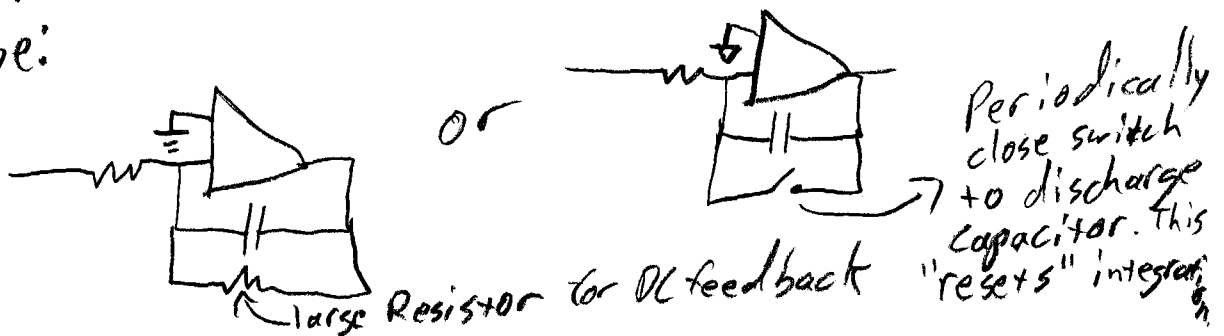
$$\frac{v_{out2}}{v_{in}} = -\frac{1}{R_2 C_2 s}$$

$$v_{out2} = \left(-\frac{1}{R_2 C_2}\right) \underbrace{\left[\frac{1}{s} v_{in}\right]}$$

From your signals classes, this implements an integrator.

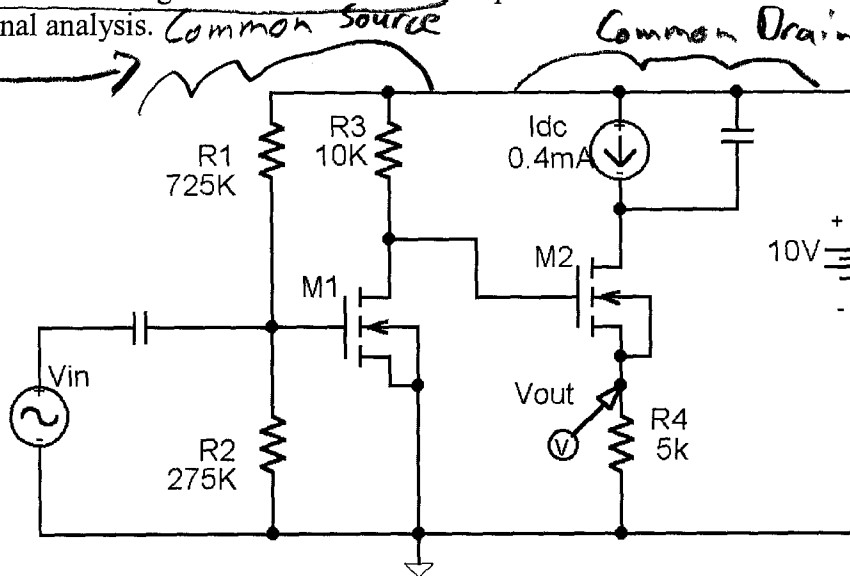
5 pt. Bonus

This circuit has no DC feedback. Thus, the transistors that make up the op amp input will have finite leakage currents which will tend to make the DC output drift with time. A solution would be:



Pulling all the concepts together for a useful purpose:

7.) (60-points) Given the following circuit and material parameters,
 (a) Determine the threshold voltage, V_T , flatband potential, ϕ_F , oxide capacitance per cm^2 , C_{ox} , and transistor transconductance parameter, K_n , (b) Identify the configuration of all stages in the amplifier. (c) What is the AC voltage gain, V_{out}/V_{in} ? You may assume all capacitors have infinite capacitance and are thus, AC shorts. Additionally consider the circuit to be operated at low frequencies where you can neglect all small signal capacitances. Grading will be based as such: 20 points for plug and chug calculations, 4 points for configuration identification, 18 points for DC solution and 18 points for small signal analysis.



$$\phi_F = \frac{kT}{q} \ln \left(\frac{1.68e16}{1e10} \right)$$

$$= 0.0259 \ln(1.68e6) = 0.371 \text{ V}$$

$$C_{ox} = \frac{3.9(8.854e-14)}{1.38e-6}$$

$$= 2.5e-7 \text{ F/cm}^2$$

$$K_n = \frac{Z}{L} \bar{\mu}_n C_{ox}$$

$$= \frac{10}{1} (100)(2.5e-7)$$

- Gate Length, $L=1 \mu\text{m}$
- Gate Width, $W=Z=10 \mu\text{m}$
- Effective mobility, $\bar{\mu}_n=100 \text{ cm}^2/\text{VSec}$
- Oxide Thickness, $t_{ox}=x_{ox}=13.8 \text{ nm}$
- Channel Length Modulation parameter, $\lambda=0.1 \text{ V}^{-1}$
- Substrate Doping, $N_A=1.68e16 \text{ cm}^{-3}$
- Oxide relative Dielectric Constant, $\epsilon_{r-oxide}=K_O=3.9$
- Substrate relative Dielectric Constant, $\epsilon_{r-semiconductor}=K_S=11.7$
- Substrate intrinsic concentration, $n_i=1e10 \text{ cm}^{-3}$
- Dielectric Constant of free space, $\epsilon_0=8.854e-14 \text{ F/cm}$

$$V_T = 2\phi_F + \frac{K_S \epsilon_0}{C_{ox}} \sqrt{\frac{2q N_A}{K_S \epsilon_0}} \quad 2\phi_F$$

$$= 2(0.371) + \frac{11.7(8.854e-14)}{2.5e-7} \sqrt{\frac{2(1.6e-19)}{11.7(8.854e-14)}}$$

$$\dots \frac{1.68e16(2)(0.371)}{1} = 1 \text{ V}$$

Plug and Chug Answers (As these answers are required to continue on with the problem, you may purchase these answers for 5 points each. Exam proctors should clearly mark values as "PURCHASED"):

$V_T = 1 \text{ V}$

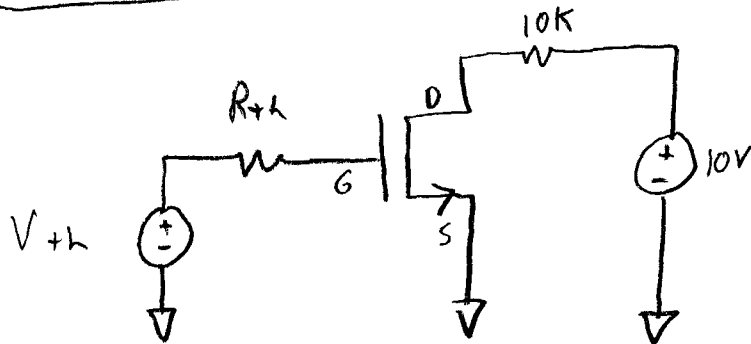
$\phi_F = 0.371 \text{ V}$

$C_{ox} = 2.5e-7 \text{ F/cm}^2$

$K_n = 250 \mu\text{A/V}^2$

Extra work can be done here, but clearly indicate with problem you are solving.

DC for M1:



$$V_{th} = 10V \frac{275}{275 + 725}$$

$$= 2.75V$$

$$R_{th} = 275k \parallel 725k$$

$$= 199.4k$$

Since the source is grounded, $V_{GS1} = V_{th} = 2.75V$

$$V_{DS1} = 10V - I_{DS1}(R_3)$$

Assume Saturation:

$$I_{DS1} = \frac{K_n}{2} (V_{GS1} - V_{TN})^2 (1 + \lambda V_{DS1})$$

$$I_{DS1} = \left(125 \frac{\mu A}{V^2}\right) (2.75 - 1)^2 (1 + 0.1 [10V - I_{DS1} 10k])$$

$$I_{DS1} = [0.0003828] [2 - I_{DS1} 1k]$$

$$I_{DS1} = 0.0007656 - I_{DS1} (0.3828)$$

$$I_{DS1} = \left(\frac{0.0007656}{1 + 0.3828}\right) = \boxed{554 \mu A = I_{DS1}}$$

$$V_{DS1} = 10V - (554 \mu A) 10k$$

$$V_{DS1} = 4.46V$$

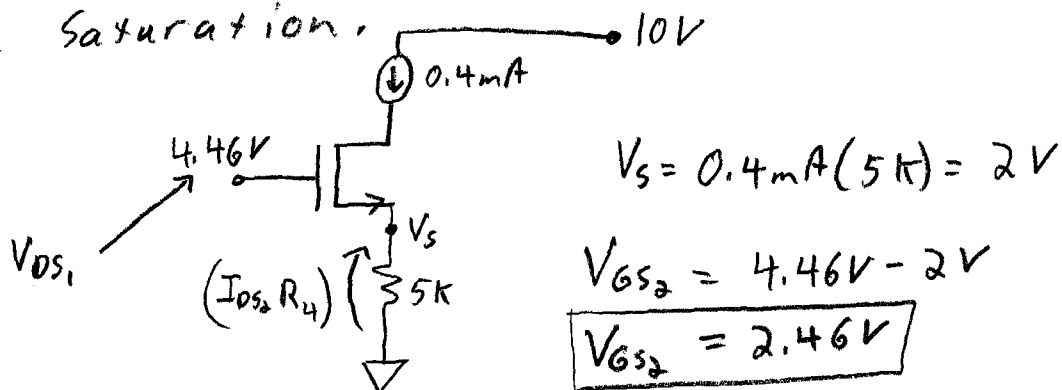
$$V_{GS} = 2.75V$$

$$V_T = 1V$$

$$V_{GS} - V_T < V_{DS} \Rightarrow \underline{\text{Saturation}}$$

Extra work can be done here, but clearly indicate with problem you are solving.

DC M2: Since the DC current source insures a constant current, M₂ should be in saturation.



$$I_{OS2} = \frac{\mu_n}{2} (V_{GS2} - V_{TN})^2 (1 + \lambda V_{OS2})$$

$$0.4 \text{ mA} = \left(\frac{125 \mu\text{A}}{\text{V}^2} \right) (2.46 - 1)^2 (1 + 0.1 V_{OS2})$$

$$V_{OS2} = 5.01 \text{ V}$$

$$V_{GS2} - V_T < V_{OS2}$$

$$1.46 < 5.01 \text{ V} \Rightarrow \text{saturation confirmed}$$

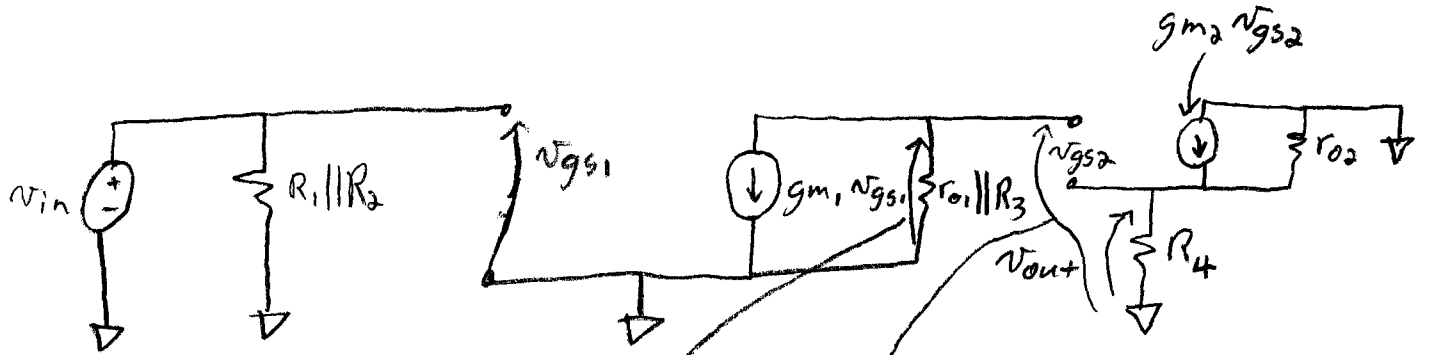
$$g_{m1} = \frac{I_{OS1}}{\frac{V_{GS1} - V_T}{2}} = 633 \mu\text{A/V}$$

$$g_{m2} = \frac{I_{OS2}}{\frac{V_{GS2} - V_T}{2}} = 548 \mu\text{A/V}$$

$$r_{o1} = \frac{1}{\frac{\lambda \mu_n}{2} (V_{GS1} - V_T)^2} = 26.1 \text{ k}\Omega$$

$$\dots r_{o2} = 37.53 \text{ k}\Omega$$

Extra work can be done here, but clearly indicate with problem you are solving.



Step 1 : 1.) $v_{in} = v_{gs1}$

$$2.) -g_{m1} v_{gs1} (r_{o1} \parallel R_3) = [g_{m2} v_{gs2} (R_4 \parallel r_{o2}) + v_{gs2}]$$

$$3.) v_{out} = g_{m2} v_{gs2} (R_4 \parallel r_{o2})$$

$$\frac{v_{out}}{v_{in}} = \left(\frac{v_{out}}{v_{gs2}} \right) \left(\frac{v_{gs2}}{v_{gs1}} \right) \left(\frac{v_{gs1}}{v_{in}} \right)$$

$$= g_{m2} (R_4 \parallel r_{o2}) \left[\frac{-g_{m1} (r_{o1} \parallel R_3)}{1 + g_{m2} (R_4 \parallel r_{o2})} \right] \quad (1)$$

$$= \underbrace{-g_{m1} (R_3 \parallel r_{o1})}_{\text{CS gain}} \left[\underbrace{\frac{g_{m2} (R_4 \parallel r_{o2})}{1 + g_{m2} (R_4 \parallel r_{o2})}}_{\text{CD gain}} \right]$$

$$= -(0.000633)(7230) \left[\frac{0.000548(4412)}{1 + 0.000548(4412)} \right]$$

$$= -(4.577) (0.707)$$

$$\boxed{\frac{v_{out}}{v_{in}} = -3.24 \text{ V/V}}$$