

Assume Saturation:  
1) 
$$I_0 = \left(\frac{0.25 \text{ mA/v}^2}{2}\right) \left(V_{65} - 1\right)^2$$
  
2)  $V_{65} = 4.05 - 27,000 I_0$   
 $I_0 = \left(0.125 \text{ mA/v}^2\right) \left(3.05 - 27,000 I_0\right)^2$   
 $I_0 = 82.2 \text{ mA}$ 

View  $V_{0S} = 15 - 82000 I_0 - 27,000I_0 = 6.04V$   $(1.93 - 1) < 6.04 \implies Saturation Verified$   $V_{TN}$   $V_{0S}$  AC: Rin AC: Rin  $\frac{AC:}{(V_{es}-V_{TN})} \stackrel{Rin}{=} \frac{1}{9} R_s \frac{1}{9} \sqrt{s_s} \frac{$ 

$$g_{m} = \underbrace{(32, 2e-6)(2)}_{1,93-2} A_{v} = \underbrace{(R, 1|R_{2})}_{R, 1|R_{2} + Rin} (-g_{m}(R_{0}||R_{3}))$$

$$g_{m}^{=} (198e-6 A) A_{v} = \underbrace{(0, 998)}_{A_{v} = (0, 998)} (-198e-6 (82\pi||470k))$$

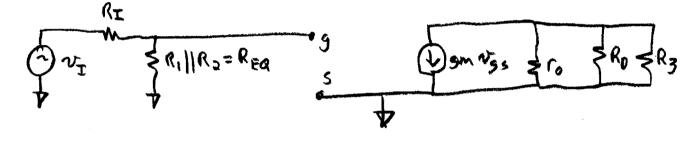
$$A_{v} = -13.8 V/V$$

Note only 1 current. 13.31 PMOS Common-Gate Amplifier  $T_D = \frac{12 + V_{GS}}{33000} = \frac{200 \times 10^{-6}}{2} (V_{GS} - 1)^{10}$ Depletion mode pmosjvipio  $V_{GS} = -0.84 V$  |  $I_D = 338 \mu A$  $V_{DS} = -(12 - 33000I_D - 22000I_D + 12)$ VDS = -5.41 V >> 5.41 2 -> 1.84 VOS 2 VES-VTP > 0 => Satur verified Q-point:  $(338 \ \mu A, -5.41 \ V)$ = 367,4 e-6 A/V Norton ro => o since no à given  $\frac{1}{2} \frac{1}{2} \frac{1}$  $\frac{v_{\rm I}}{R_{\rm I}}$ 1) - N35 = (inor + gm N35) thor 2) No= (-gm N55) (R3/1R0)  $-v_{35} = \left(\frac{v_{1}}{R_{T}} + 9 \times v_{55}\right) \left(R_{1} || R_{T}\right)$  $\frac{N_0}{N_{55}} = -gm(R_3 ||R_0)$  $- \sqrt{g_{5}} = \frac{N(R,R_{I})}{RI(R,+RI)} + (m\sqrt{g_{5}}) \left(\frac{R,R_{I}}{(R,+RI)}\right)$ = -6.63  $A = \frac{N_0}{N_{55}} \frac{N_{55}}{1} = (-0.834)(-66)$  $-v_{55}\left(1+g_{\rm R}R_{\rm I}|R_{\rm I}\right)=\frac{v_{\rm A}}{R_{\rm I}}\left(R_{\rm I}\right)|R_{\rm I}\right)$ A= 5.53 V/V  $\frac{N_{55}}{N_{1}} = \frac{-R_{1}}{(R_{1} + R_{I})(1 + 5m_{1}R_{1})}$ = - 0.834 V/v

For the bias network :  $V_{EQ} = 10V \frac{430k\Omega}{430k\Omega + 560k\Omega} = 4.343V | R_{EQ} = 430k\Omega | 560k\Omega = 243k\Omega$   $I_D = \frac{5x10^{-4}}{2} (V_{GS} - 1)^2 | V_{GS} = 4.343 - 2x10^4 I_D \rightarrow V_{GS} = 1.72 V | I_D = 131 \mu A$   $V_{DS} = 10 - 63k\Omega (131\mu A) = 1.75V \ge V_{GS} - V_{IN}$  so active region assumption is ok.  $\left(\frac{1}{2} + 1.75\right)$ 

$$g_{m} = \sqrt{2(5x10^{-4})(131\mu A)} = 362\mu S + r_{o} = \frac{(0.0133^{+1.75})}{131\mu A} = 586k\Omega$$

$$A_{v} = \frac{(243k\Omega)}{(243k\Omega + 1k\Omega)}(362\mu S)(586k\Omega + 43k\Omega + 100k\Omega) = -10.3 \quad V/v$$



## 13.98

3.) Jaeger 13.90 Plus, solve for the input and output resistances.

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Small Signal Analysis  
Rin  

$$N_{5} \bigoplus R_{5} \bigoplus R_{1}||R_{2} = \sqrt{2} \int \frac{1}{2} R_{0} \bigoplus R_{3} \int N_{5}$$
  
 $\frac{N_{65}}{N_{5}} = \frac{R_{1}||R_{2}}{R_{5} + R_{1}||R_{2}} = 0.996 \frac{V}{N}$   
 $\frac{N_{65}}{N_{65}} = -gm \bigoplus (r_{0}||R_{0}||R_{3})$   
 $= -0.000362 (28.6 \text{ k})$   
 $= -10.35 \frac{V}{N}$   
 $A_{V} = \frac{N_{65}}{N_{5}} \frac{N_{6}}{N_{65}} = -0.996 (10.35)$   
 $\boxed{A_{V} = -10.31 \frac{V}{N}}$   
This is greater than the results  
from figure 13.33 in the text  
since  $gm = \frac{105}{N_{65}}$  increases with decreasing  
 $205 \text{ due to V_{60-M}}$  that the total of the tota

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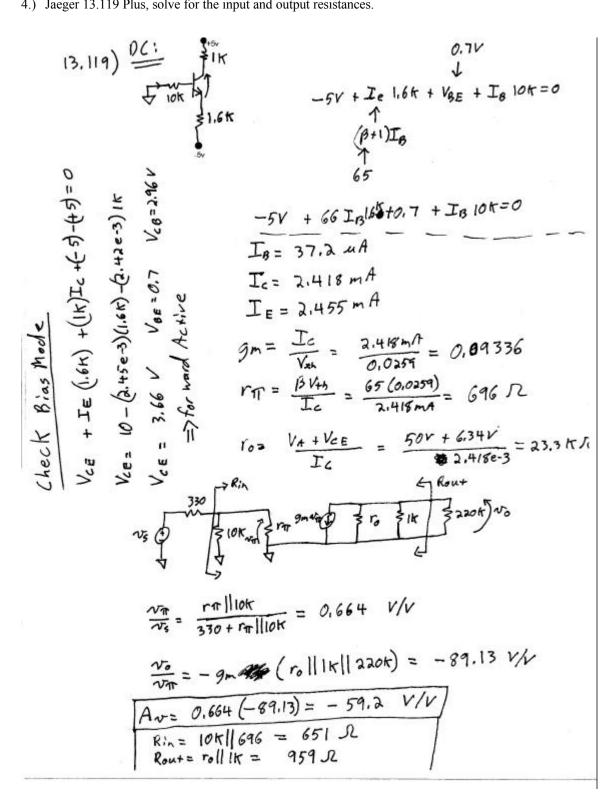
.

3) No= (- 5m Nbe) RL  $\frac{N_0}{N_{be}} = -(0.096)(995) = -95,56 \, V/V$  $A_{V} = \begin{pmatrix} v_{50} \\ v_{5e} \end{pmatrix} \begin{pmatrix} v_{5e} \\ v_{5e} \end{pmatrix} \begin{pmatrix} v_{5e} \\ v_{5r} \end{pmatrix} \begin{pmatrix} v_{5e} \\ v_{T} \end{pmatrix}$ - (-95,56) (0,34) (0,968) Av = -31.45 V/V

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This problem is the same problem without the 15 ohm resistor. Understand what an emitter resistor does to the gain. It also shows more detail on the DC solution and calculates input and output resistances.

4.) Jaeger 13.119 Plus, solve for the input and output resistances.



5.) a.) Use ideal opamps to design a filter (show work) that has 2 zeros at DC, and poles at 100 Hz, 10KHz, and 500 kHz and to have a bandpass gain of 1000 v/v. b.) Simulate this filter in PSPICE using ideal voltage controlled voltage amplifiers (setting gain to ~1e9). Plot the 20xLOG(Voltage Gain) verses Log(frequency) up to 10 MHz. c.) Simulate this filter in PSPICE using the u741 Operational amplifier model. Plot the 20xLOG(Voltage Gain) verses Log(frequency) up to 10 MHz. d.) Explain the differences between your results in b and c.

Note: Sample lowpass filter circuits are available on the web page illustrating how to model the op amps.

Since each basic high pass filter has a zero at DC and a pole, and each basic low pass filter has only one pole, we need 2 high pass stages and one low pass stage. Noting as was done in the notes that we can use a bandpass configuration to combine the low and high pass functions around one op-amp, we can perform this operation with only 2 op-amps.

Generally, to preserve the "pass-band gain" at the desired 1000 v/v (or 60 dB), we need to have our lowest and highest "break frequencies" (the frequencies where the slope of the Bode Plot changes) in our first stage. Otherwise, the first stage will be reducing the gain in frequency ranges where the second stage is trying to amplify the signal.

Thus, the circuit on the next page is our solution. This circuit's transfer function is:

$$\frac{Vout}{Vin} = \left(\frac{R_2C_1s}{1+R_1C_1s}\right) \left(\frac{1}{1+R_2C_2s}\right) \left(\frac{R_4C_3s}{1+R_3C_3s}\right)$$

where the first term is the high pass filter of the first op-amp (E1, or U1), the second term is the low pass filter of the first op-amp (E1, or U1), and the last term is the high pass filter of the second op-amp (E2, or U2).

This function implements the zeros at DC due to the  $s^2$  term in the numerator. I will choose to give (free choice) 20 dB of gain (10 V/V) in the first stage, and 40 dB of gain (100 V/V) in the second stage for a total gain of 60 dB (1000 V/V). This sets the ratio of resistors as:

$$\frac{R_2}{R_1} = 10$$
 and  $\frac{R_4}{R_3} = 100$ 

due to the desired "pass-band gain" constraints .

Now we can set our frequencies:

$$f_{pole@100 Hz} = \frac{1}{2p R_1 C_1}$$

$$f_{pole@500 kHz} = \frac{1}{2p R_2 C_2} = \frac{1}{20p R_1 C_2}$$

$$f_{pole@10 kHz} = \frac{1}{2p R_3 C_3}$$

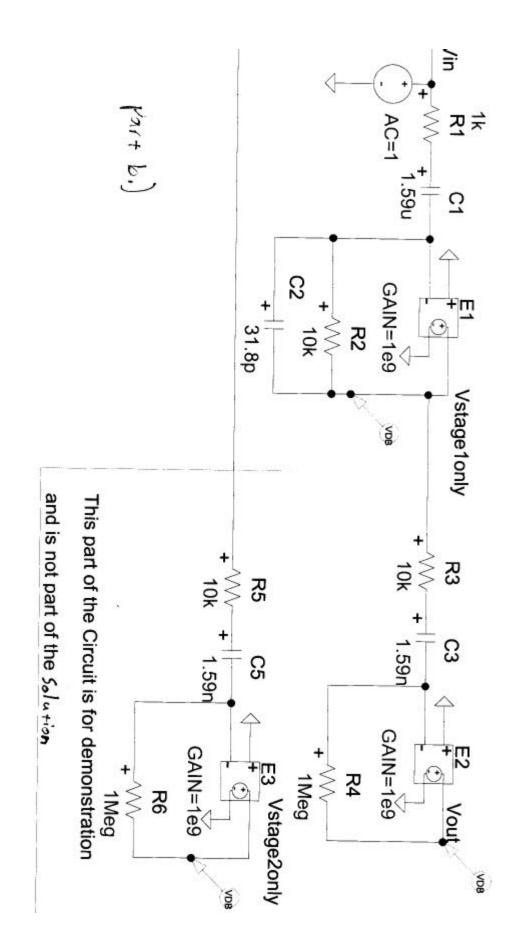
Beyond these limitations (and practical limits of resistor and capacitor choices), we are free to choose parameters at will. The values below satisfy all of these constraints: R1=1K, R2=10K, R3=10K, R4=1Meg, C1=1.59uF, C2=31.9pF, and C3=1.59nF

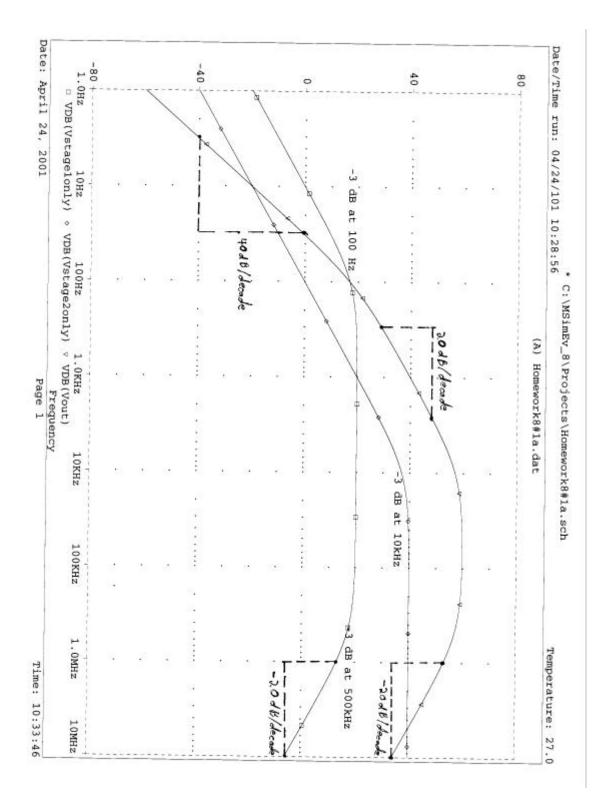
b.) The Bode Plot of the gain simulation from PSPICE of each stage (stage 1 is for E1, or U1 and stage 2 is for E2, or U2) is shown on the page following the circuit diagram. Note that the slope of the Bode Plot starts out at +40 dB per decade due to the existence of 2 zeros at DC. After the first pole at 100 Hz (set by stage 1), the slope reduces to +20 dB/decade. After the second pole at 10

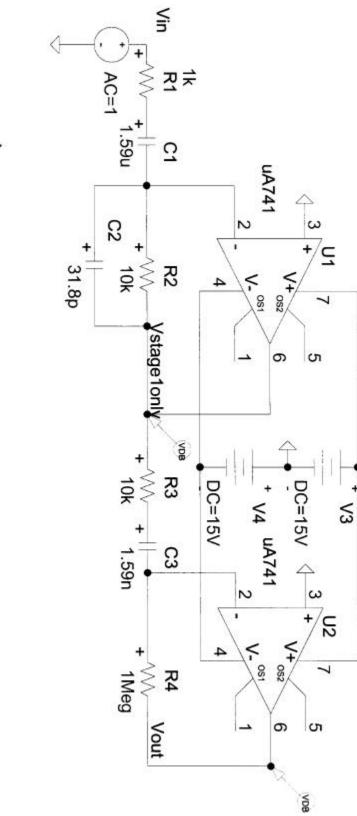
kHz (set by stage 2) the slope is zero. After the last pole at 500 kHz (set by stage 1), the slope is - 20 dB/decade. Also note that stage 2 implements the high pass function while stage 1 implements the bandpass function. The pass-band gain is correct at 60 dB (or 1000 V/V).

- c.) The circuit using the ua741 op-amp is shown on a following page. Note that the model for the ua741 op-amp does require us to include the power supply voltage sources. Otherwise everything is identical to the previous circuit from parts a and b. The Bode Plot for this circuit is shown on a following page. The lower frequency response (~<10kHz) behaves identically to that of the ideal case. However, the frequency response at high frequencies is severely degraded resulting in gain that falls off faster than the expected -20 dB/decade.
- d.) The rapid decrease in the high frequency gain results from the finite "Gain-Bandwidth" of the ua741.

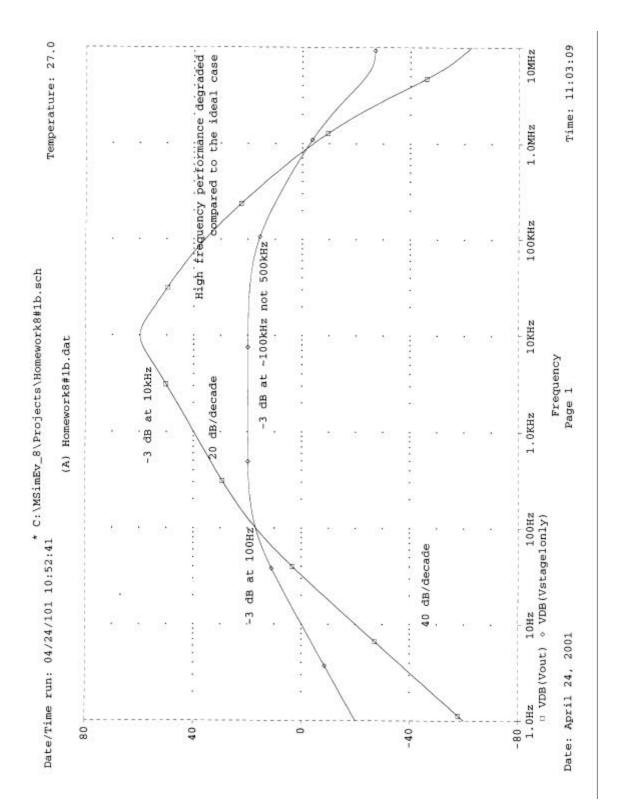
**Further incite into this problem:** Since the gain begins to role off somewhere around ~100 kHz for stage 1 which has a gain of 10, we can estimate the gain-bandwidth product to be (10 v/v)(100kHz)=1,00,000 Hz. We can check this calculation by using the unity gain (follower) circuit shown on a following page. The Bode Plot for this circuit is also shown. From this figure we clearly see that the gain drops by -3dB at ~1MHz confirming our calculation. This concept of gain effecting frequency response is also shown in the last Bode Plot for this problem for 3 standard non-inverting amplifiers with gains of 101, 1001 and 10,001 V/V. Note the lower frequency response for the higher gain circuit. All of these gain responses converge to the open loop frequency response for the ua741 (not shown).

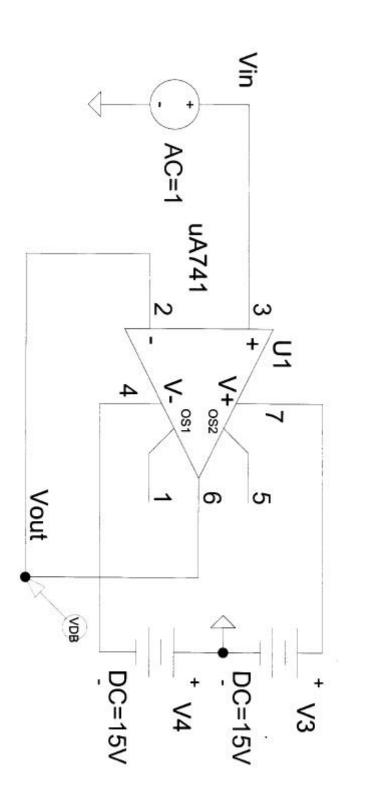






part 2.)





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