# ECE 6450 Introduction to Microelectronics Technology

*Exam 1*

*September 26, 2014*

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Print your name clearly: Solutions

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**Instructions:**
Read all the problems carefully and thoroughly before you begin working. **DO NOT SEPARATE ANY PAGES OF THIS EXAM.** You are allowed to use 1 sheet of notes (1 page front and back) as well as a calculator. There are 100 total points. Observe the point value of each problem and allocate your time accordingly. **SHOW ALL WORK ON THE PROVIDED SHEETS AND CIRCLE YOUR FINAL ANSWER WITH THE PROPER UNITS INDICATED**. Write legibly. No work should be done on any other paper. If I cannot read it, it will be considered to be a wrong answer. Do all work on the paper provided. Turn in all scratch paper, even if it did not lead to an answer. Report any and all ethics violations to the instructor. Good luck!

Sign your name on **ONE** of the two following cases:

I did not observe any ethical violations during this exam:

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I observed an ethical violation during this exam:

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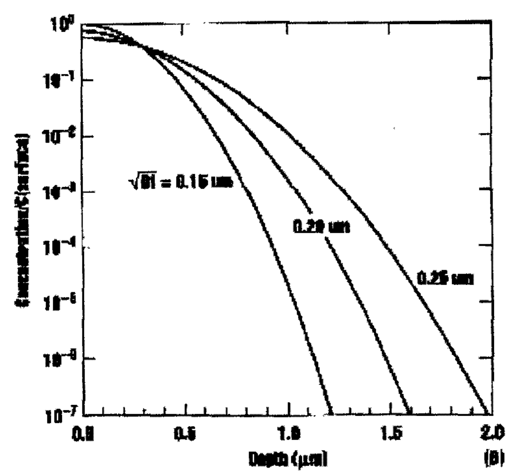
**Problem 1. (20 points total in 4, 5 point parts):**
True/False and Multiple Choice and short answer/calculation:

a.) Based on the periodic table (see attached table) which of the following are true (one or more answers possible)?
   1.) C will have a larger bandgap than Si
   2.) CdTe will have a smaller bandgap than HgTe
   3.) $Cd_{2.2}Mn_{0.8}S$ is a real semiconductor
   4.) All of the above
   5.) None of the above
   6.) I wish I had gone to Clemson instead of Ga Tech.

**b.)** Which of the following defects are considered planar (2D) defects (may have more than one answer....or not)?
   1.) Vacancies
   2.) Interstitials
   3.) Dislocations
   4.) Stacking faults
   5.) Precipitates
   6.) Grain Boundaries

c.) Given the diffusion profiles obtained below for the same temperature and identical dose in all cases, which of the following are true (may have more than one answer...or not)?
   1.) This is a pre-deposition diffusion.
   2.) This is a drive in diffusion.
   3.) The area under each of the three curves is the same.
   4.) For the 0.20 um characteristic diffusion length case, it was performed for a shorter time than the 0.15 um case.
   5.) This is a Gaussian shaped profile.




d.) True or False (circle the correct answer)
The present (<22 nm node) Intel process uses exotic materials for the gate dielectrics because the capacitance per unit area is greatly increased compared to what is possible with thin $SiO_2$. (Hint: consider the effective oxide thickness comparison, EOT, of the alternative materials).

This question eliminated due to ambiguity

**Problem 2. (20 points total):**

Name and describe the process that produces silicon with the least concentrations of impurities like oxygen, carbon, and various undesirable metals. ***For full credit, keep your description to 4 sentences or less and feel free to draw diagrams to furthur explain your answer.***

Float Zone processing.

See book + notes for description.

**Problem 3. (60 points total):**

You are about to make your first MOSFET. This question makes a MOSFET in several steps.

**Assumptions:**

Assume no lateral oxidation nor diffusion occurs (I.E. consider only the 1 dimensional case), the wet oxide parameters are valid for all regions, regardless of initial conditions, and the porosity and density of wet and dry oxides are the same. To answer this question you must know which oxide, wet or dry is of higher quality.

At 1000 degrees C:

A=0.165 μm, B=0.0117 $\mu m^2$/hr and t=0.37 hr for dry oxides

A=0.226 μm, B=0.287 $\mu m^2$/hr for wet oxides.

At 1200 degrees C:

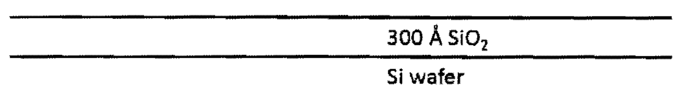
A=0.040 μm, B=0.045 $\mu m^2$/hr and t=0.027 hr for dry oxides

A=0.05 μm, B=0.720 $\mu m^2$/hr for wet oxides.

*Note: erfc(x)=1-erf(x), erf(0)=0, erf(∞)=1*

(6 pts)

A.) A 300 angstrom gate oxide is to be grown and should be of the highest possible electrical quality. What time at 1000 degrees C is required?



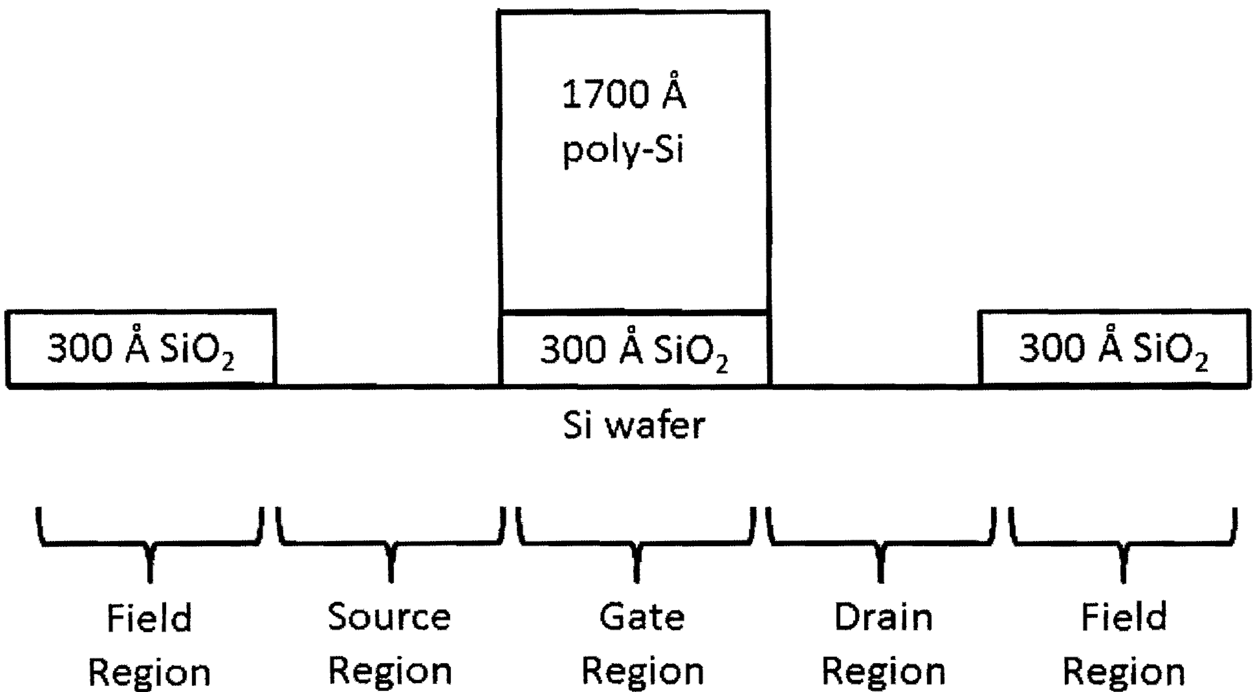

$$t = \frac{d^2 + Ad}{B} - \tau$$

$$= \frac{(0.03\,\mu m)^2 + (0.165\,\mu m)(0.03\,\mu m)}{0.0117\,\mu m^2/hr} - 0.37\,hr$$

$$\boxed{t = 0.13 \text{ hours}}$$

(10 pts)

B.) A 1700 angstrom thick polysilicon Gate metal is deposited and patterned which will act as a subsequent mask for the later diffusions and oxidation steps. Openings in the oxide are also created for the source and drain regions. Thus, the starting configuration for part (B) is as shown in the figure below. Phosphorous (P) is first deposited on a p-type silicon wafer uniformly boron




doped at $1\times10^{15}$ cm$^{-3}$ (bulk concentration) using Phosphine ($PH_3$) at 900 degrees C where the solubility of P in Silicon is $5\times10^{20}$ cm$^{-3}$. Assuming a neutral vacancy controlled diffusion with $D_o$=3.9 cm$^2$/sec and $E_a$=3.66 eV, what is the time required to achieve a dose of $1\times10^{15}$ atoms/cm$^2$? Note this is approximately a complete single atomic layer of Phosphorous on the surface.

→ $C_B$ → $C_s$

Predeposition

$$D = (3.9\ cm^2/sec)\ e^{-3.66\,eV/k(900+273)}$$

$$D = 7.33\times10^{-16}$$

$$Q_T = 1\times10^{15}\ atoms/cm^2 = \frac{2}{\sqrt{\pi}}\left(5\times10^{20}\ cm^{-3}\right)\sqrt{D\,t}$$

$t$ = 4286 sec
or
1.11 hr

12pts

C.) If water vapor is then introduced to the wafer, and simultaneously the phosphorous is driven into the wafer at 1200 degrees C, how much time is required to achieve a final junction depth of 0.1 um?

Drive In @ 1200°C

$$D = 3.9e^{-3.66/k(1473)} = 1.17e{-12}\ cm^2/s$$

$$x_j = 1e{-5}cm = \sqrt{4Dt \ln\left(\frac{Q_T}{C_B\sqrt{\pi}\sqrt{Dt}}\right)}$$

$$1e{-5} = \sqrt{(4.68e\ 12)(t) \ln\left(\frac{1}{\sqrt{\pi}\sqrt{D}\sqrt{t}}\right)}$$

Iteration

| t | right side |
|---|---|
| 1 | 8.05e-6 |
| 10 | 2.4e-5 |
| 5 | 1.74e-5 |
| 2.5 | 1.25e-5 |
| 1.25 | 9e-6 |
| 1.875 | 1.09e-5 |
| 1.5625 | 9.98e-6 |

→ **t = 1.56 seconds**

⇒ requires RTP or lower Dose

(10pts)

D.) What is the thickness of the oxide above the Source and Drain regions (assume the doped oxide grows at the same rate as undoped oxides on Si)?

t = 1.56 seconds

or 0.000433 hrs

$$d^2 + Ad = B(t + \tau)$$ → ∅ pre-existing oxide

$$d^2 + (0.05\,\mu m)d + 0.720\left(\frac{\mu m^2}{hr}\right)(0.000433)$$

$$d^2 + 0.05d - 0.000312 = 0$$

$$d = \frac{-0.05 \pm \sqrt{(0.05)^2 - 4(-0.000312)}}{2}$$

$$d = -0.0556 \text{ or } 0.00561\ \mu m$$

**$d = 56.1$ Å**

Note: I also accepted (0.56) 56.1Å due to "above" wording.

5pts

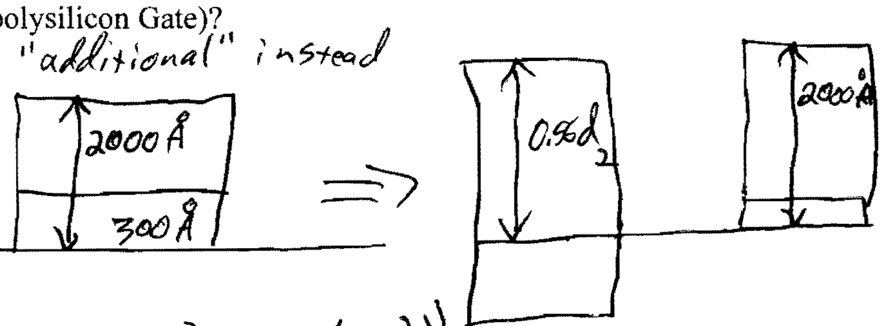
E.) How much of the wafer was consumed (thickness) in the source and drain regions?

$$0.44d = \boxed{24.7\,\text{Å}}$$

(Most) F.) What alternative time in step (C) would be needed to insure the wafer is globally flat (i.e. the field oxide is at the same height as the polysilicon Gate)?

Note: Some Interpreted this as "additional" instead of "alternative". Therefore my solution is for the "additional time". Accepted either 300 or 327 Å starting thickness.

327 ∓ 300 Å




$$d^2 + (0.05)d - (0.72)\left(0.000433 + \left(\frac{0.03^2 + 0.05(0.03)}{0.72}\right)\right)$$

$\tau = 0.00333$ hrs

$$0.56d_2 = 2000\,\text{Å}$$
$$d_2 = 3571\,\text{Å}$$

$$d^2 + 0.05d - 0.002712 = 0$$

$d = -0.08\,\mu m$ or $0.0327\,\mu m$

$d_1 = 327\,\text{Å}$

(300 for "alternative" interpretation)

$$t = \frac{(0.3571)^2 + 0.05(0.3571)}{0.720} - 0.0033$$

$t = 0.198$ hrs or ~11.9 minutes

G.) Draw the final cross-sectional view (i.e. similar to the above figure) of the resulting structure clearly showing the oxide-silicon interfaces.

Answer given after bonus turned in