ECE 6450 Dr. Alan Doolittle Homework #8

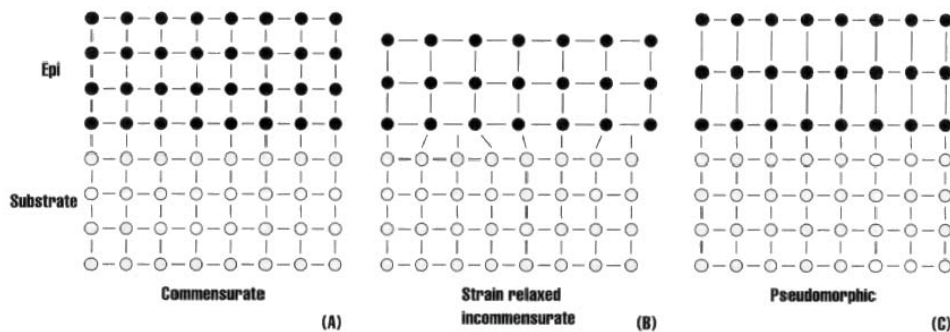


Figure 14-15 Epitaxial growth processes can be divided into (a) commensurate, (b) strain relaxed incommensurate, and (c) incommensurate but pseudomorphic.

Besides these problems, good example problems (not to be turned in) include 12.2 and 14.3 .

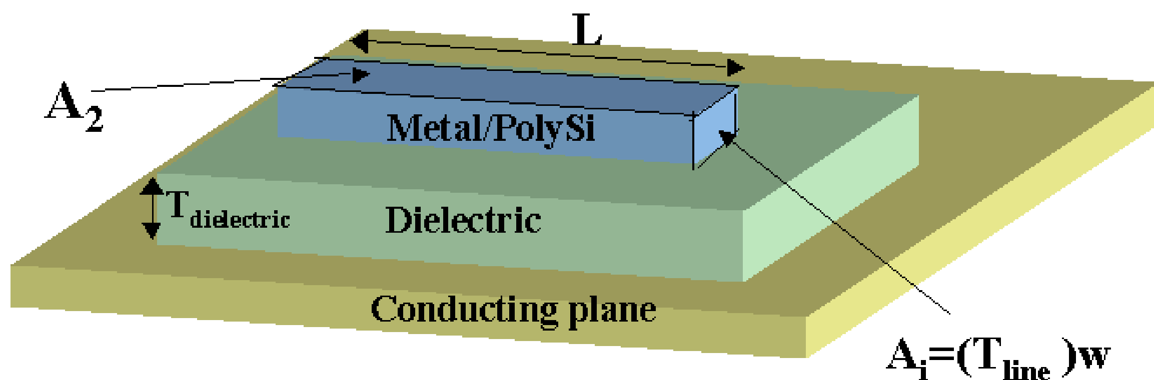
1.) A simple cubic epitaxial material is grown by MBE pseudomorphically strained to a simple cubic substrate as shown in cross section in figure 14-15C. During this process, extra energy is required to force the atoms to arrange in the above configuration. The epitaxial material has a lattice constant that is 1% larger than the substrate. The bond energy per atomic bond is 2.2 eV/bond, about the value found for GaN semiconductors. Assuming that the epitaxial layer has a natural unstrained lattice constant of 2.5 angstroms and the increase in bond energy is linearly dependent on its deviation from its natural bond energy (ie the strained material has a bond energy of 1.01 x 2.2 eV/bond), what is the total amount of stored *excess* energy in a 0.5 um thick layer on a 4" diameter wafer? For simplicity, you may assume the material distorts the same vertically as it does laterally (normally, this is not accurate as the Poisson ratio would describe the asymmetry in the distortion).

2.) Discuss the differences that pressure makes in a CVD or MOCVD system versus a MBE system. Include discussions of step coverage, purity, and growth rates. Would the same comparisons be applicable to sputtering versus evaporation?

3.) A thick low doped region is needed for a power device (often used to withstand very large voltages). Is this best achieved by diffusion, ion implantation or epitaxy? Why?

4.) A pure metallic aluminum layer is needed for a Schottky diode contact to Si. These contacts require a clean, undamaged region just under the metal. Is a thermal evaporator or a sputterer a better system to apply this metal? Why?

5.) A 1 cm long (global interconnect), 5000 angstrom thick, 1000 angstrom wide interconnect line is placed over a conducting plane separated by a 1 um thick dielectric SiO_2 layer (ε_R=K=3.9) as shown below. This forms a standard parallel plate capacitor (ignore fringing fields). Fill in the following table for the RC delay expected for the materials listed in the table (see figure and/or equations 15.18-15-20). This RC delay represents the time delay required for the electrical signal to charge the capacitor through the wire resistance. If the RC charging were viewed as a simple RC filter, what would be the frequency at which ½ the power is lost (an estimate of the maximum frequency operation of such an interconnect line). Why is copper used for high speed CMOS? What other means could be used to increase these operational frequencies?



$$R = \frac{\rho L}{A_i} \qquad C = \frac{\varepsilon_{dielectric} A_2}{T_{dielectric}} = \frac{\varepsilon_o \varepsilon_R L w}{T_{dielectric}}$$

$$RC = \frac{\rho \varepsilon_o \varepsilon_R L^2}{T_{line} T_{dielectric}}$$

L=	1	cm	
T_{line}=	5.00E-05	cm	
$T_{dielectric}$=	1.00E-04	cm	
ε_0=	8.85E-14	cm^2/F	
ε_R=K=	3.9		
Material	ρ ($\mu\Omega$-cm)	RC (nsec)	Frequency @ 50% power loss (GHz)
poly-Si	1000		
Al	2.65		
Cu	1.678		
Ag	1.586		

6.) Sketch a process flow for the CMOS structure below by drawing a series of drawings showing each step in the fabrication process. For each step provide details of the process used (tool, temperature, chemistry, etc...).

Figure Key:
Blue hashed region is an oxide.
Red cross-hashed region is the polysilicon gate contact.
Black layers are the metal contacts.

The CMOS technology we need to realize is shown below.