Lecture 2

Semiconductor Substrates

Reading:

Chapter 2

Phase Diagrams

Only certain compositions of materials are allowed at a given temperature and pressure when the material is in thermodynamic equilibrium. These compositions can be described by "Phase Diagrams". These allowed compositions effect semiconductor growth, and dictate the stability and electrical properties of metal-semiconductor contacts.

A phase diagram contains a "map" of a materials state including liquid only, solid only, coexisting as liquid with solid, or even various crystal structures of solid phases verses changes in material temperature, composition or pressure. We will only examine phase diagrams at a single pressure.

Consider the SiGe material system.

Determine the Composition of the Liquid and solid

Things to know about phase diagrams:

1.) Note the melting points of pure Ge and pure Si.

2.) Identify the Solid, Liquid and combination regions as well as the solidus (S/L+S) and liquidus (L/L+S) lines.

3.) Assume a **40% atomic Si** composition of the starting material (thoroughly mixed powder).

4.) As the material is heated from room temperature it starts in a "single phase field" (I.e, solid phase) and the composition remains the same, 40% atomic Si. However, as the temperature is elevated, the material begins melting at ~1070 degrees entering into a "two phase field" containing part liquid and part solid. When the material reaches ~1230 degrees, the material is completely melted and enters a "single phase field" (liquid) again. When in the solid or liquid regions, the composition is identical to the original composition (40%).

5.) When the 1070<Temperature<1230, both liquid and solid phases coexist. However, the composition of the liquid and solid materials can differ from the original composition. For example at 1200 C, draw a horizontal "tie line" (shown as green and purple) from the liquidus line to the solidus line. Read off the compositions of the liquid, **34%at Si**, and the solid, **67% at Si**. Note that the compositions of the solid and liquid are different.

6.) The amount of the melt that is solid and the amount that is liquid can be determined by the "Tie line" between the solidus line, and the liquidus line.
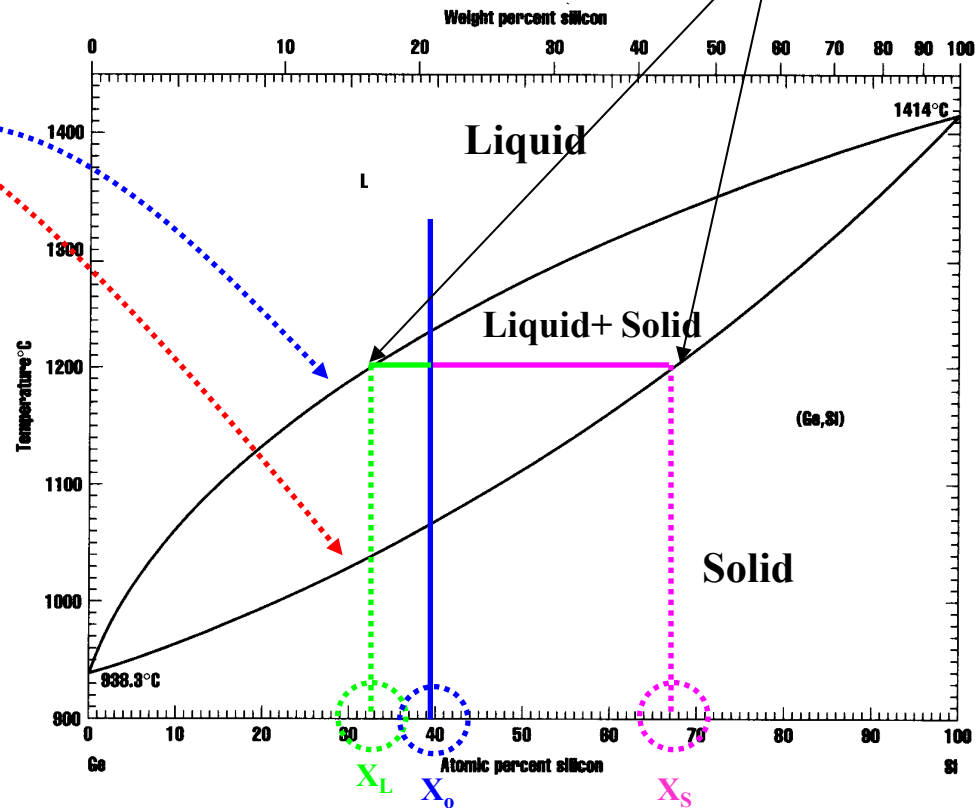
Figure 2-1 Phase diagram of Si-Ge. The dashed lines correspond to a heating process that remains in thermodynamic equilibrium *(courtesy of ASM International).*

$$\% \ Solid = \frac{X_o - X_L}{X_S - X_L} \ x \ 100$$

$$\% \ Solid = \frac{40 - 34}{67 - 34} \ x \ 100 = 18.2\%$$

$$\% \ Liquid = \frac{X_S - X_o}{X_S - X_L} \ x \ 100$$

$$\% \ Liquid = \frac{67 - 40}{67 - 34} \ x \ 100 = 81.8\%$$

So in this example, at 1200 deg C, 18% of the material is solid and that material has 67% Si and 33% Ge. Additionally, the 82% of the remaining material is liquid and contains 34% Si and 66% Ge

Consider the Si-Al material system.

Things to know about phase diagrams:

7.) In certain material systems a Horizontal, isothermal boundary exists that indicates the existence of phase transformations involving three phases. If α, β and γ are solid phases, we can classify the transformations as a:

      a.) Eutectic: $L \rightarrow \alpha + \beta$

      b.) Eutectiod: $\gamma \rightarrow \alpha + \beta$

      c.) Peritectic: $L + \alpha \longrightarrow \gamma$

Si-Al experiences a "Eutectic" transformation at 577 C. Note this is lower than the melting point of Al (660 C) and Si (1412 C). At this temperature, a liquid containing 11.3% Si will transform to two solid phases, (Al with 1.59%Si) + (Si + minimal fraction of Al-I.e. Al doped)
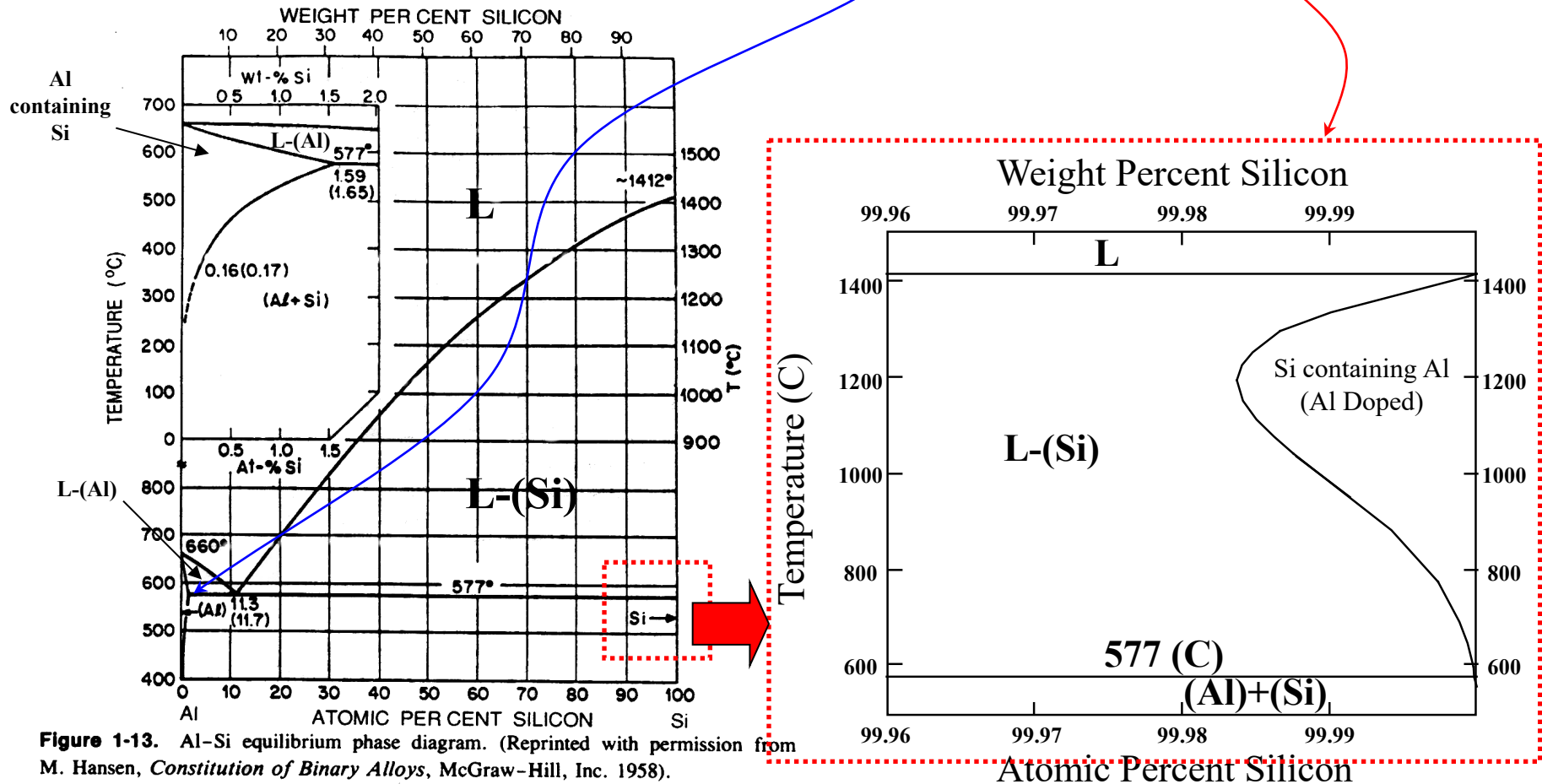

Figure 1-13. Al–Si equilibrium phase diagram. (Reprinted with permission from M. Hansen, *Constitution of Binary Alloys*, McGraw–Hill, Inc. 1958).

Consider the Si-Al material system.

Si-Al "Eutectic" transformation at 577 C. Note this is lower than the melting point of Al (660 C) and Si (1412 C). At this temperature, a liquid containing 11.3% Si will transform to two solid phases, (Al with 1.59%Si) + (Si + minimal fraction of Al-I.e. Al doped)

Chunks/Flakes of Si in the Al-Si mix.
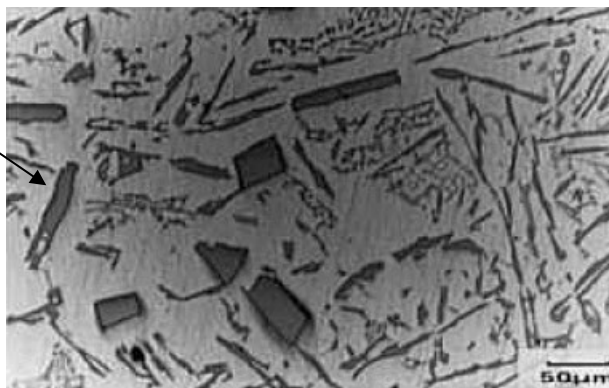
One Consequence: Only UGA students use pure aluminum contacts on Silicon. ☺ Ga Tech Students will use a small alloy mix of Al and Si.
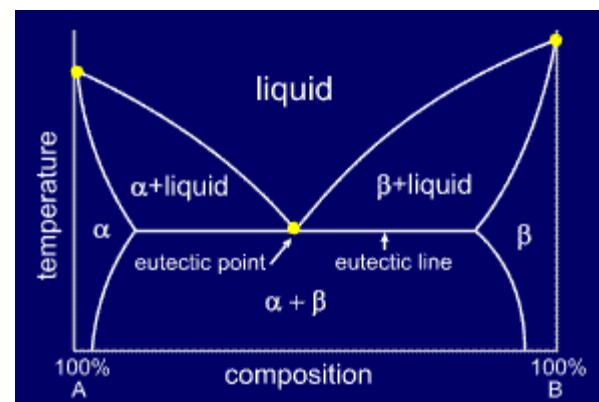
Figures from and a great explanation of phase diagrams in more detail than we have discussed here can be found at:

http://www.soton.ac.uk/~pasr1/index.htm

Defects in Semiconductors

Crystalline defects can be classified as:
1.) Point defects
2.) Line defects
3.) Planar defects
4.) Volume defects.

1.) Point Defects: Some include Vacancies (Schottky defect), interstitials, substitutional, and impurity-vacancy complexes (Frenkel defect, Si_I - V, is shown).

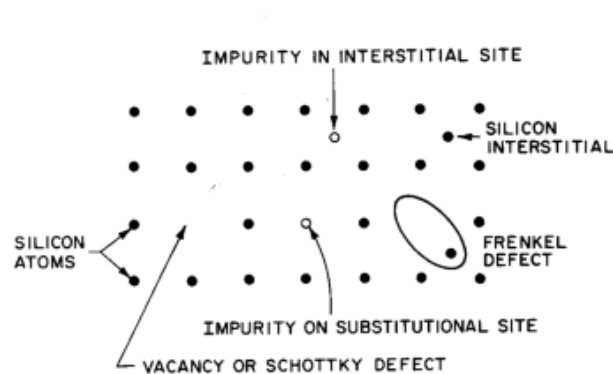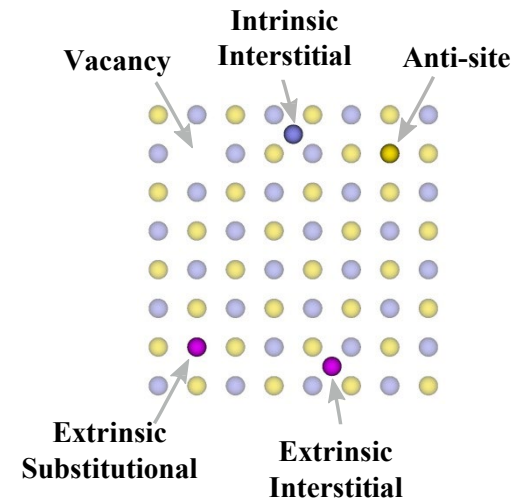Point Defects dictate most diffusion mechanisms, and thus, determine the impurity profile.

FIGURE 5
The location and types of point defects in a simple lattice.

Point Defects: Vacancies

Charge neutrality must exist in the crystal. When a vacancy is created,

     1.) it can cleanly break all four bonds ==> Neutral vacancy, V^0, neutral Interstitial,

     2.) n electrons may stay at the vacancy ==> $V^{-n} + I^{+n}$,

     3.) n electrons may go with the interstitial ==> $V^{+n} + I^{-n}$

The number of neutral vacancies is thermodynamically determined by,

$$\left[V^0\right] = N_O e^{-E_a/kT}$$

where N_o is the density of Atoms/cm³ and Ea is the activation energy for the formation of the vacancy (in silicon, $N_o = 5.02 \times 10^{22}$ cm⁻³ and $E_a = 2.6$ eV)

Singularly and doubly charged vacancies have concentrations that depend on the number of carriers present (reminder $n_i \propto e^{Eg/2kT}$ and np=n_i^2),

$$\left[V^-\right] \propto \left[V^0\right]\frac{n}{n_i} = f(n,T) \qquad\qquad \left[V^+\right] \propto \left[V^0\right]\frac{p}{n_i} = f(p,T)$$

$$\left[V^{--}\right] \propto \left[V^0\right]\left[\frac{n}{n_i}\right]^2 = f(n^2,T) \qquad \left[V^{++}\right] \propto \left[V^0\right]\left[\frac{p}{n_i}\right]^2 = f(p^2,T)$$

Point Defects: Interstitials

Atoms not residing on lattice sites are called interstitials. They can be foreign, unwanted impurities, intentionally introduced impurities, or "misplaced" host atoms. Dopant atoms diffuse through the semiconductor faster as interstitials, but we need to place them in substitutional sites to make use of them.

Oxygen Interstitial

Equivalent Oxygen Sites
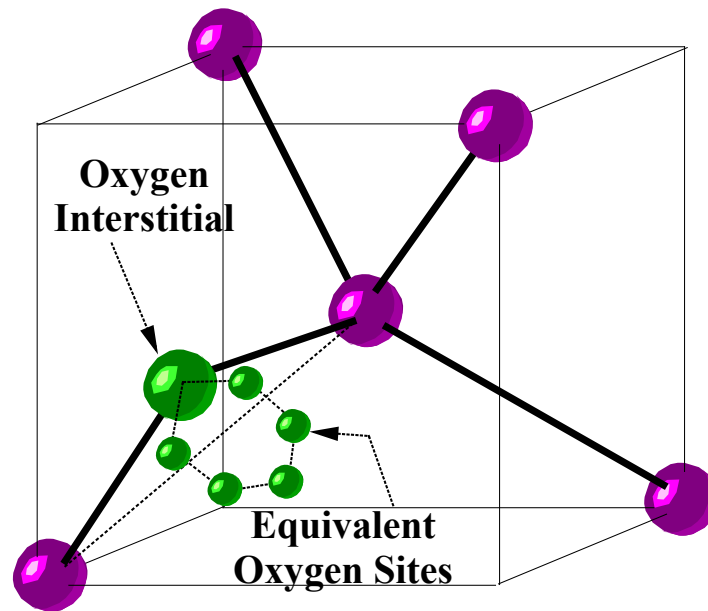
Point Defects: Substitutional

Impurities can replace a host atom in the lattice site. They can be foreign, unwanted impurities, or intentionally introduced impurities. You may want a dopant impurity to be on a substitutional site, but you may not want a heavy metal atom or other unwanted impurity to be on a substitutional site (harder to remove).
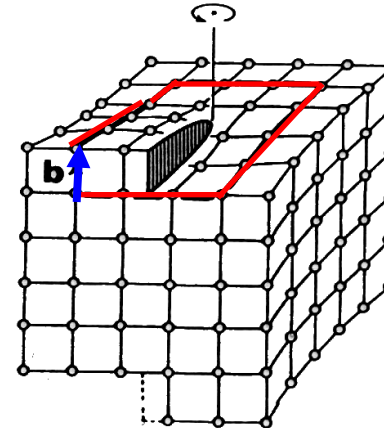
Carbon
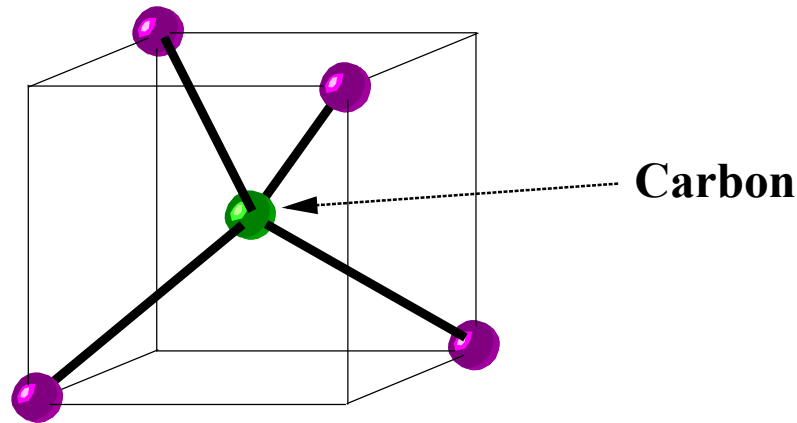
Si Lattice

Line Defects: Dislocations

A missing line or additional line of atoms is called a dislocation. Dislocations are either pure edge, pure screw or a combination of both type called mixed character.
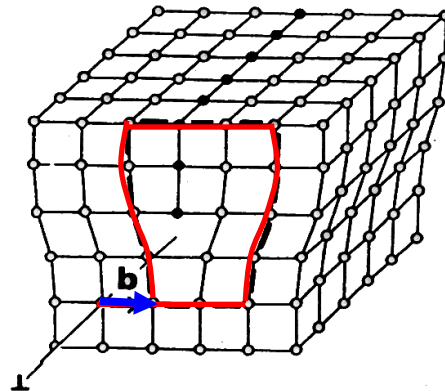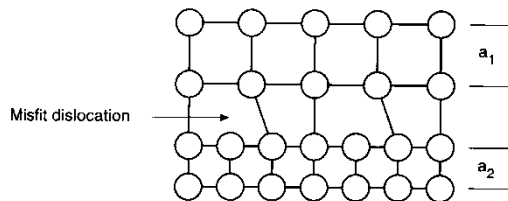

EDGE DISLOCATION

SCREW DISLOCATION

Misfit dislocation

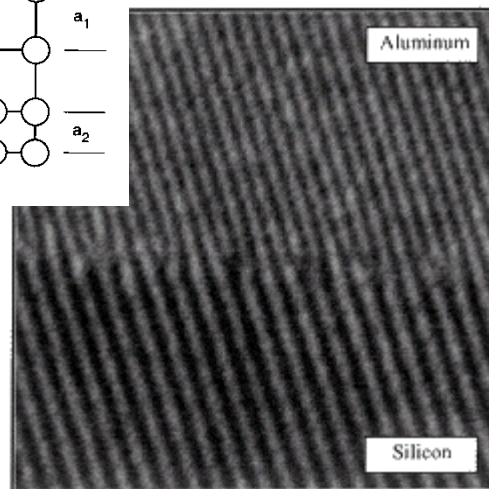**Figure 2.7** Misfit dislocation schematic.
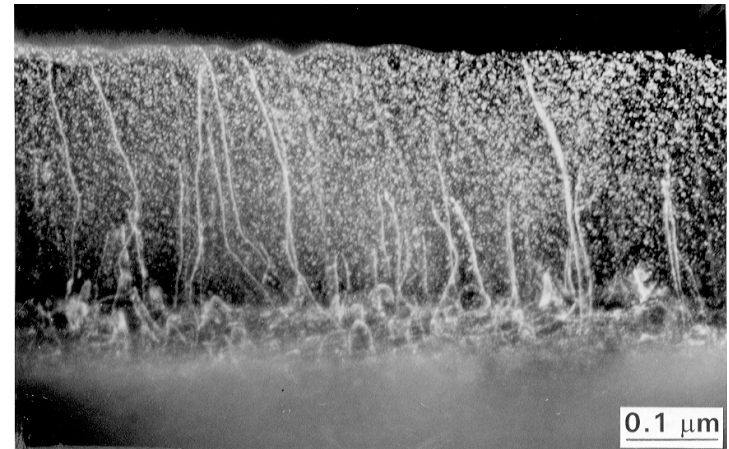

Aluminum

Silicon

Figure 2.8 A TEM comparable to the schematic of Figure 2.7 that shows the (111) planes of aluminum epitaxially overgrown on silicon and the (111) planes of the silicon substrate.


0.1 μm

The term, "threading", describes specific cases in which the dislocation "threads" through a grown layer (i.e. starts at or near the substrate and ends on the surface).

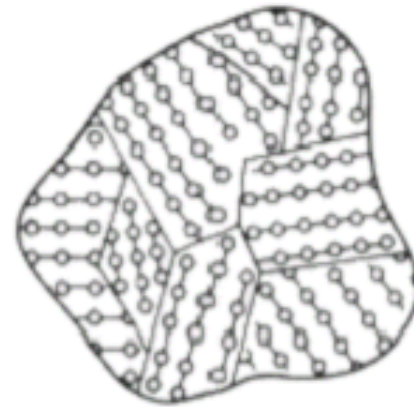# Planar Defects: Grain Boundaries & Stacking Faults

Two dimensional defects include:
1.) Grain boundaries in polycrystalline materials
2.) Stacking faults in crystalline material.

A **grain boundary** is an array of dislocations that line up to form a plane that forms a boundary between two crystalline regions (grains) that are misoriented relative to one another.
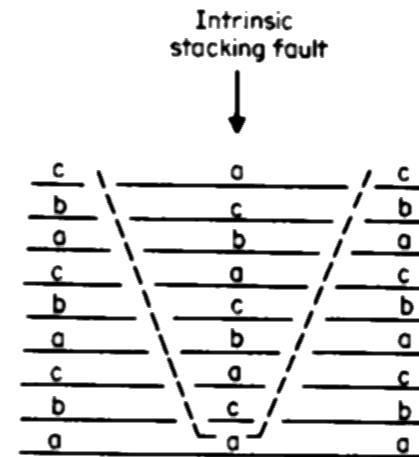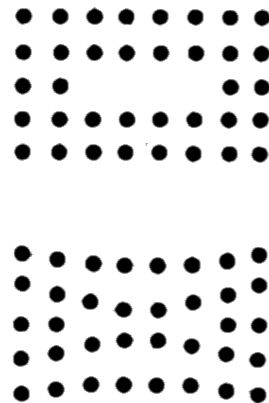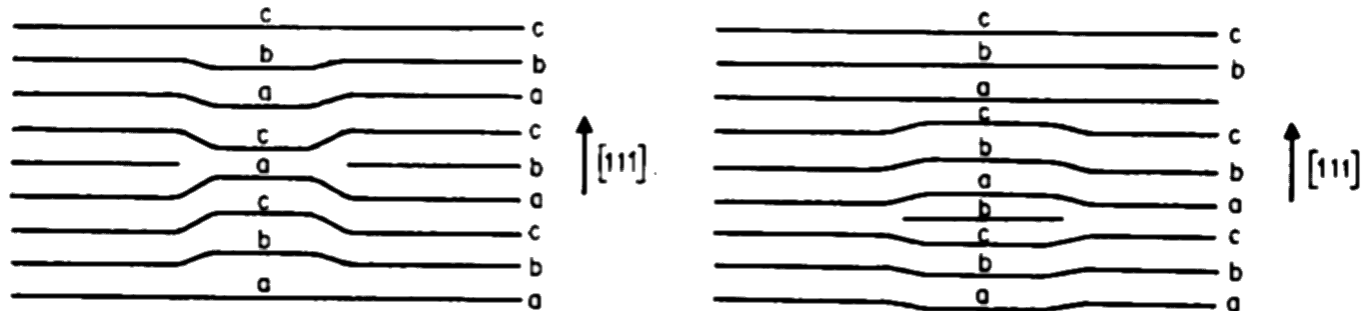
$$\theta = \frac{b}{d_b}$$
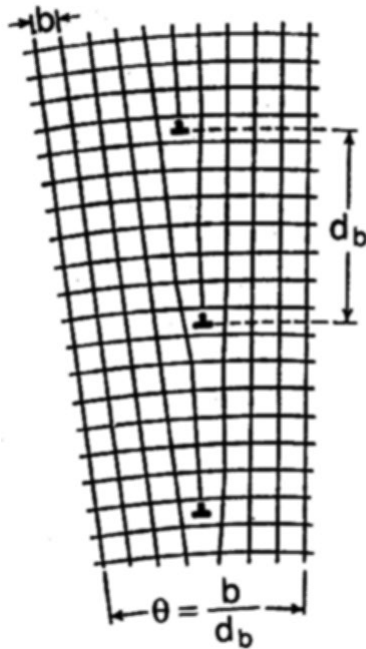
Low Angle Grain Boundary

High Angle Grain Boundaries

Planar Defects: Stacking Faults

A **stacking fault** is a disruption in the stacking of layers in the crystal.
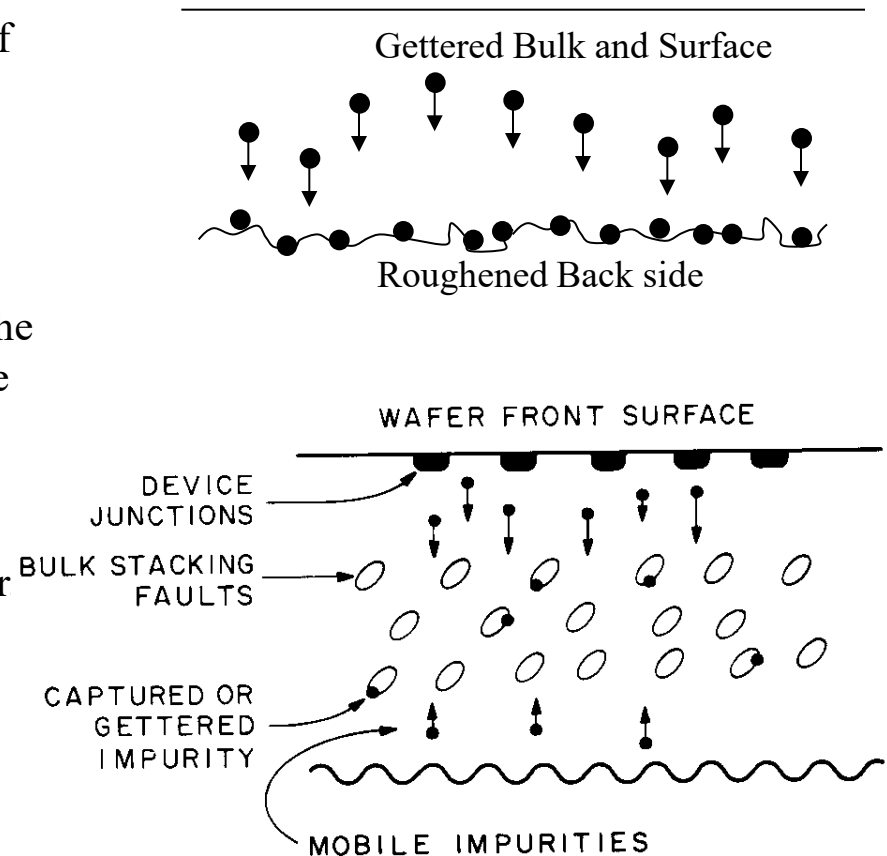

Intrinsic stacking fault

Volume Defects: Precipitates

Precipitates are three dimensional defects that have a different chemical makeup from the host lattice. They can result from an impurity exceeding the maximum solubility of the crystal (much like supersaturation of sugar in water). Generally, these defects are harmful, but they do have some technological value - oxygen gettering to form a denuded zone and As precipitates for high speed optical devices.

•External Gettering: Roughing the backside of the wafer to provide a low energy "sink" for impurities.

Gettered Bulk and Surface

Roughened Back side

•Internal gettering: Using internal defects to trap impurities moves impurities away from the active region of the wafer, were transistors are to be formed. Oxygen precipitates are the gettering sites. 15 to 20 ppm Oxygen wafers are required. Less than 15 ppm - precipitate density is too sparse to be an effective getterer Greater than 20 ppm, wafers tend to warp during the high temperature process. Note: devices that use the entire wafer as the active region (solar cells, thyristors, power diodes, etc...) cannot use this technique, but can use extrinsic gettering. Today, most wafer manufactures perform this task.

WAFER FRONT SURFACE

DEVICE JUNCTIONS

BULK STACKING FAULTS

CAPTURED OR GETTERED IMPURITY

MOBILE IMPURITIES

Volume Defects: Oxygen Precipitates

A given denuded zone may need to have minimal Oxygen (to prevent precipitation in the active regions of devices during later thermal cycles) and be of a required depth (enough "clean material to form the active device region).

These are determined by:

Concentration of DISOLVED Oxygen in Si

$$[\text{Oxygen in Si}] = \left(2x10^{21} \frac{atoms}{cm^3} \right) e^{-1.032eV/kT}$$

$$L_d = \sqrt{\left(0.091 \frac{cm^2}{\sec} \right)(t) e^{-1.2eV/kT}}$$
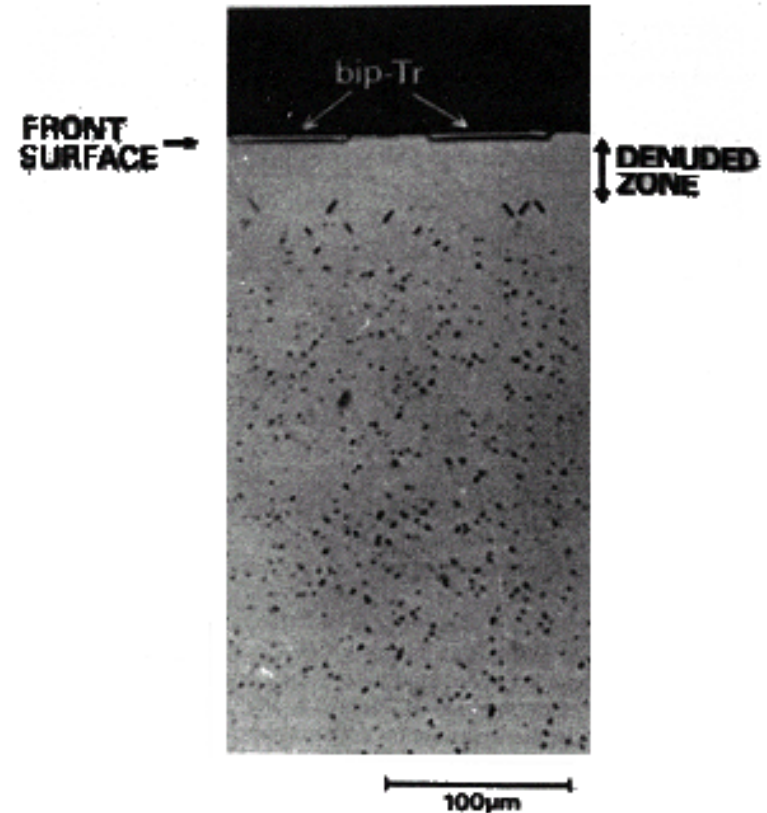
Figure 2-11 Cross section view of denuded wafer with bipolar transistor (*reprinted by permission, Academic Press, after Shimura*).