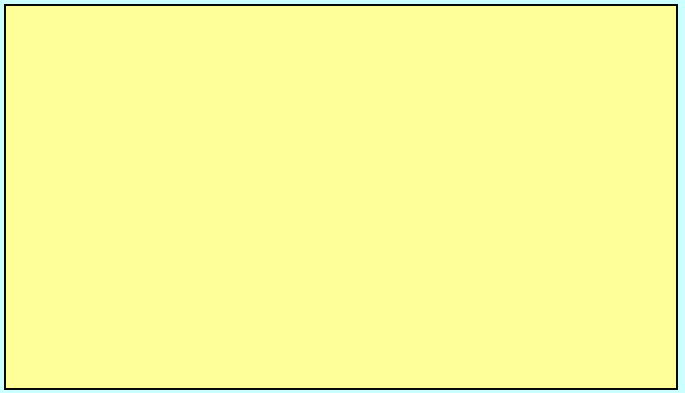
In Class Example of a "Simplified" Inverter Mask set: You probably will not want to print this file.

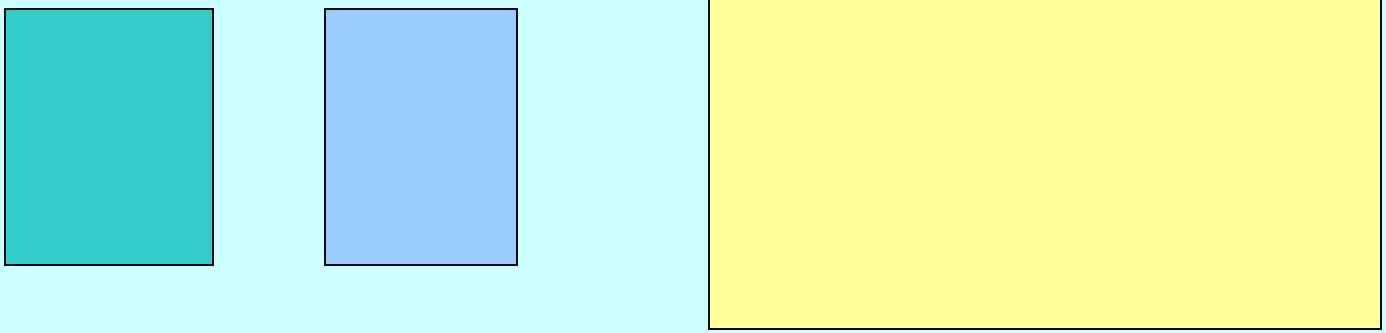
Note: this example is meant to show effects of resolution and alignment only and is NOT the process used to produce most CMOS inverters

Top View of a p-type wafer

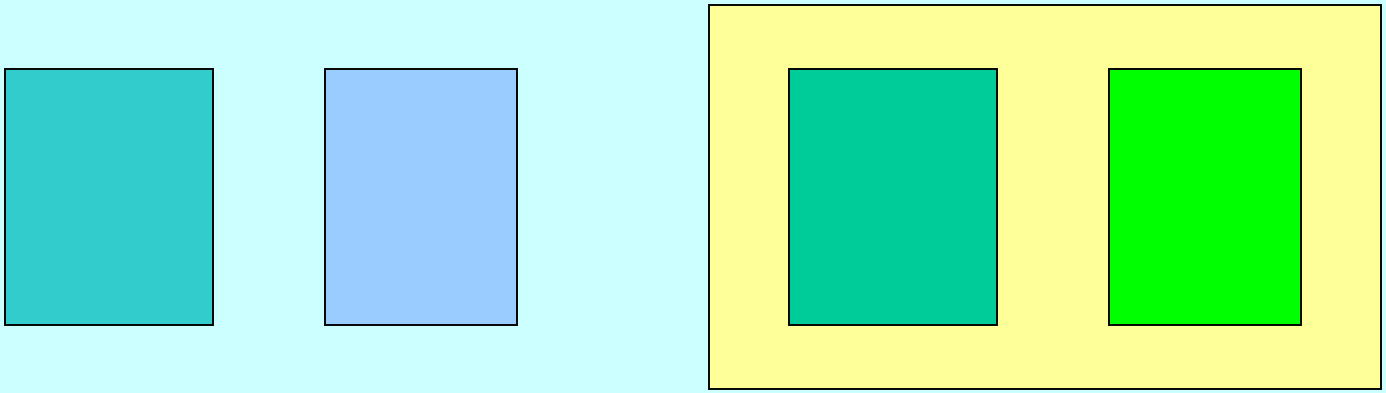
In Class Example of a "Simplified" Inverter Mask set: Probably will not want to print. Note: this example is meant to show effects of resolution and alignment only and is NOT the process used to produce most CMOS inverters



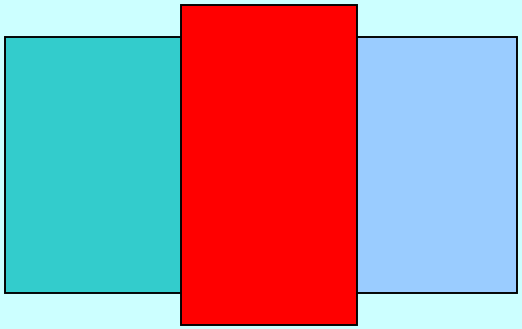
…open windows in oxide and add n-type well

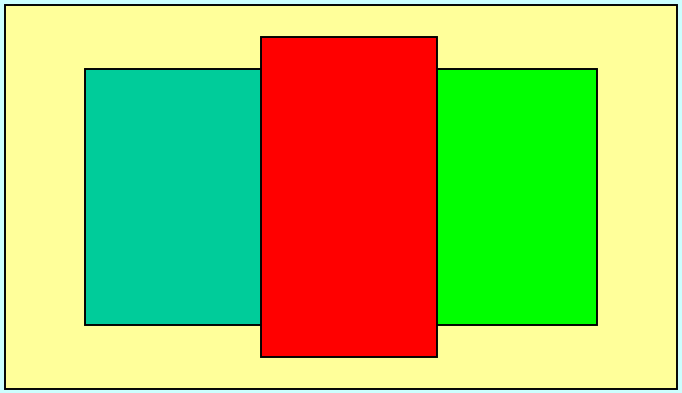


…open windows in oxide and add NMOS source/drain

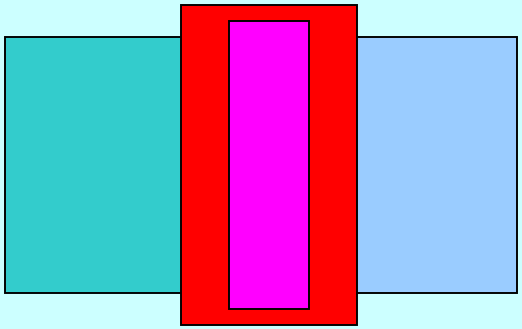


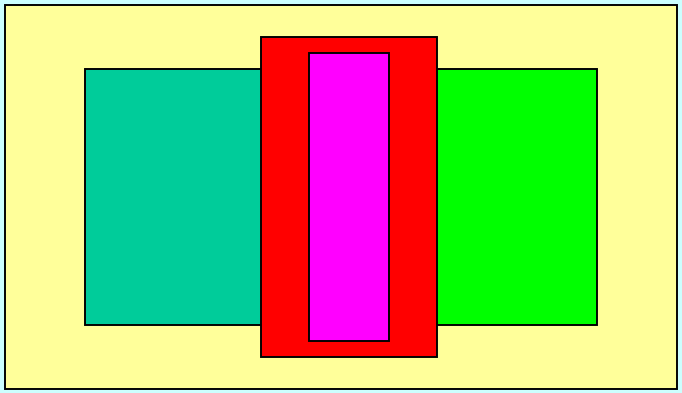
…open windows in oxide and add PMOS source/drain



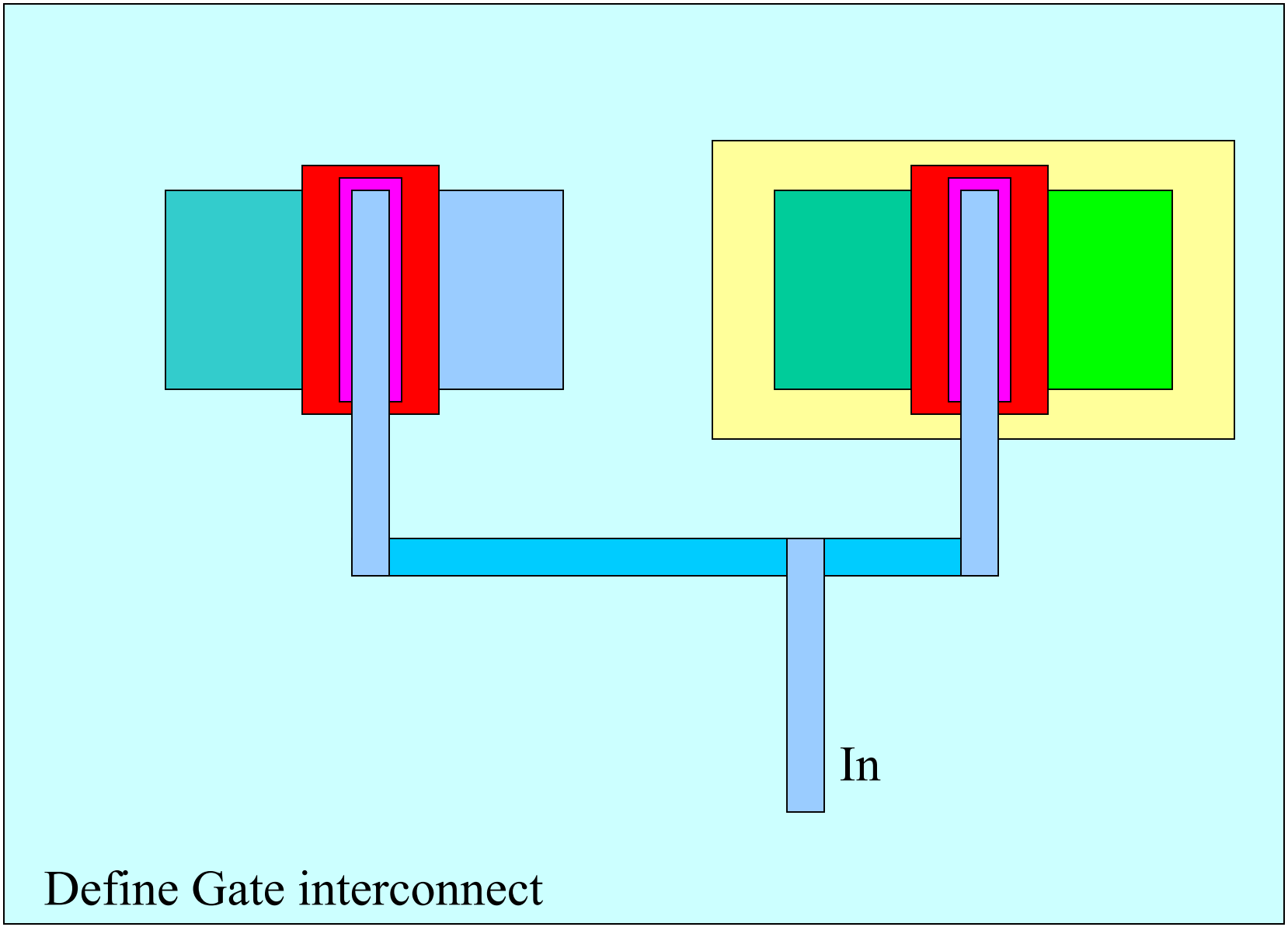


Define the gate oxide

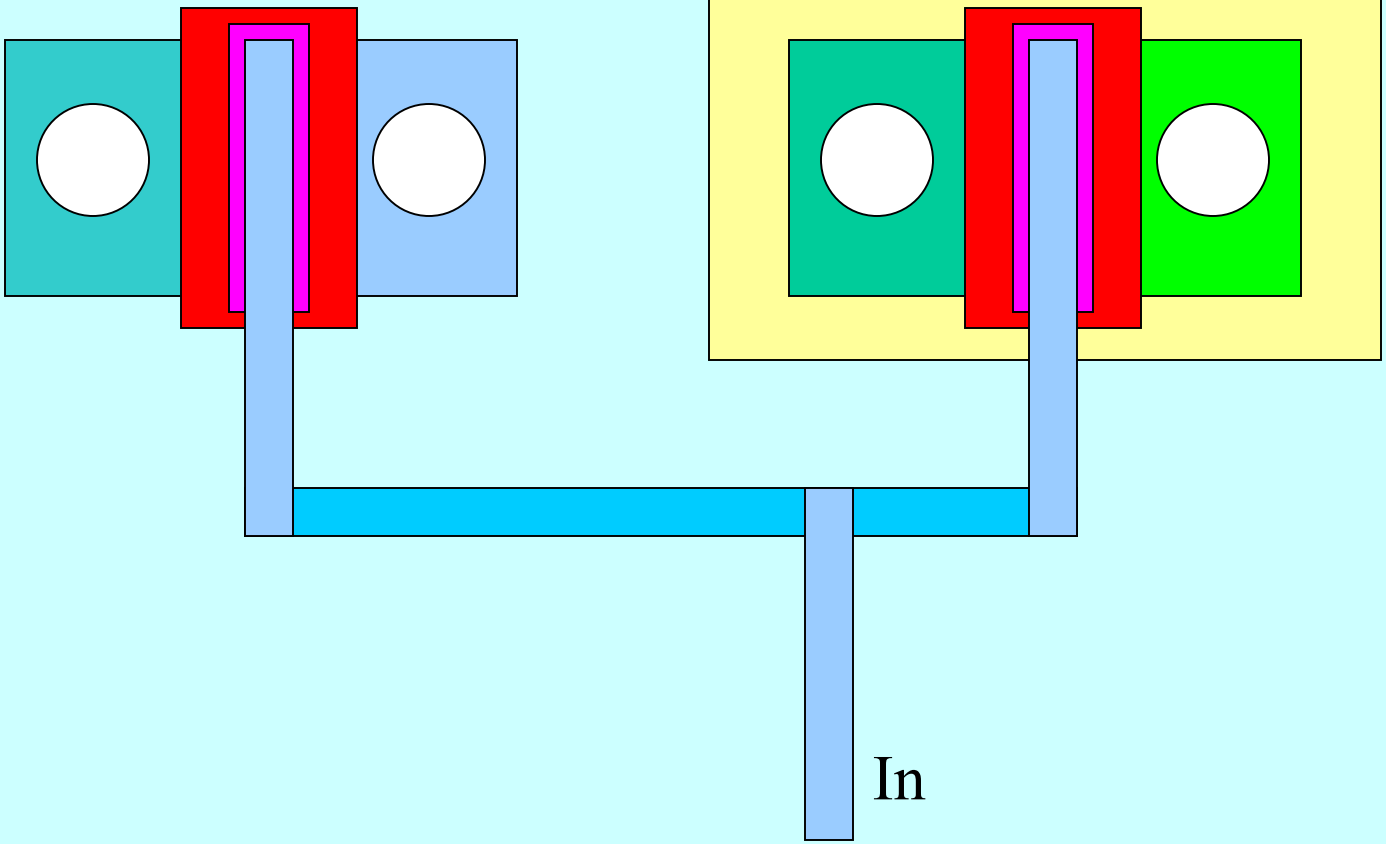




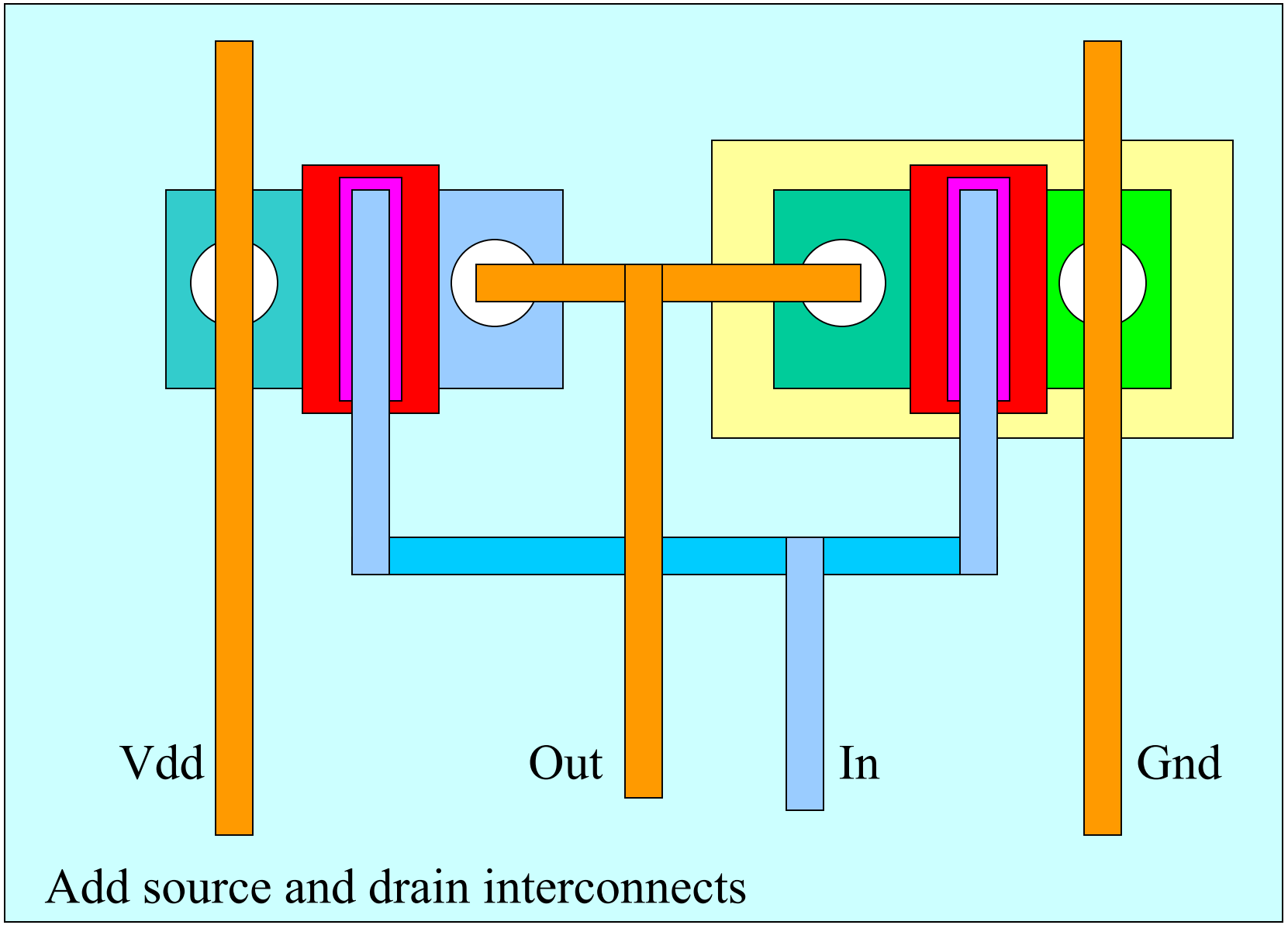
Define the contact to the gate



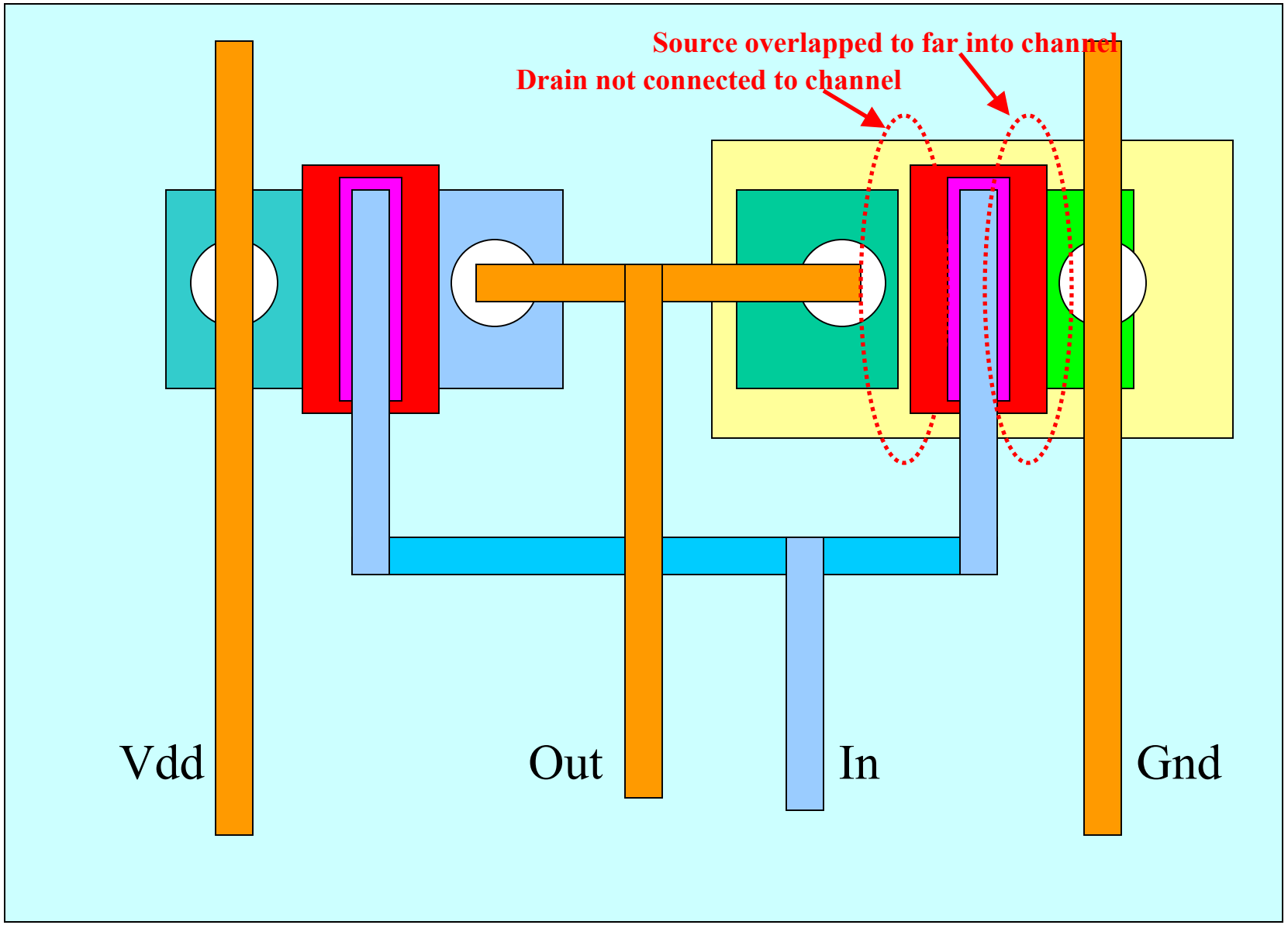
Define Gate interconnect



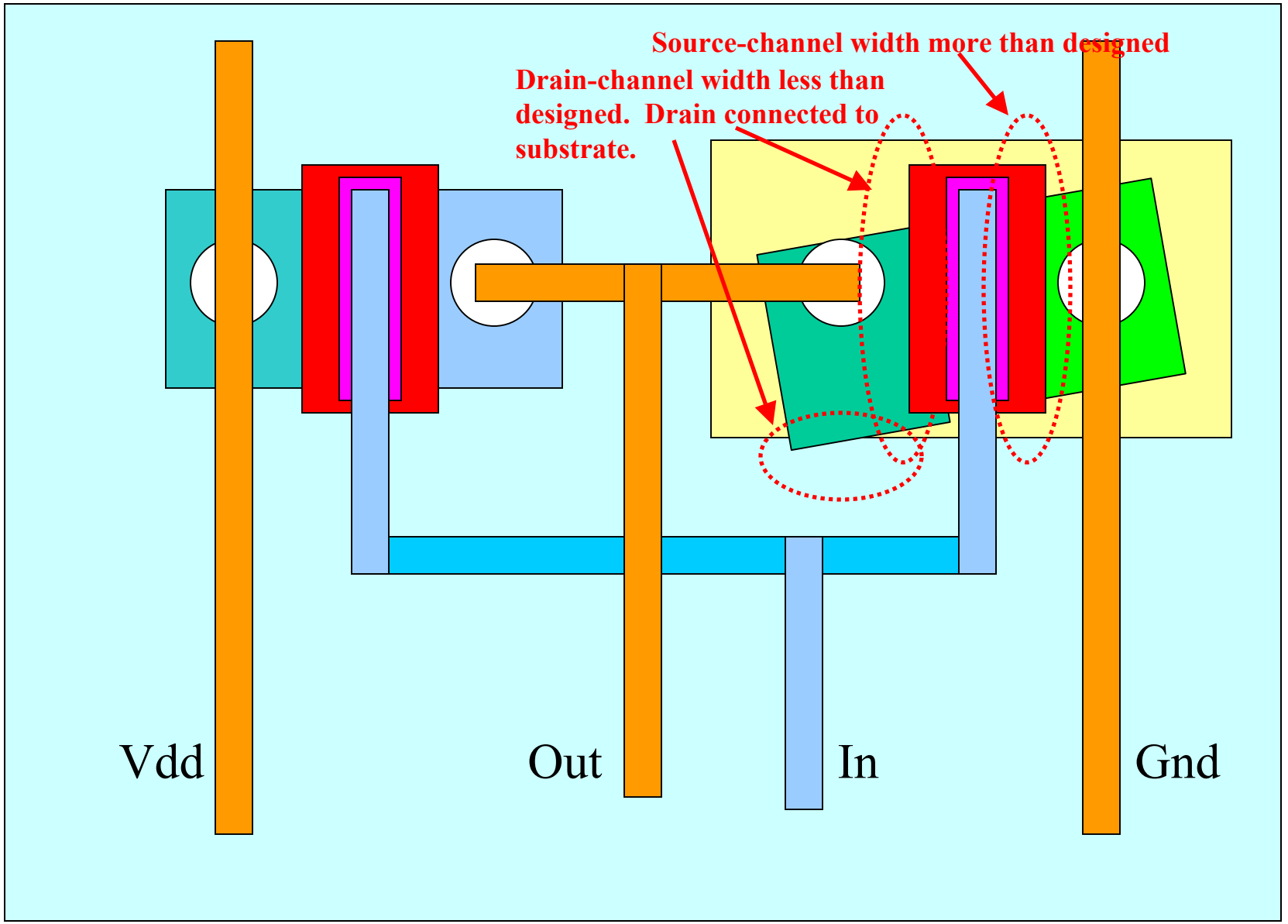
Open contacts to the source and drain


Vdd
Out
In
Gnd
Add source and drain interconnects

Effect of improper Registration (Source/drain PMOS Mask layer)



Effect of improper Registration (Source/drain PMOS Mask layer)



Effect of improper Resolution (Gate contact window of NMOS Mask layer not resolved)